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Lab 8 — CPU Datapath

Objectives

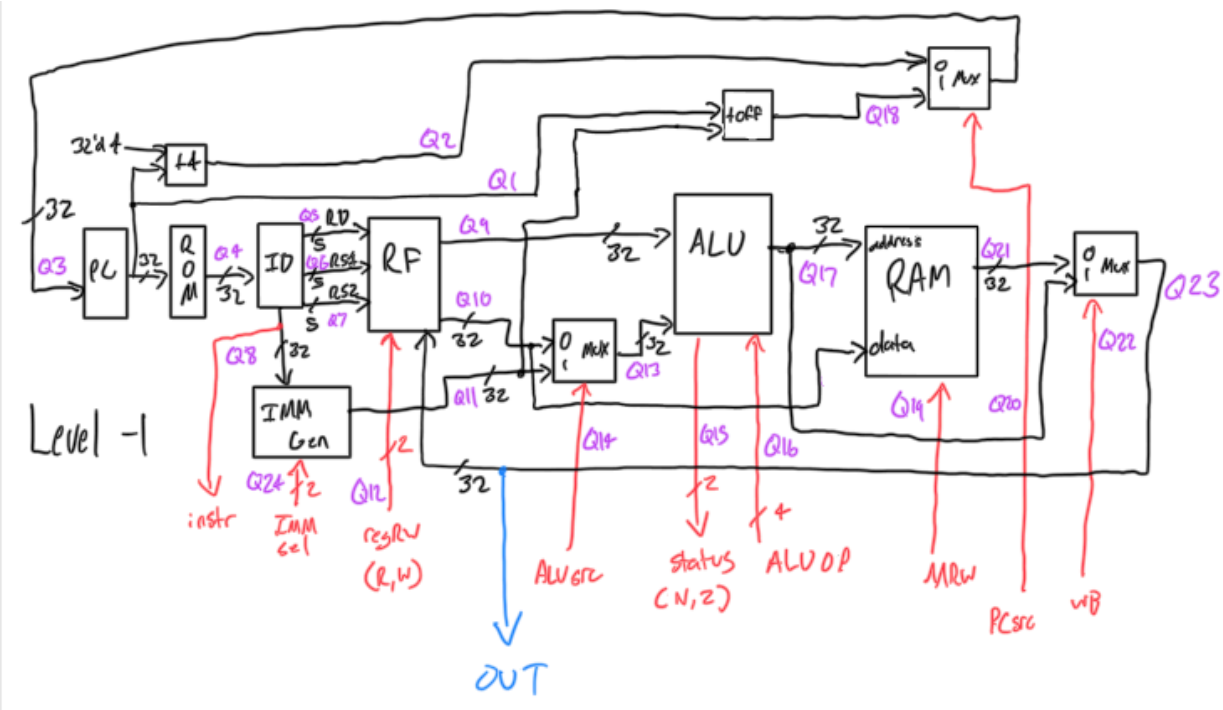
For this lab, I am creating a single cycle CPU datapath for a processor which uses RISC-V ISA. It will be created ready to connect to a companion control unit.

Introduction

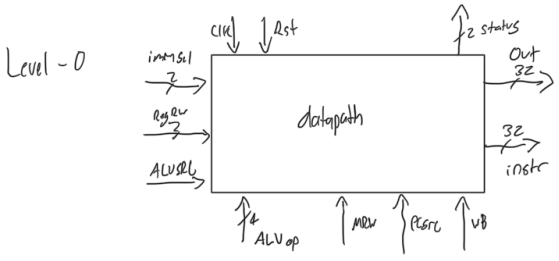
The datapath in a processor consists of the program counter, instruction decoder, arithmetic logic unit, RAM, and accompanying hardware. It's what fetches instructions, decodes them, reads and processes data from the register file and RAM, and writes them back for later use or as an output.

Methodology

The following is a level -1 diagram of my CPU datapath. It has a 2 bit IMMsel input, 4 bit ALUop input, and regRW input, ALUsrc input, MRW input, PCsrc input, and WB input. These will all be connected to the outputs of the processor control unit. Additional inputs are clock and reset, and are shared inputs with the control unit. The datapath has a status output from the ALU and 32 bit instruction output. These are connected to the control unit as inputs. Finally, there is a final output which is 32 bits wide.



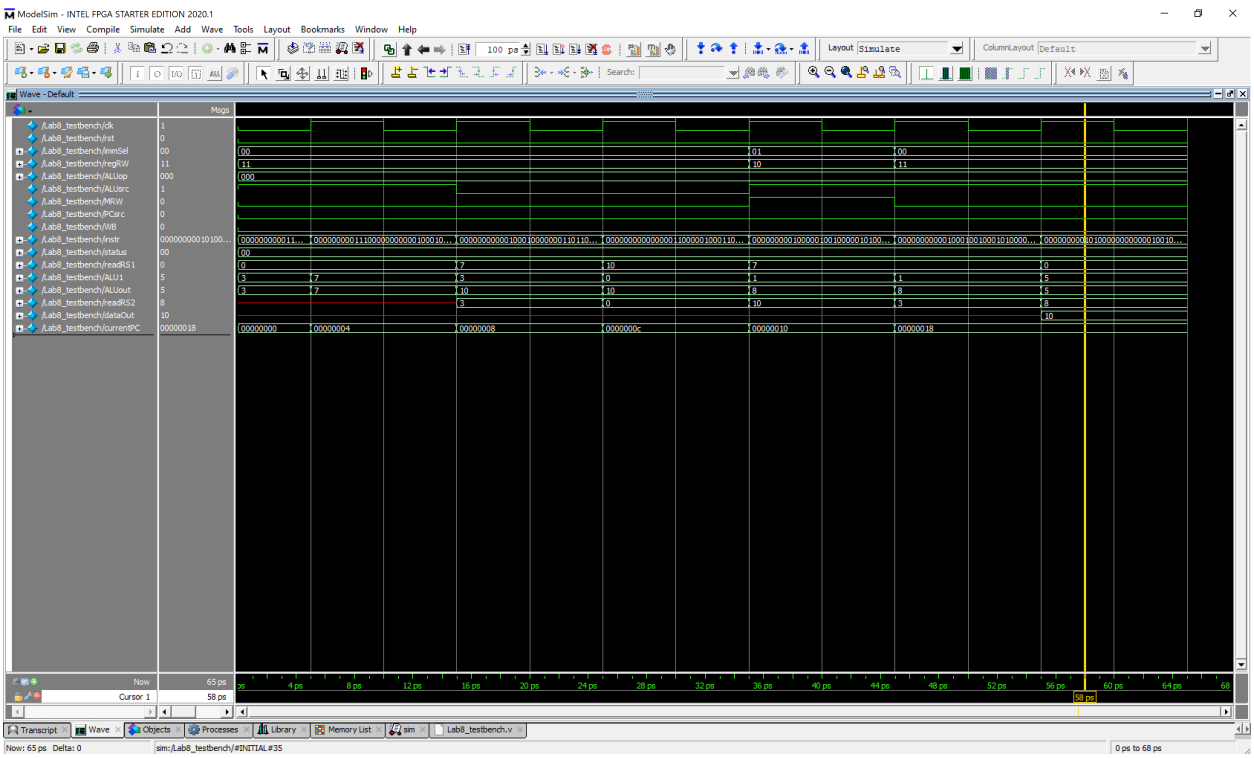
This is a level -0 diagram of my CPU datapath.



The datapath executes instructions found in the ROM by using the register file, arithmetic logic unit, and RAM. For this to work, the control inputs must be correct for each cycle and correspond to the current instruction.

Result and analysis

When tested in ModelSim, the datapath is found to be fully functional. It is tested with each type of instruction. For each instruction, the expected output is equivalent to what the datapath calculates.



Branch instruction testing is not included in this report, although it is tested and fully working. For these test results, look to Lab 9 or my final project submission.

All code, diagrams, and simulation results can be found as files on GitHub: https://github.com/Eth7an/Lab-8.git

A video explanation of the top level design and ModelSim simulation can be found here: https://youtu.be/RX16spnfzl4

Discussion and Conclusion

To conclude, I have built a fully working and tested CPU datapath. By mimicking a control unit in the testbench, we know that when connected to a functional control unit this will form a full RISC-V ISA processor.