 **ECE 09243 (Spring 2022)**

**Lab#8 (2 weeks Lab)**

**Task Description: You have to create a** **datapath for a processor which uses RISC-V ISA for all basic instruction.**

1. Draw the level -0, level-1 block diagram . (10 points)
2. Write a Verilog code and also the testbench for the above design. (10 points)
3. Simulate it in ModelSim and analyze it with a proper Modelsim screenshot. For each of the group members, please add your simulation and analysis. (10x3=30 points)
4. Make a video of your top-level design where you will explain the diagram and ModelSim simulation. Your video can be 3-5 minutes long. Share the link in your report. (10 points)
5. Create an account in Github upload your code with a proper ReadMe file and share the link. (10 points)
6. Write a report (20 points)
7. Individual Contribution (10 points)

**Report Writing Instruction:** ( This assignment can be done as a group/individual assignment. One group can have a maximum of 3 members in the group)

1. Contribution chart
2. Objectives
3. Introduction
4. Methodology (This should include all the components of your top-level, the diagram, and the truth tables)
5. Result and analysis (Modelsim screenshot, video link, Github link)
6. Discussion and Conclusion

**Sample Contribution Chart**:

|  |  |  |  |
| --- | --- | --- | --- |
|  | Member ‘A’ | Member ‘B’ | Member ‘C’ |
| Initital research |  |  |  |
| Part 1-coding |  |  |  |
| Part1-simulation |  |  |  |
| Part3-simulation |  |  |  |
| Video making |  |  |  |
| Report writing |  |  |  |