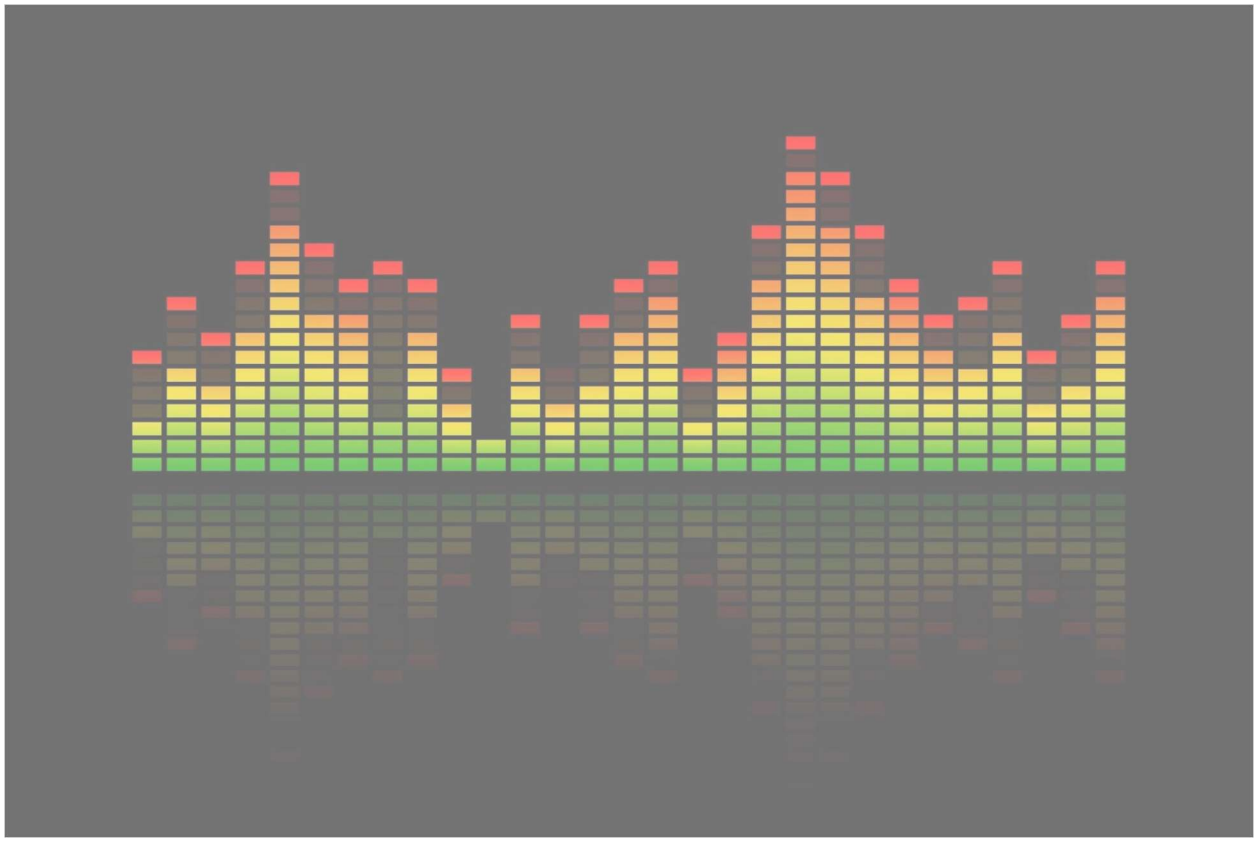

Audio Volume Unit Meter Hardware Readiness Report

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Table of Contents

Executive Summary 3
Electrical Design Details 3
Arduino Due Microprocessor 3
Op-Amp Selection 3
Shift Register Selection 4
LEDs Selection 4
Power Supply 4
Linear Voltage Regulator – Thermal Analysis 5
Summation Circuit – Design Analysis 6
Active Bandpass Filters – Design Analysis 7
Rectification/RC Circuit – Design Analysis 10
Sensitivity/Gain Circuit – Design Analysis 12
Signal Conditioning (Stretch Goal) – Design Analysis 12
Schematic Diagram and Walkthrough 14
Printed Circuit Board 24
Enclosure Drawings 26
Wiring Diagram 27
Hardware Test Plan 27
Parts List 30

Executive Summary

The purpose of this document is to describe the hardware design for the Audio Volume Unit Meter. The subsystems that comprise the Audio Volume Unit Meter are the Arduino Due microprocessor, shift registers, active bandpass filters, rectifier RC circuits, summation circuit, gain stage circuit, sensitivity circuit, signal conditioning (stretch goal) circuit, and the LEDs matrix. These subsystems have been designed and their analysis and circuit walkthrough are explained in this report. The Audio Volume Unit Meter will use a plastic enclose which will allow for the device to be easily transportable. This report will show that all of the hardware is ready for procurement and assembly of the unit should begin immediately. The biggest challenge of making this possible has been the layout of the Front-End PCB. This, however, has been solved in a timely mannered. This report includes hardware design calculations, the schematic diagrams of the device, the parts list, and the plan for testing all crucial hardware components prior to integrating them with firmware.

Electrical Design Details

Arduino Due Microprocessor

The Arduino Due microcontroller was selected for this device because it has an 84 MHz, 32-bit ARM microprocessor which is required for the Digital Signal Processing (DSP) operations for our stretch goal design which will be described in the signal conditioning section of this document. Also, the Arduino Due has a total of 8 ADC inputs which are required for the Audio Volume Unit Meter. The Due has a 12-bit ADC which gives us the resolution of about 805.6µV as shown in Equation 1.

$$Resolution = \frac{3.3V - 0V}{2^{12}} = 805.6\mu V$$

Equation 1 - ADC Resolution

$$dB = 20\log_{10}\left(\frac{3.3V}{805\mu V}\right) = 72.24dB$$

Equation 2 - Minimum Detectable Signal by ADC in dB

This means that our ADC can detect a signal that is approximately -72dB as show in Equation 2. The Audio Volume Unit Meter only needs the ADC to detect signals of approximately -24dB therefore, this 12-bit ADC will suffice. The Arduino Due will be powered by an 9V supply that is regulated from the 12V power input, which will be described in the power supply section of this document.

Op-Amp Selection

The Audio Volume Unit Meter uses two types of op-amps, and they are the TLV9302 and LMC6482. The TLV9302 and LMC6482 op amps are rail-to-rail with a maximum differential voltage of 18V and 16V respectively. All op-amps are powered up by a ±5V supply regulated from the 12V power input which, again, will be described later in the power supply section of this document. Rail-to-Rail op-amps were selected to preserve the integrity of the audio signal peak voltages as much as possible. The TLV9302 op-amps are used as voltage followers, summation of two audio channels (left and right), sensitivity to control the loudness of the audio signal, and most importantly as active bandpass filters. The LMC6482 op-amp is only used as an ideal rectifier. Note that the TLV9302 is perfectly capable of being used as an ideal rectifier, however, due to a low supply of the TLV9302, the LMC6482 op-amp is a viable candidate.

Shift Register Selection

The Audio Volume Unit Meter uses the SN74HC595NE4 shift register to multiplex more digital pins which in turn supply current to the 56 LEDs matrix. The shift register is an 8-bit serial-in, parallel-out and it is controlled by the Audio Due. It can supply a maximum current of 35mA per output and 70mA total for the part. Each LED is configured to consume about 2mA and so16mA total for each shift register. Therefore, the SN74HC595NE4 shift register will handle this current demand with ease.

LEDs Selection

The LEDs selected for the Audio Volume Unit Meter come in three colors: red, green, and yellow. Their lens transparency is diffused with a forward voltage of 1.9V, 1.9V, and 2.4V respectively. There is a total of 56 LEDs used and each LED will consume 2mA and so 112mA in total. This LED was chosen due to its low current consumption which reduces the current demand from the 9V regulator.

Power Supply

The Audio Volume Unit Meter uses two RS-35-12 power supplies. Figure 1 shows how the power supplies are connected to the Front-End PCB board via terminal block. What is not shown on Figure 1 is the power input receptable 703W-00/04 which is responsible for connecting the inputs of the power supplies to the wall socket via a power cord. The ±12V are then sectioned off into three different voltages via voltage regulators: 9V, 5V, and -5V. The 9V supply powers up the Arduino Due and the 56 LEDs, while the ±5V powers up the op-amps. The RS-35-12 power supplies were chosen due to having a clean DC output voltage with minimal distortions. This will in turn, not degrade our audio signal.

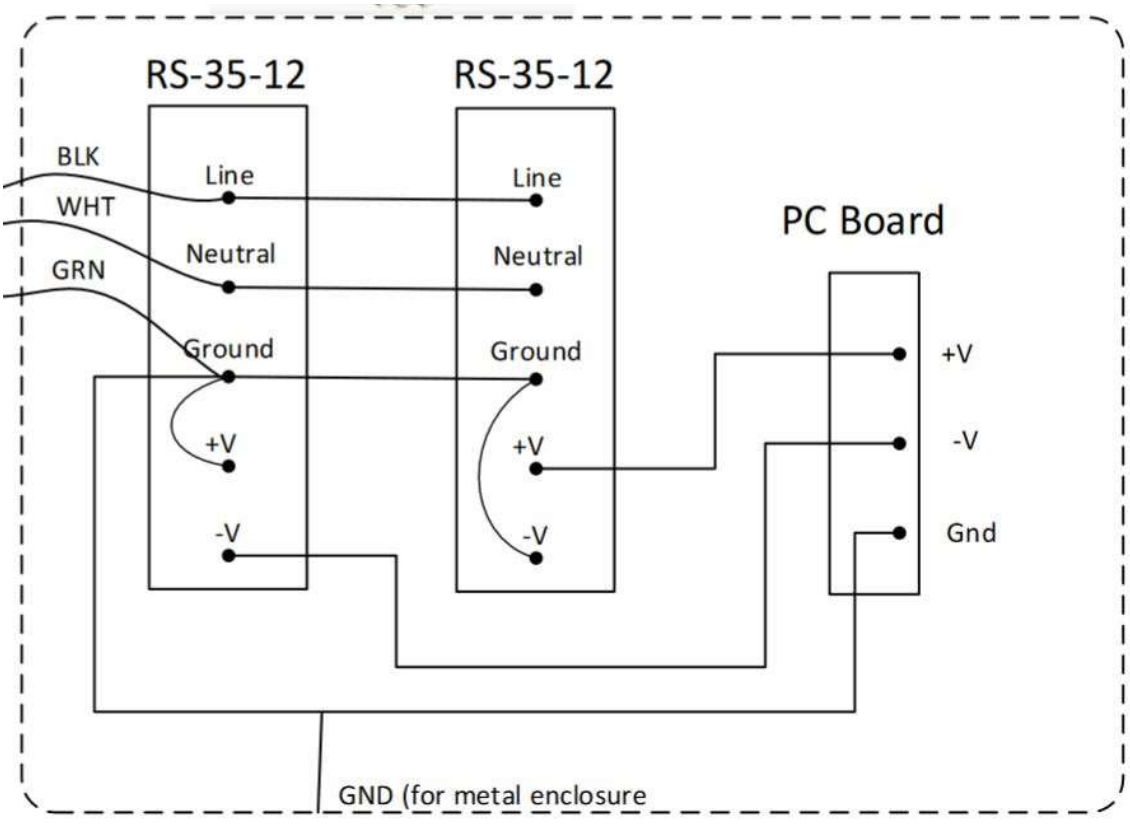

Figure 1 - ±12V Power Supply

Linear Voltage Regulator – Thermal Analysis

To determine whether the selected voltage regulators need a heat sink, we must calculate the voltage that needs to be dissipated across the regulator and the output current. Equation 3 shows the voltage dissipated across the 9V regulator while Equation 4 shows the voltage dissipated for the ±5V regulators. For the output current, the worst-case scenario is considered. If the worst case does not need a heat sink, then no heat sink is needed.

$$V_{diss} = V_{IN} - V_{OUT} = 12V - 9V = 3V$$

Equation 3 - 9V Regulator Voltage Dissipated

$$V_{diss} = V_{IN} - V_{OUT} = 12V - 5V = 7V$$

Equation 4 - ±5V Regulator Voltage Dissipated

The maximum current for the 9V voltage regulator output is 0.5A. This results in a 1.5 watts dissipation for the 9V regulator as shown in Equation 5. The thermal resistance between the TO-220 case and ambient is 50 °C/W, so the rise in temperature between ambient and the junction is 75.0°C as shown in Equation 6. At room temperature (25°), the junction temperature will be 100°C which is well below the maximum for the TO-220. As a result, no heat sink will be used.

$$P = 9V * 0.5A = 1.5W$$

Equation 5 - Power Dissipated across 9V Regulator

$$T = 1.5W * 50\frac{°C}{W} = 75.0°C$$

Equation 6 - Temperature between ambient and the junction

The maximum current for the ±5V voltage regulator output is 0.5A. However, approximately 0.1A will be used by all operational amplifiers if possible. This current value is an educated guess as the op-amps will consume far less than 0.1A. This is because the resistors used in all op-amp configurations are of high resistance values which, in turn will drive less current. This results in a 0.7 watts dissipation for both regulators as shown in Equation 7. The thermal resistance between the TO-220 case and ambient is 50 °C/W, so the rise in temperature between ambient and the junction is 35.0°C as shown in Equation 8. At room temperature (25°), the junction temperature will be 60.0° which is well below the maximum for the TO-220. As a result, no heat sink will be used for both regulators.

$$P = 7V * 0.1A = 0.7W$$

Equation 7 - Power Dissipated across ±5V Regulator

$$T = 0.7W * 50\frac{°C}{W} = 35.0°C$$

Equation 8 - Temperature between ambient and the junction

Summation Circuit – Design Analysis

The summation circuit shown in Figure 2 allows for the left and right audio channels to be summed into a single channel. This is required since the audio jack used is a stereo jack. This means that audio gets split into two channels, a left and a right one. By using KVL the following equation, equation 9, is obtained.

$$\frac{V_1 - V_{IN}}{R_1} + \frac{V_2 - V_{IN}}{R_2} = 0$$

Equation 9 - KVL at node V1 and V2

Let $R = R_1 = R_2$

$$V_{IN} = \frac{V_1 + V_2}{2}$$

Equation 10 - Summation Op-Amp Input Voltage

As shown in Equation 10, both the left and the right audio channels are summed but the voltage is reduced by half. To fix this problem, the summation op-amp needs a gain factor of 2. A non-inverting configuration is used as seen in Figure 2.

$$V_{OUT} = 1 + \frac{R_4}{R_3}$$

Equation 11 - Non-Inverting Voltage Gain

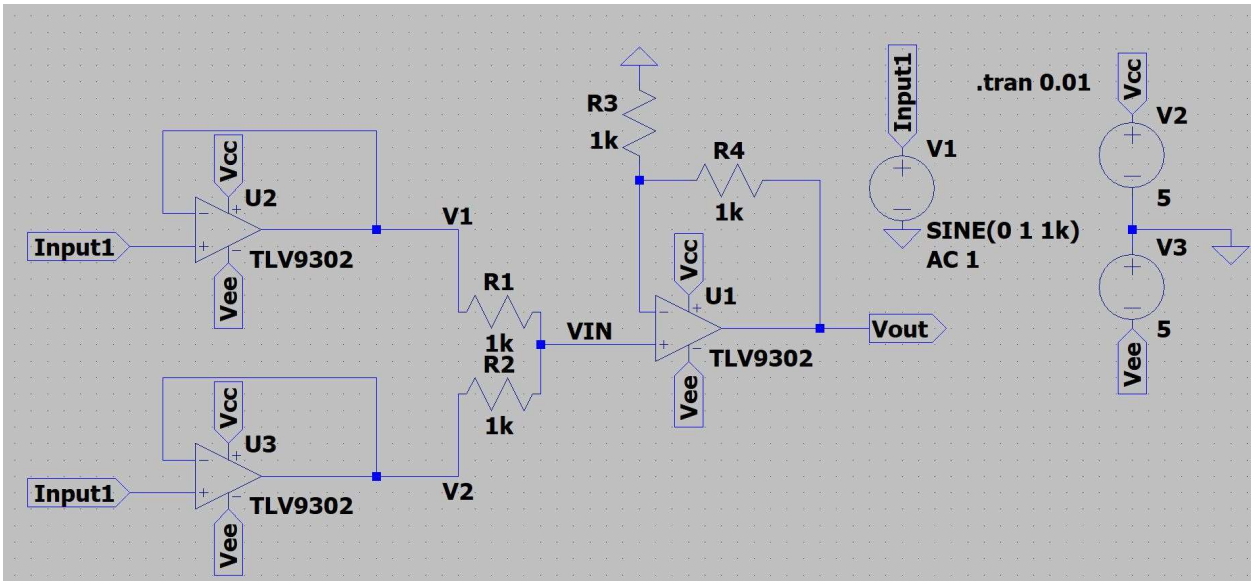

Figure 2 - LTSpice Summation Circuit

As shown in Equation 11, the lowest gain possible with a non-inverting op-amp configuration is of 2 and this is achieved by setting $R_3 = R_4$. To draw minimal current, resistors of 1kΩ were chosen.

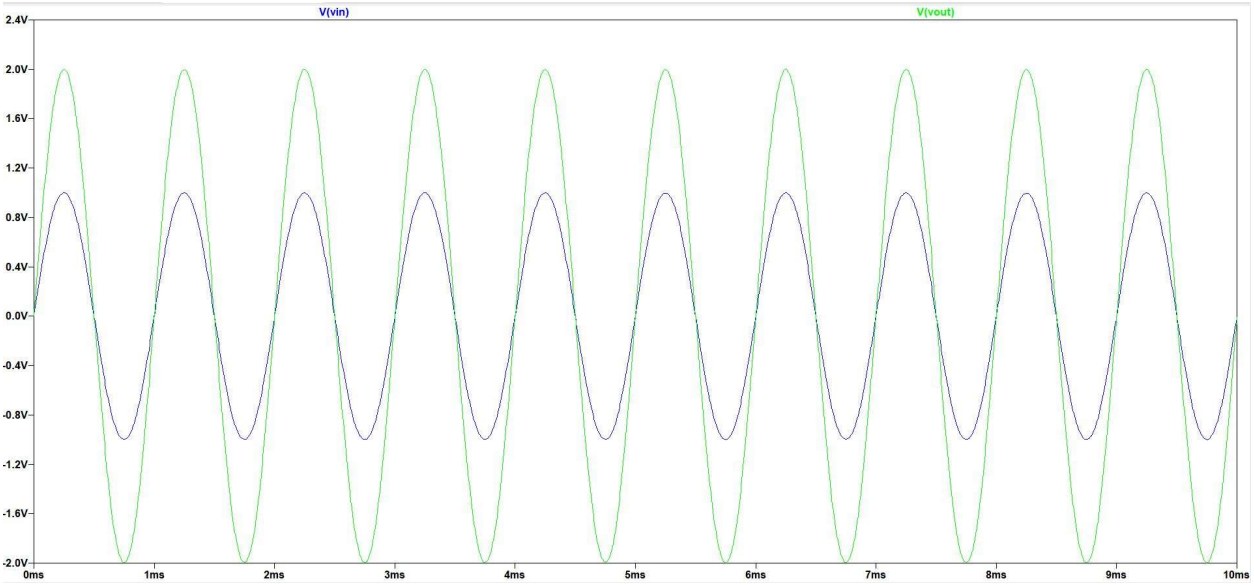

Figure 3 - LTSpice Summation Circuit Output

The output simulation is shown in Figure 3. Two 1kHz sine waves with a peak-to-peak voltage of 1V were placed at the input through a voltage follower configuration. This is to isolate impedances from the summation circuit and audio jack. The output is a 2V peak-to-peak sine wave at 1kHz. The resistors that will be used on the PCB are of 1kΩ with a tolerance of ±2%. This means that our gain will vary slightly, however, this tolerance will not cause issues with the design.

Active Bandpass Filters – Design Analysis

At the core of the Audio Volume Unit Meter are the active bandpass filters. These filters are responsible for the sectioning of the incoming audio signal into seven distinct frequency bins. The frequency bins were chosen based on common household audio equalizers. Sub-bass (20Hz – 60Hz), Bass (60Hz – 250Hz), Low Midrange (250Hz – 500Hz), Midrange (500Hz – 2kHz), Upper Midrange (2kHz – 4kHz), Presence (4kHz – 6kHz), and Brilliance (6kHz – 20kHz). To ensure that the frequencies of one bin do not interfere with the center frequency of its neighboring bins, filters were designed to have fast roll-off frequency. Since the smallest signal that the Arduino Due ADC needs to detect is -21dB, any frequency below this range must be considered as noise. In order to achieve this, fifth order Chebyshev active bandpass filters with a 0.5dB ripple in the passband were selected. This is because at around the center frequency, -40dB of attenuation is achieved effectively solving this issue. Also, active filters were used instead of passive filters since passive filters would require large inductor values at low frequencies. Active filters do not use inductors and so they are a more suitable candidate. The configuration of the active bandpass filters is two cascaded fifth order filters, a high-pass followed by a low-pass filter. To determine the resistor and capacitor values needed for this filter configuration a generalized transfer function must be obtained.

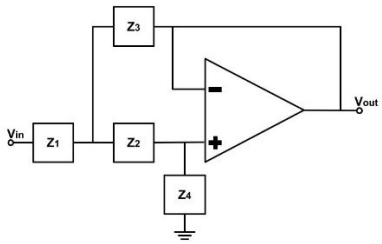

Figure 4 - Generalized Active Two Pole Filter Configuration

Figure 4 shows a generalized active two-pole filter configuration. To create a fifth order filter, it requires the cascading of a three-pole filter followed by a two-pole filter. Using basic ideal op-amp rules and KVL, Equation 12 was developed. The transfer function equation in Equation 12 can be used to design either a two-pole high pass or lowpass filter.

$$H = \frac{V_{OUT}}{V_{IN}} = \frac{Z_3 Z_4}{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 + Z_3 Z_4}$$

Equation 12 - Generalized Two Pole Filter Transfer Function

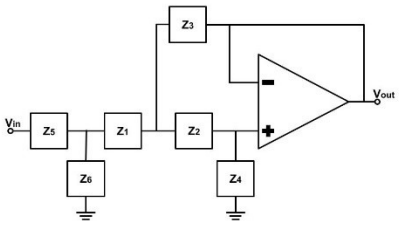

Figure 5 - Generalized Active Three Pole Filter Configuration

Figure 5 shows a generalized active three-pole filter configuration. Trying to apply KVL on this configuration can make deriving the transfer function quite difficult due to the additional pole added to the front-end of the op-amp configuration. Therefore, to make the configuration easier to solve a Thevenin approach was required. Equation 13 and Equation 14 reduce the additional pole to a simple Thevenin voltage and Thevenin impedance.

$$V_{TH} = V_{IN}\left(\frac{Z_6}{Z_5 + Z_6}\right)$$

Equation 13 - Thevenin Voltage of a Three Pole Filter

$$Z_{TH} = \frac{Z_5 Z_6 + Z_1 Z_5 + Z_1 Z_6}{Z_5 + Z_6}$$

Equation 14 - Thevenin Impedance of a Three Pole Filter

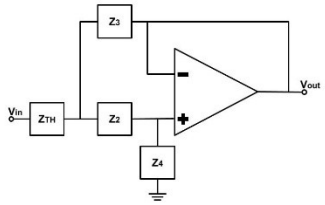

Figure 6 - Simplified Generalized Active Three Pole Filter Configuration

Figure 6 shows a simplified generalized active three-pole filter configuration. Now using basic ideal op-amp rules and KVL, Equation 15 was developed.

$$H = \frac{V_{OUT}}{V_{IN}} = \frac{Z_6}{Z_5 + Z_6} * \frac{Z_3 Z_4}{Z_{TH} Z_2 + Z_{TH} Z_3 + Z_2 Z_3 + Z_3 Z_4}$$

Equation 15 – Generalized Three Pole Filter Transfer Function

Having Equation 12 and Equation 15, MATLAB was used to determine the resistor and capacitor values. These values were used to construct the fifth order filters in LTSpice. Figure 7 shows the frequency response of these filters.

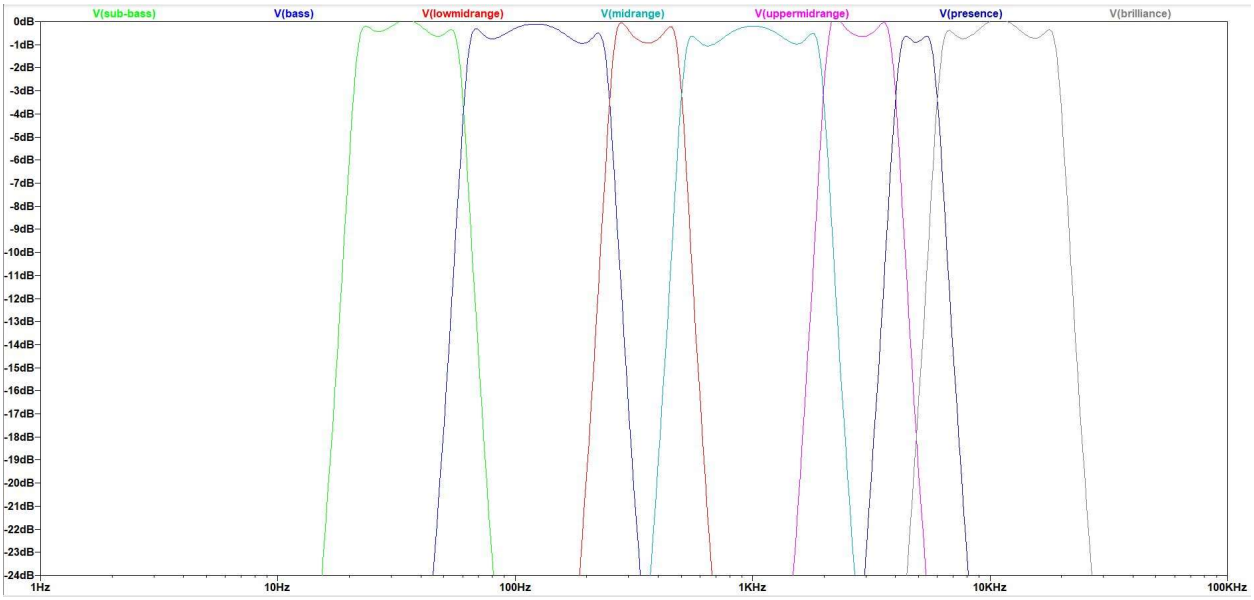

Figure 7 - LTSpice Ideal Active Bandpass Filters Frequency Response

This response shows ripple in the passband of about 1dB. This ripple attenuation will not affect our measurements since the bottom LED of each column represent -21dB, which is the lowest decibel level detectable by the device, while the top LED will represent 0dB, the highest decibel level. Starting from the bottom LED, each LED will represent a +3db increase. Therefore, if -1dB is detected by the input of the ADC, this will be interpreted as 0dB since -1dB is closest to 0dB then -3dB. If the ripple attenuation in the passband remains at 1dB or lower, our measurement will not be affected.

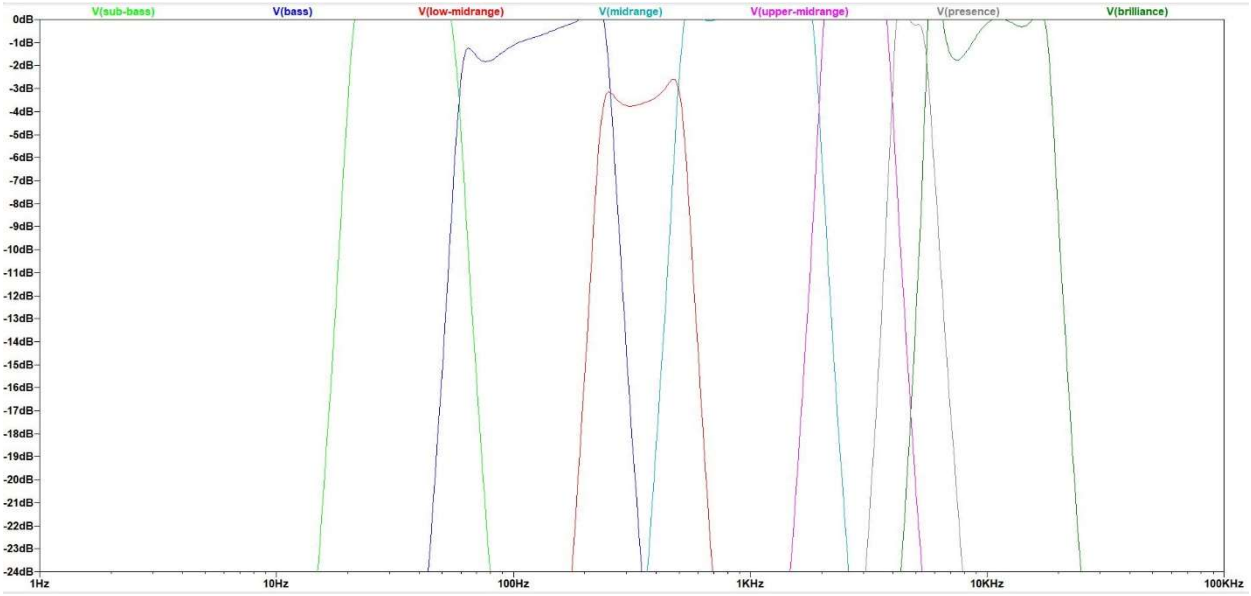

Figure 8 - LTSpice Non-Ideal Active Bandpass Filters Frequency Response

Figure 8 shows the frequency response of the seven active bandpass filters using in-house resistor components. As is evident, the Bass, Low Midrange, and Brilliance filters suffer significant attenuation in their passbands. This is because the in-house resistor components are not as close to the ideal values. To solve this issue, resistor values that are much closer to the ideal are required. This will add to our cost but will ensure a better quality in our active bandpass filters.

Rectification/RC Circuit – Design Analysis

The rectification and RC circuit condition the ac signal into a dc signal. This is achieved by first having the signal go through an ideal rectifier circuit. The ideal rectifier circuit will neglect the 0.7V drop from the diode and will maintain the peak signal integrity as shown in Figure 9.

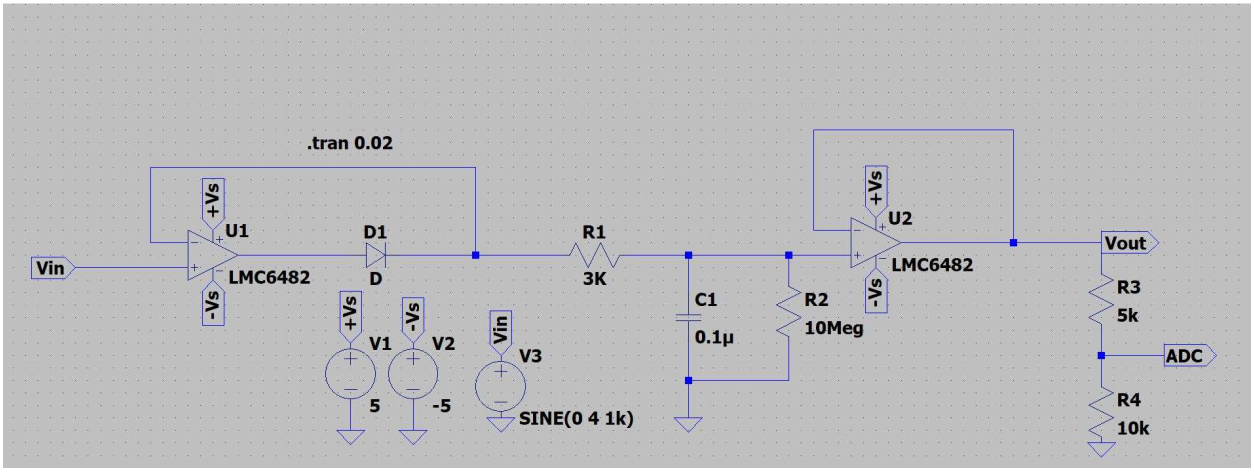

Figure 9 - LTSpice Rectification/RC Circuit

Next the rectified ac signal goes through a resistor capacitor configuration to convert it to a DC signal. To achieve this a fast attack time with a slow-release time was designed. The intent is for the capacitor to charge up to the peak value at a fast rate and discharge at a slow rate to give the ADC enough time to

sample the signal before the next incoming peak. Equation 16 and Equation 17 show the calculated attack and release times based on the chosen capacitor and resistor values.

$$\tau_{atk} = 3k\Omega * 0.1\mu F = 300\mu s$$

Equation 16 - Attack Time

$$\tau_{rel} = \frac{1}{10M\Omega * 0.1\mu F} = 1s$$

Equation 17 - Release Time

Since the rectified ac signal is expected to have a maximum peak voltage of 5V, a voltage divider is required to protect the ADC 3.3V pin. The maximum rated voltage on the ADC pin is 4V, therefore, a 5V signal will damage the ADC pin. Equation 18 shows that 5V will be mapped to 3.3V effectively protecting the ADC input.

$$V_{ADC} = \frac{10k\Omega}{10k\Omega + 5k\Omega} * 5 = 3.33V$$

Equation 18 - Voltage Divider

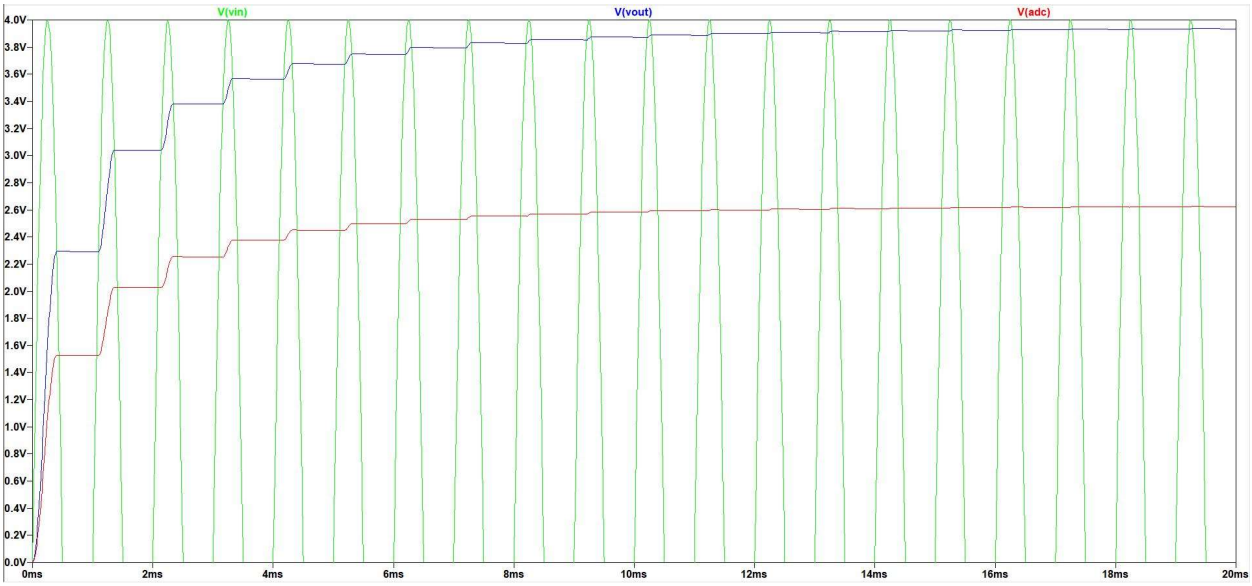

Figure 10 - LTSpice Rectification/RC Circuit Output

Figure 10 shows the output of when AC signal goes through rectification, DC conversion, and level shift. There is some voltage that is lost, however, it is minimal and will not affect our measurements.

Sensitivity/Gain Circuit – Design Analysis

The sensitivity circuit allows the user to control the relative loudness of the incoming audio signal. This is achieved by having a 500kΩ log potentiometer. The output of the summation circuit is connected to the log potentiometer. The log potentiometer will form a voltage divider, and the output is then fed to the gain stage. The gain stage is not a user control and is meant to only adjust once. To determine the correct gain needed, three different types of audio signals with different loudness will be fed into the audio jack and their respective peaks will be measured using an oscilloscope. Once the peaks are obtained, an average peak value will be determined and from this average peak, the gain will be set. This ensures that the highest peaks produced by the audio jack will be mapped to 5V.

Signal Conditioning (Stretch Goal) – Design Analysis

The signal conditioning circuit is a stretch goal for the digital design portion of the Audio Volume Unit Meter. This circuit is responsible for conditioning the audio signal such that the ADC can sample it as an AC signal rather than a DC signal. The expected audio signal will have a peak-to-peak voltage of 5V and no DC bias at the input of the signal conditioning circuit. Why the conditioning? This is because the ADC pin can only handle voltages between 0V and 3.3V. Anything higher or lower can potentially damage the ADC. Therefore, DC bias must be added to the incoming audio signal, and it must be attenuated such that 5V is mapped to 3.3V.

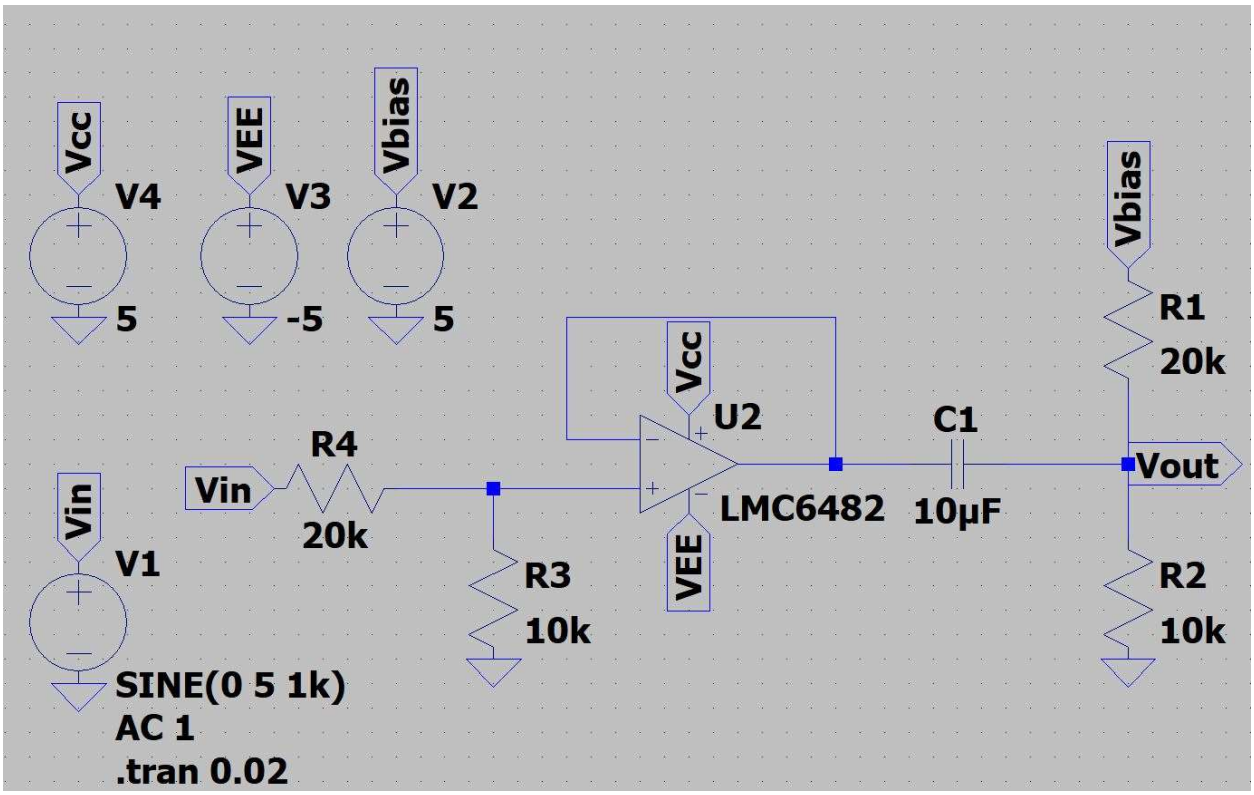

Figure 11 - LTSpice AC Signal Conditioning

Figure 11 shows the AC signal conditioning circuit. First the audio signal goes through a voltage divider. The goal here is to reduce the peak voltage of the incoming audio signal. Then the reduced audio signal goes through a voltage follower configuration. This keeps impedances isolated between the two voltage divider configurations. The output of the voltage follower goes through a voltage divider that adds a DC bias to the audio signal. This all effectively mapped 5V to 3.3V with a DC bias of 1.6V. Equation 19

shows that the two voltage dividers used are identical. This was necessary to produce an audio signal that the ADC can sample.

$$V_{OUT} = \frac{10k\Omega}{10k\Omega + 20k\Omega} * 5V = 1.6V$$

Equation 19 - DC Bias and Attenuation

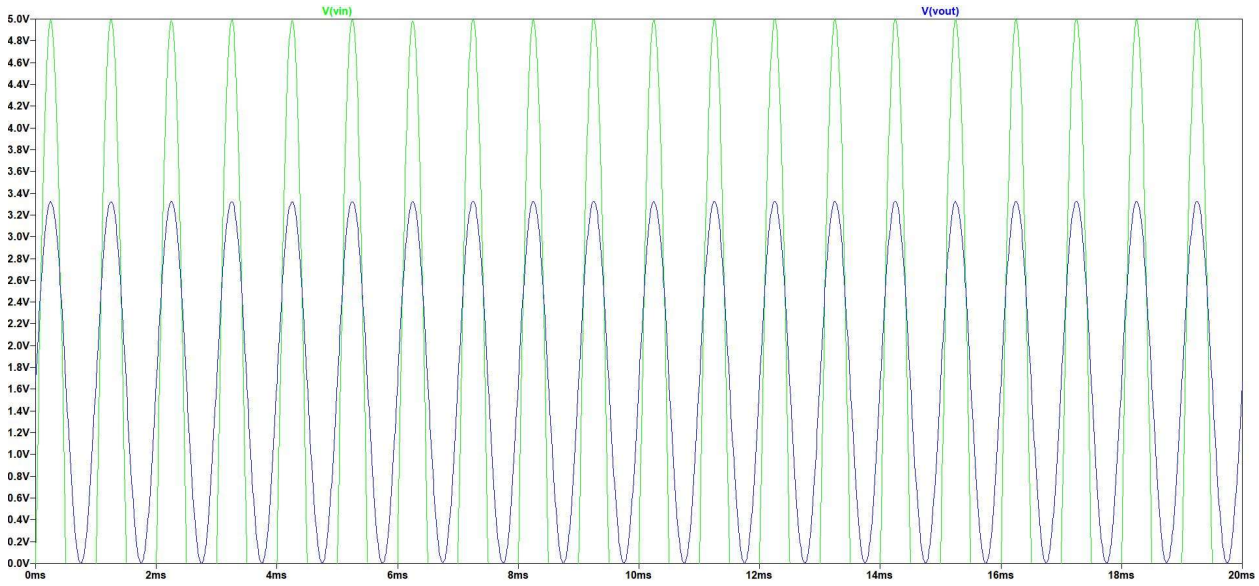

Figure 12 - LTSpice AC Signal Conditioning Output

Figure 12 shows the signal conditioning circuit output. The input signal is a 1kHz sine wave with a peak-to-peak voltage of 5V. The output is a 1kHz sine wave with a DC bias at 1.6V.

Schematic Diagram and Walkthrough

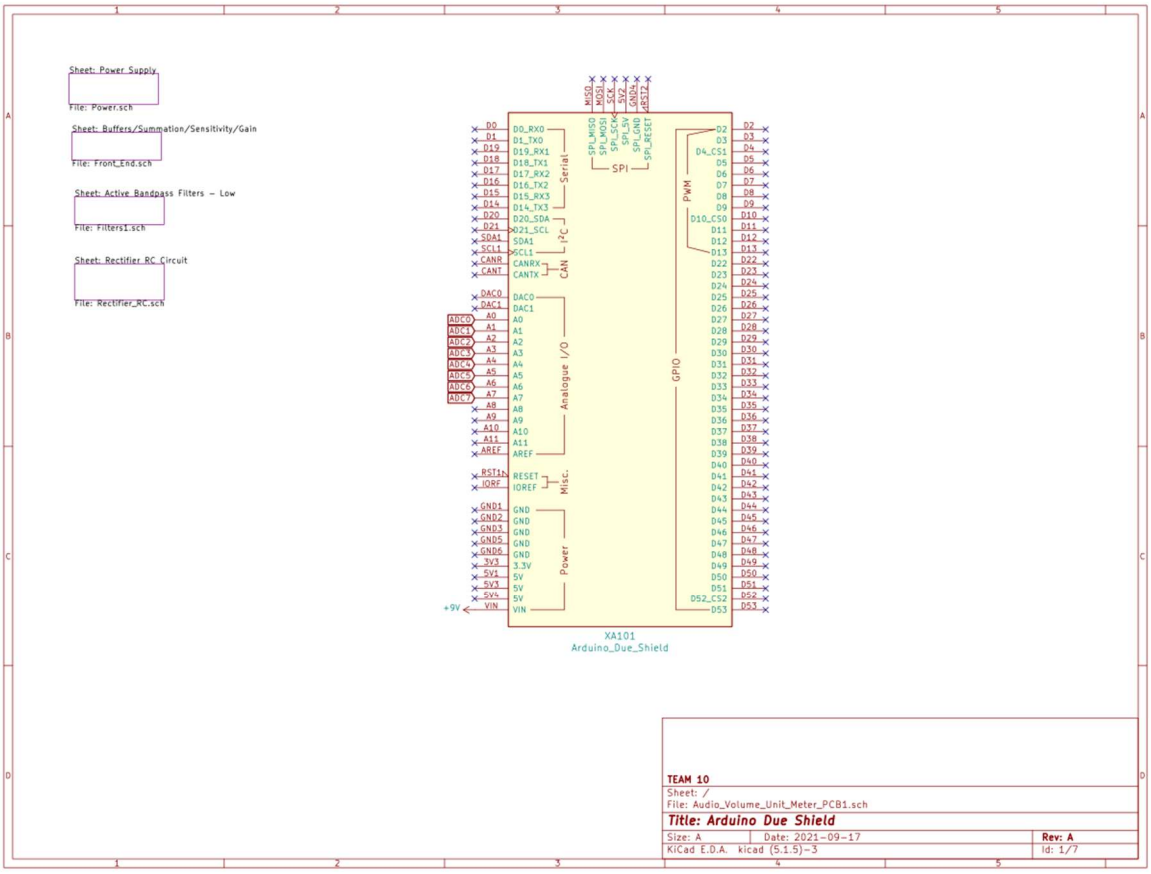

Figure 13 - Front End Arduino Shield PCB

The schematic diagram for the Arduino Shield part of the Front-End PCB is shown. These are the connection needed to attach the Arduino Due. The connection is directly routing in the Arduino Due ADCs.

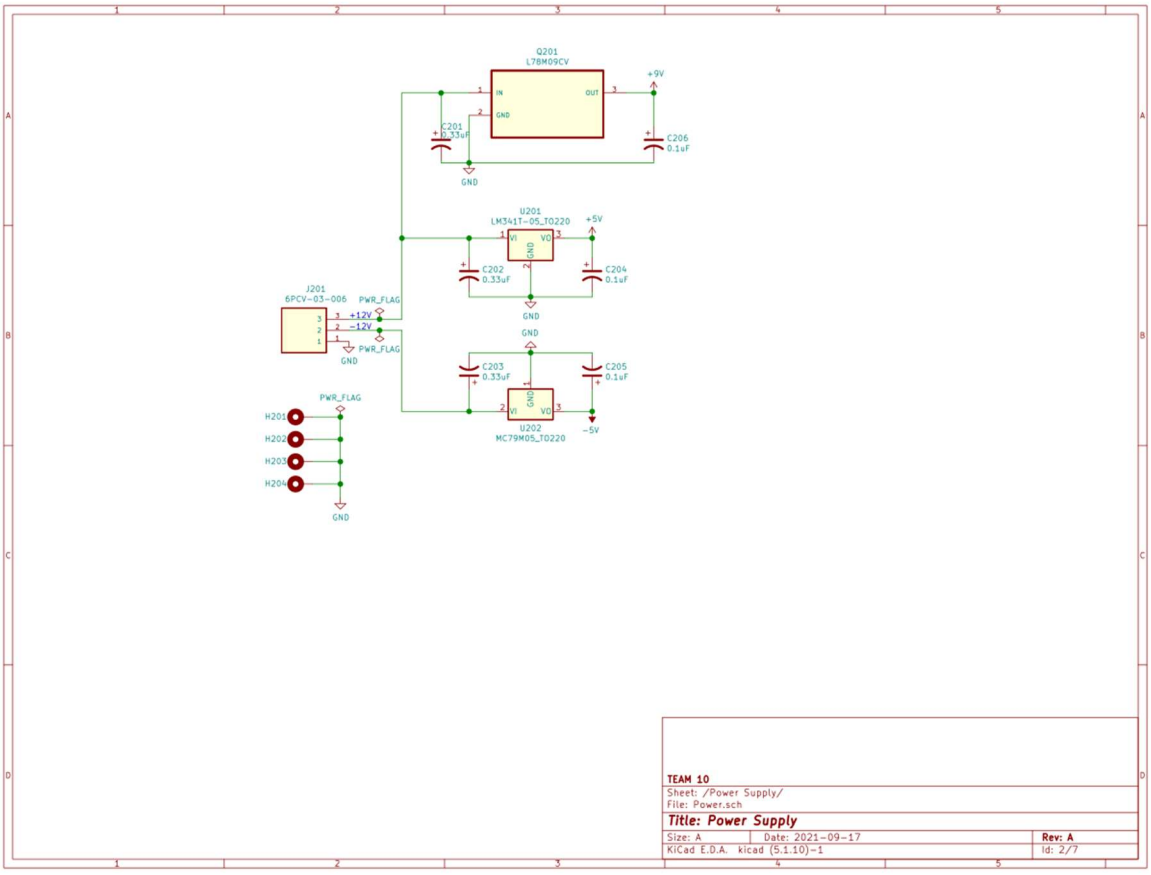

Figure 14 - Power Supply Schematic

The schematic diagram for the Power Supply is shown. The PCB accepts power from the ±12V DC supply through J201. The 12V DC is then passed through Q201 to output a 9V regulated voltage that is used to power up the Arduino Due and then in turn the LED matrix. Also, the 12V DC is also passed through U201 to output a 5V regulated voltage that is used to power up all op-amp configurations. The -12V DC is then passed through U202 to output a -5V regulated voltage. This is used to power up all op-amp configurations. H201 through H204 are the mounting holes that this Front-End PCB needs to mount into the enclosure.

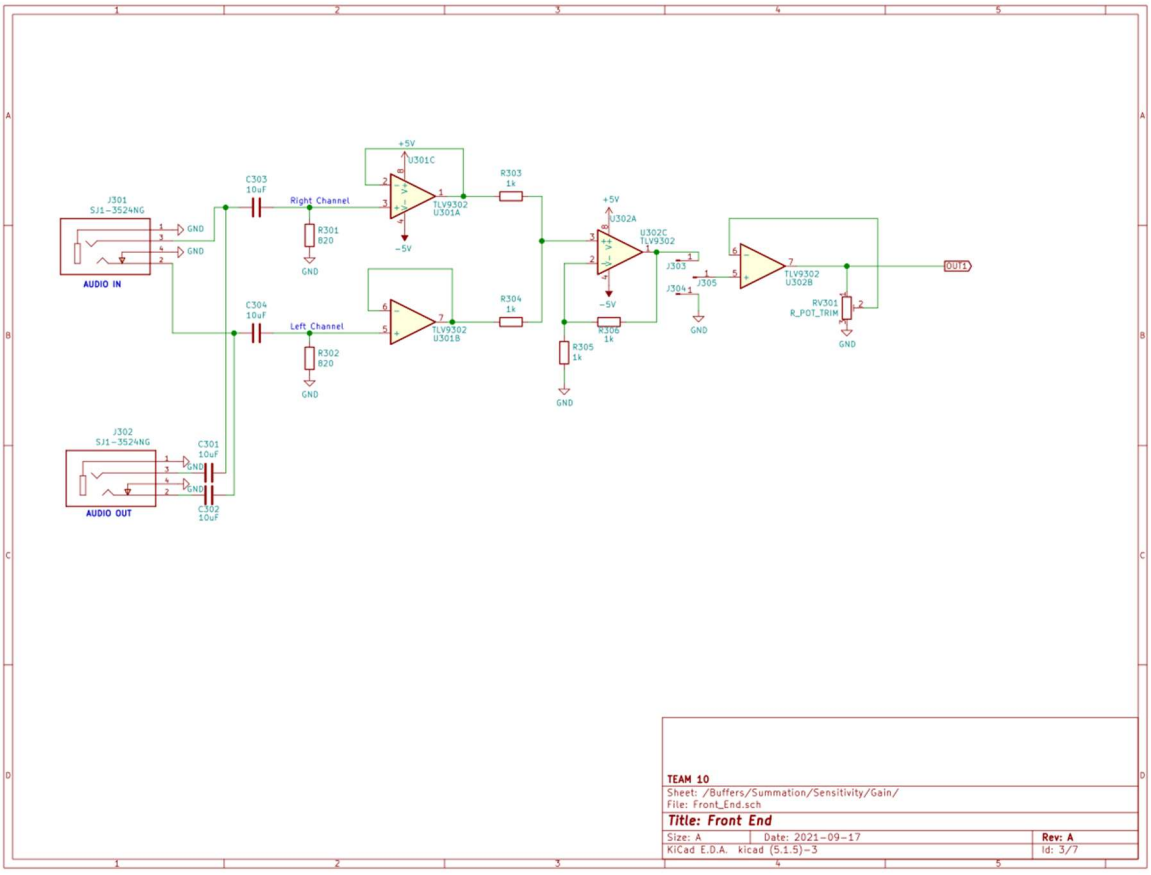

Figure 15 - Summation/Sensitivity/Gain Circuit

The schematic diagram for the Summation/Sensitivity/Gain Circuit is shown. J301 accepts an audio signal from any device with an AUX connection. The signal then goes through J302 unmodified to allow the user to connect a speaker to J302 to hear the audio signal. The signal is then split into two channels, a left and right channel. C303, C304, R301, and R302 remove any DC bias from both channels. Both channels go through U301, a voltage follower, then into U302A. U302A is a summation circuit that will sum both channels into a single channel. R305 and R306 give the summation circuit a gain of 2 to negate the one-half term created by R303 and R304. Its output then goes through J303, J305, and J304, which make up a log potentiometer that adjusts the relative loudness of the audio signal. The output of the log potentiometer then goes through U302B, a gain stage, which has its output routed to the seven active bandpass filters and a signal conditioning circuit.

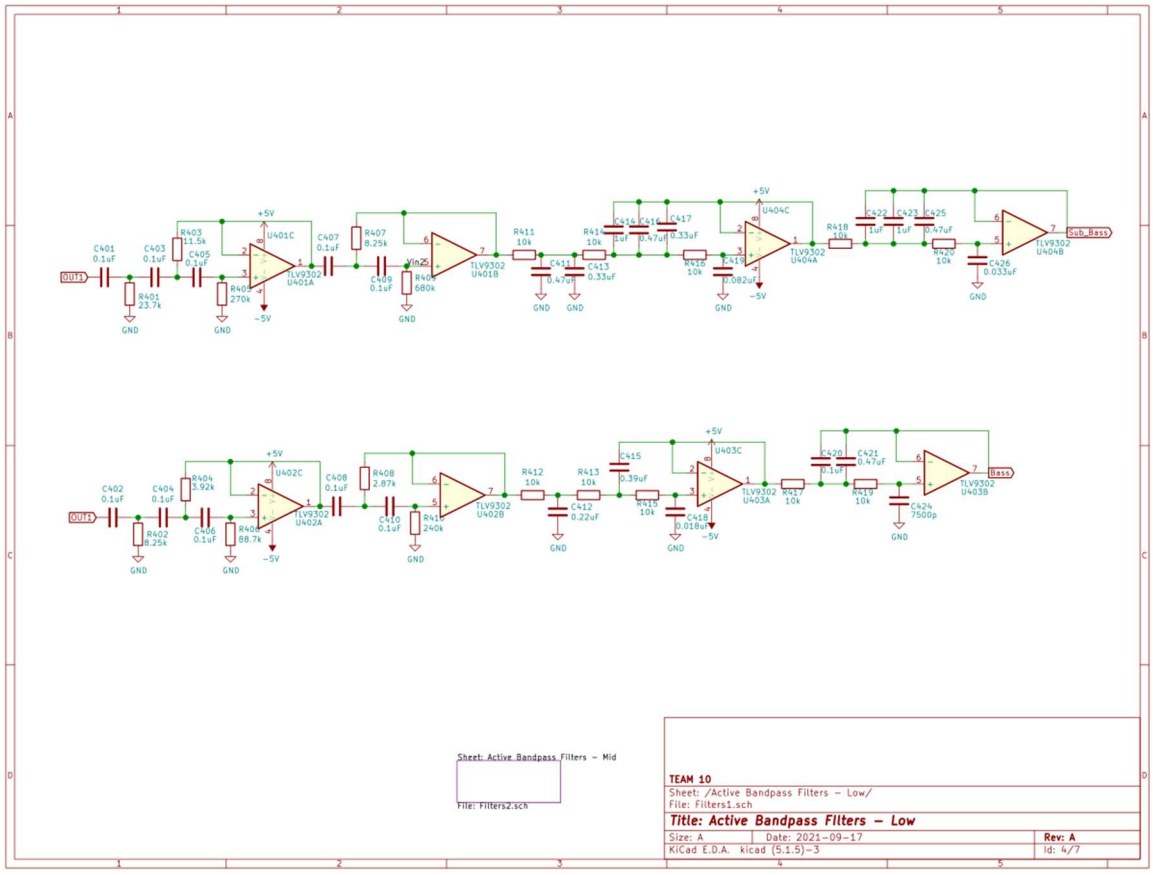

Figure 16 - Active Bandpass Filters Low Frequency Bins

The schematic diagram for the active bandpass filters for low frequency bins is shown. This is the core of the Audio Volume Unit Meter. These active bandpass filter configurations are responsible for creating the frequency bins that make up the sub-bass and bass bins. The sub-bass cut-off frequencies are 20Hz and 60Hz while the bass cut-off frequencies are 60Hz and 250Hz. The audio signal goes through a high-pass filter and then into a low-pass filter. C401 to U404B forms the sub-bass filter and C402 to U403 forms the bass filter.

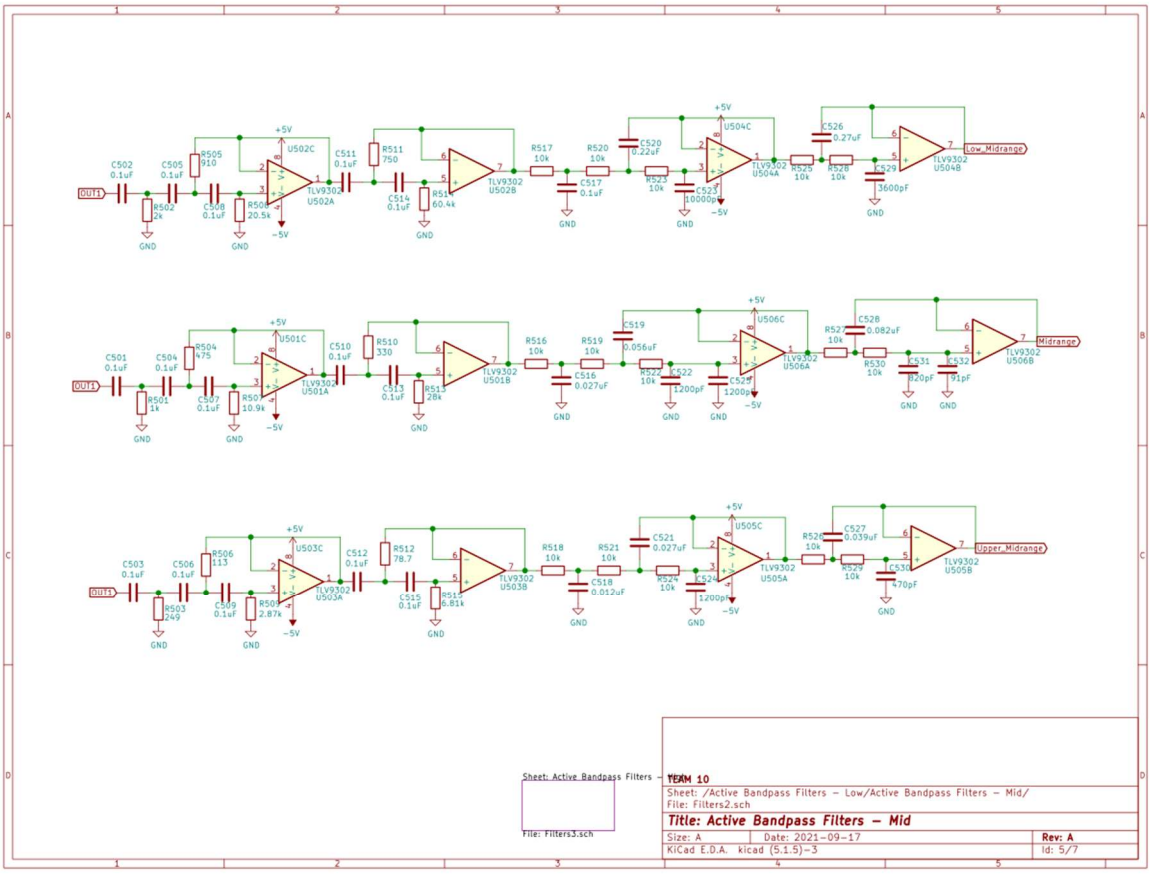

Figure 17 - Active Bandpass Filter Mid Frequency Bins

The schematic diagram for the active bandpass filters for the mid frequency bins is shown. These active bandpass filter configurations are responsible for creating the frequency bins that make up the low midrange, midrange, and upper midrange frequency bins. The low midrange cut-off frequencies are 250Hz and 500Hz, the midrange cut-off frequencies are 500Hz and 2kHz, and upper midrange cut-off frequencies are 2kHz and 4kHz. The audio signal goes through a high-pass filter and then into a low-pass filter. C502 to U504 forms the low midrange filter, C501 to U506 forms the midrange filter, and C503 to U505 forms the upper midrange.

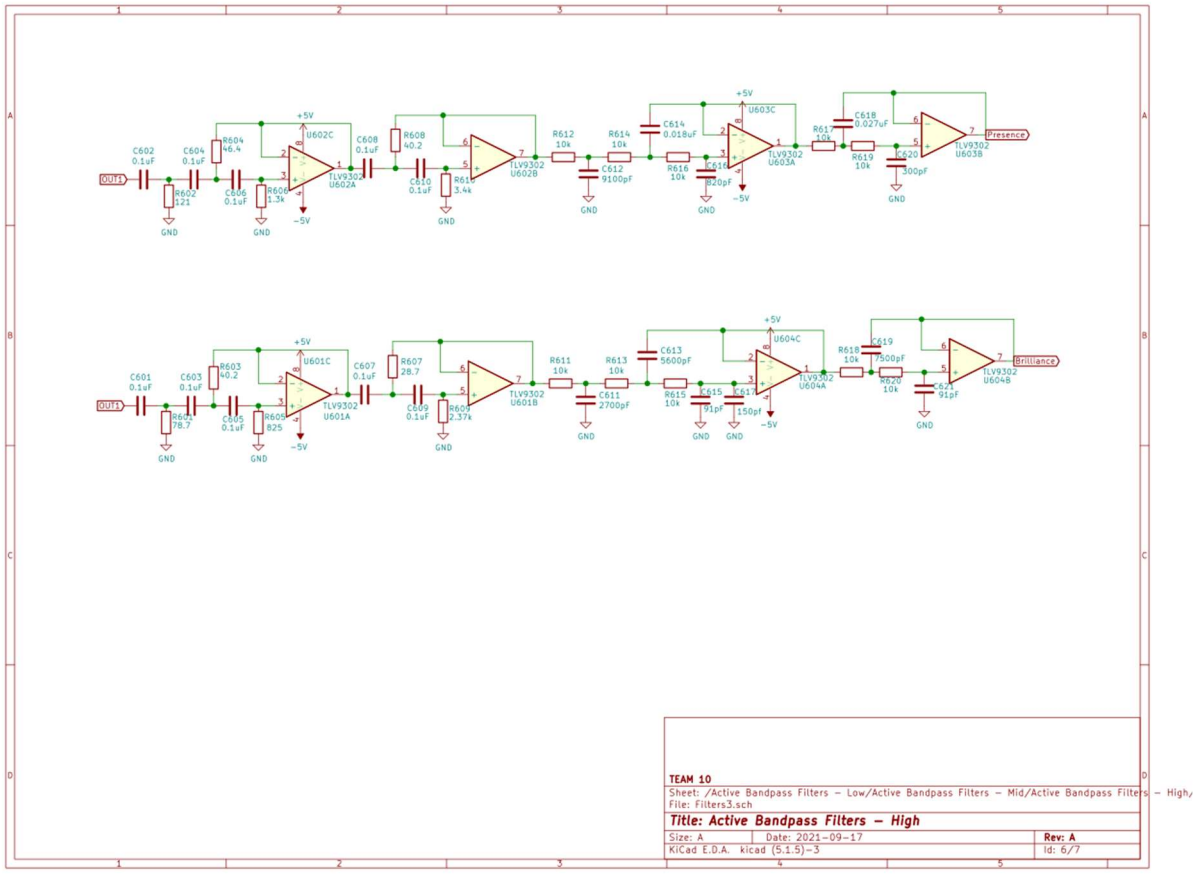

Figure 18 - Active Bandpass Filters High Frequency Bins

The schematic diagram for the active bandpass filters for the high frequency bins is shown. These active bandpass filter configurations are responsible for creating the frequency bins that make up the presence and brilliance frequency bins. The presence cut-off frequencies are 4kHz and 6kHz while the brilliance are 6kHz and 20kHz. The audio signal goes through a high-pass filter and then into a low-pass filter. C602 to U603 forms the presence and C601 to U503 forms the brilliance.

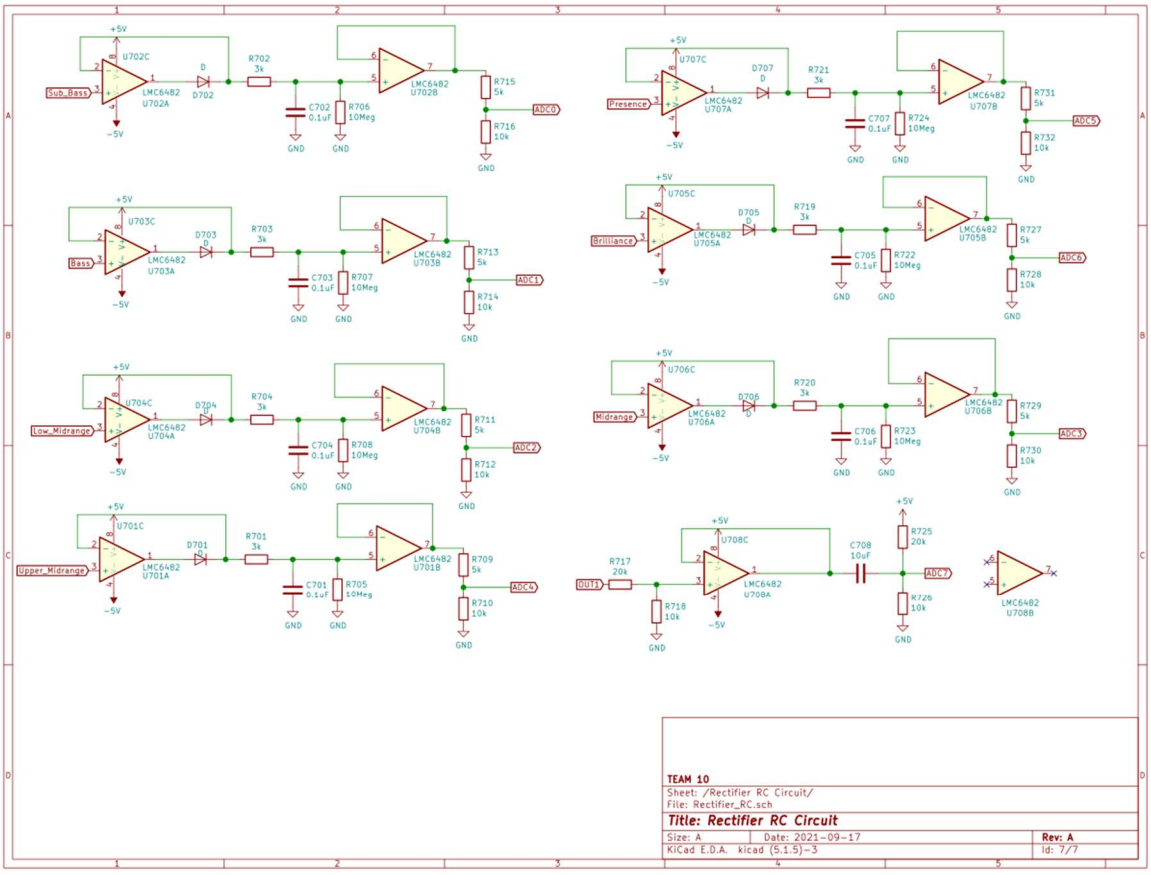

Figure 19 - Rectification/RC Circuit and Signal Conditioning Circuit

The schematic diagram for the rectification/RC circuit and signal conditional circuit is shown. These rectifier RC circuit accepts the frequency bins created from the active bandpass filters and turn the analog signal into a DC signal for the ADC to process. The signal conditioning circuit start at R717 and it is responsible for making the AC signal into a signal that the ADC can process between 3V and 0V.

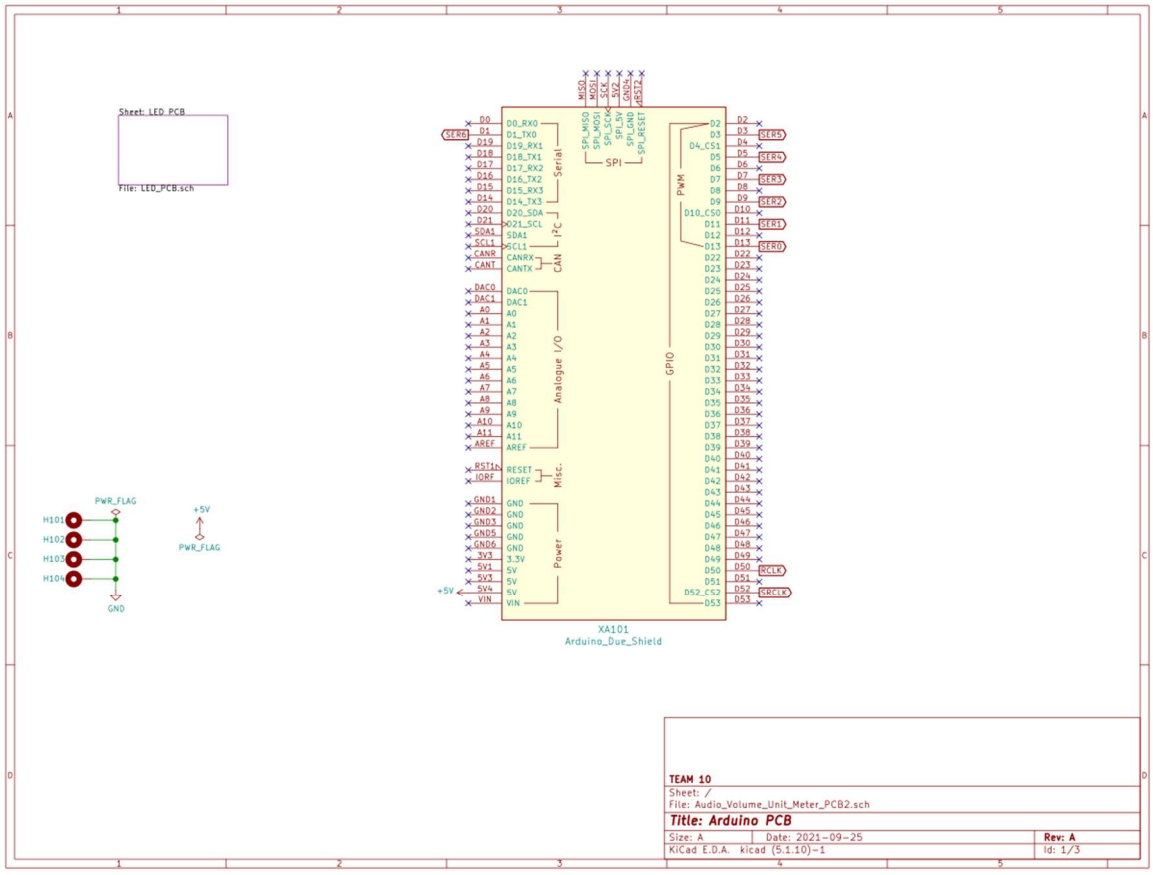

Figure 20 - Arduino Shield LED PCB

The schematic diagram for the Arduino shield part of the LED PCB is shown. The Arduino Due through the Arduino shield will control the shift register by using digital pins 52 and 50.

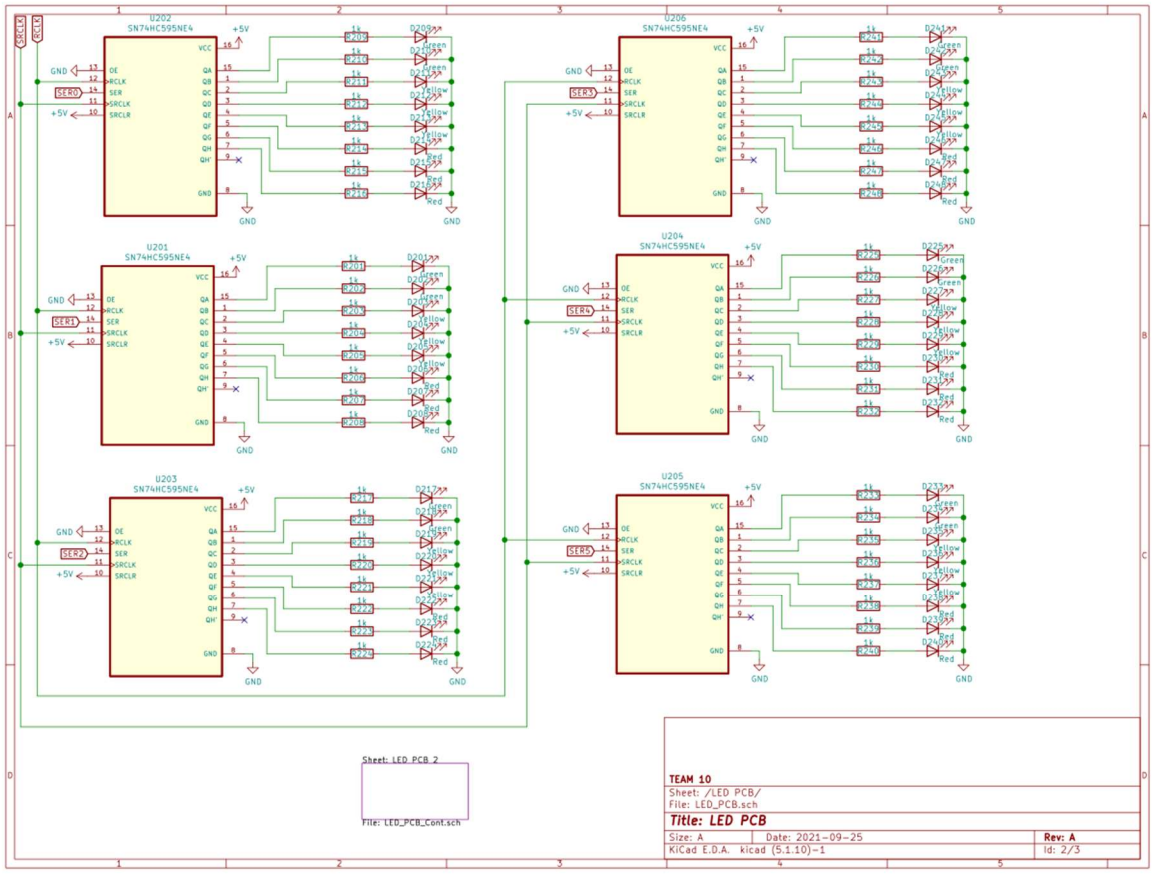

Figure 21 - LED PCB 1

The first part of the LED PCB is shown. The Arduino Due controls the shift registers and based on what it receives on the ADC inputs, a serial stream will be sent out to signal certain shift registers turn on and off the LEDs. A 5V digital signal gets sent out from a shift register to turn on the LED. Starting at the top, each shift register is connected to two green LEDs, three yellow LEDs, and then three red LEDs. Each LED connected to a resistor to draw current from. U202 represents the sub-bass frequencies, U201 represents the bass frequencies, U203 represents the low mid-range frequencies, U206 represents the mid-range frequencies, U204 represents the upper mid-range frequencies, and finally U205 represents the presence frequencies.

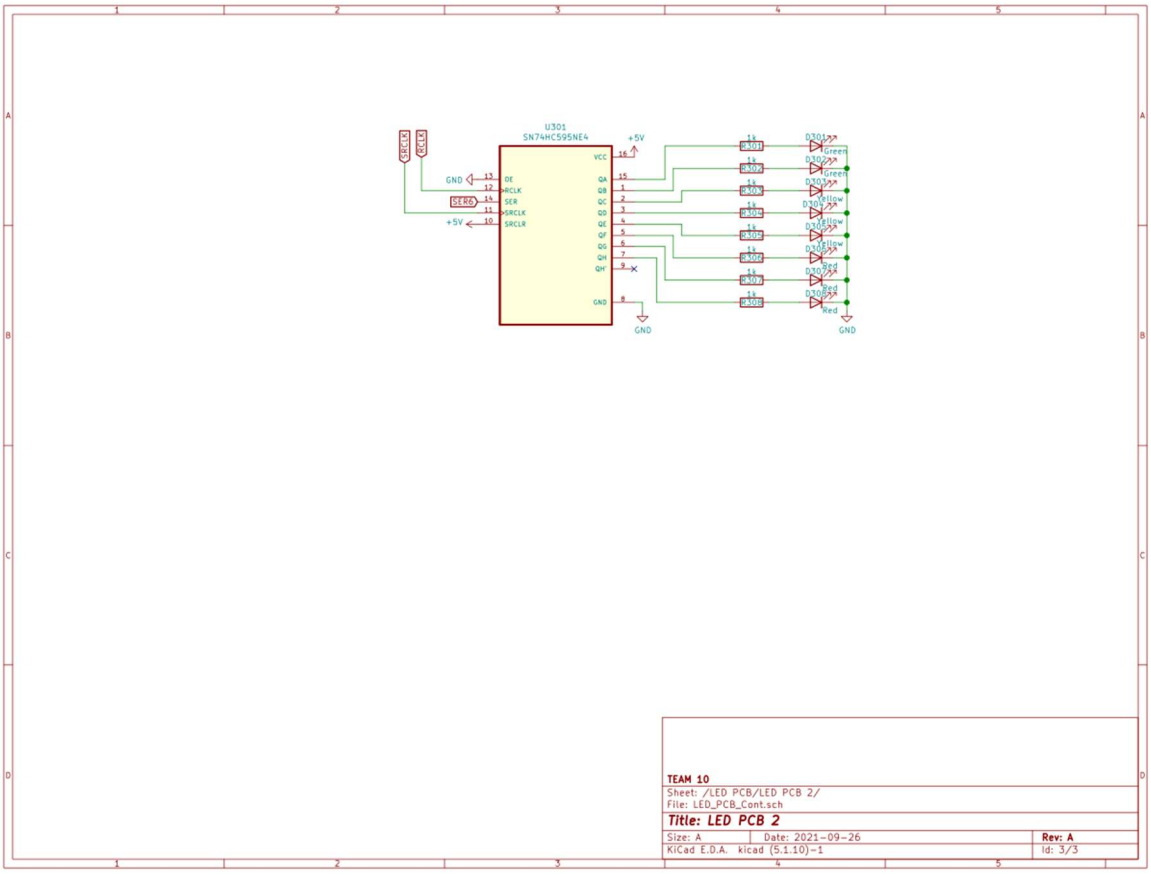

Figure 22 - LED PCB 2

The second part of the LED PCB is shown, and it is comprised of a shift register that represents the brilliance frequencies. This shift register operates the same way as the others that were previously described.

Printed Circuit Board

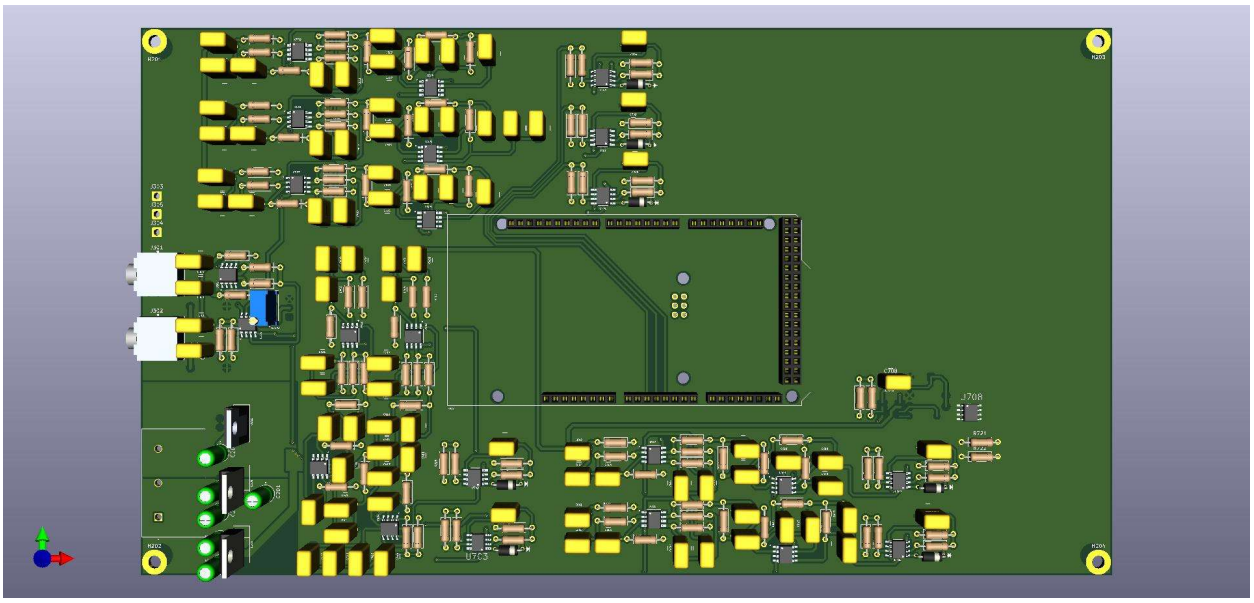

Figure 23 - Front End PCB Front View

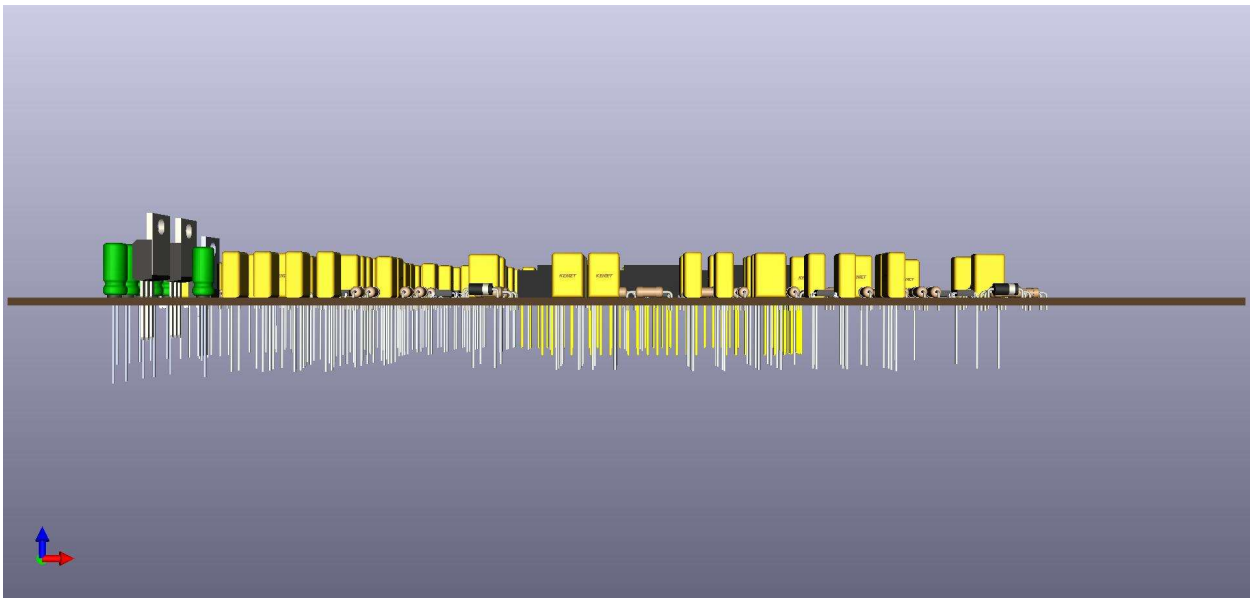

Figure 24 - Front End PCB Side View

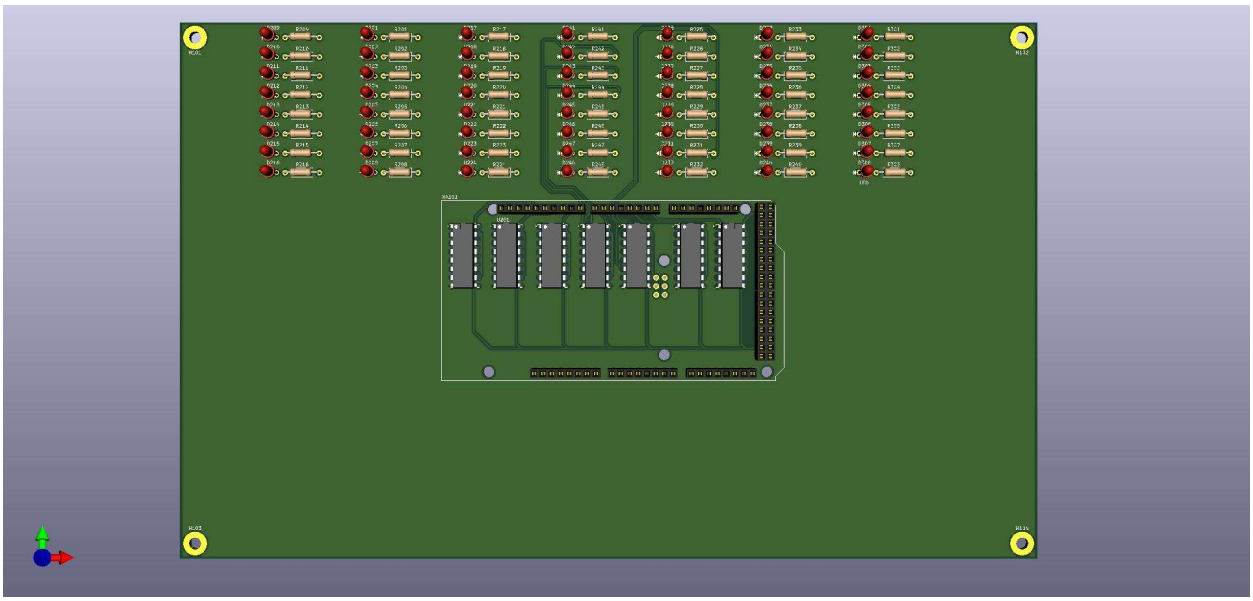

Figure 25 - PCB LED Front View

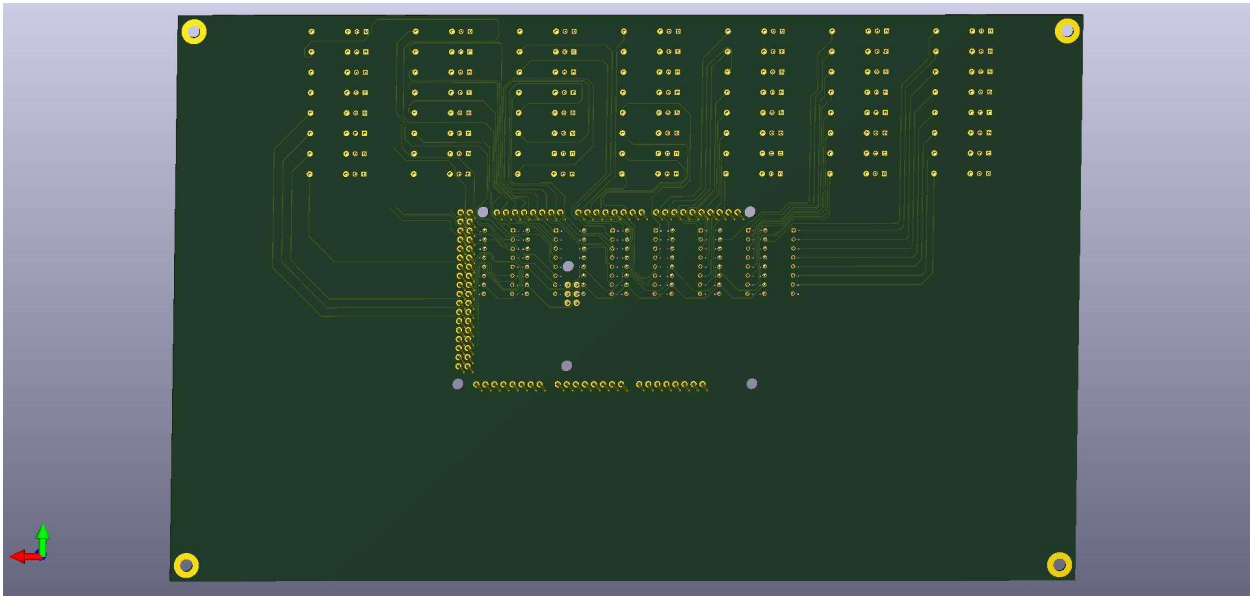

Figure 26 - PCB LED Back View

Enclosure Drawings

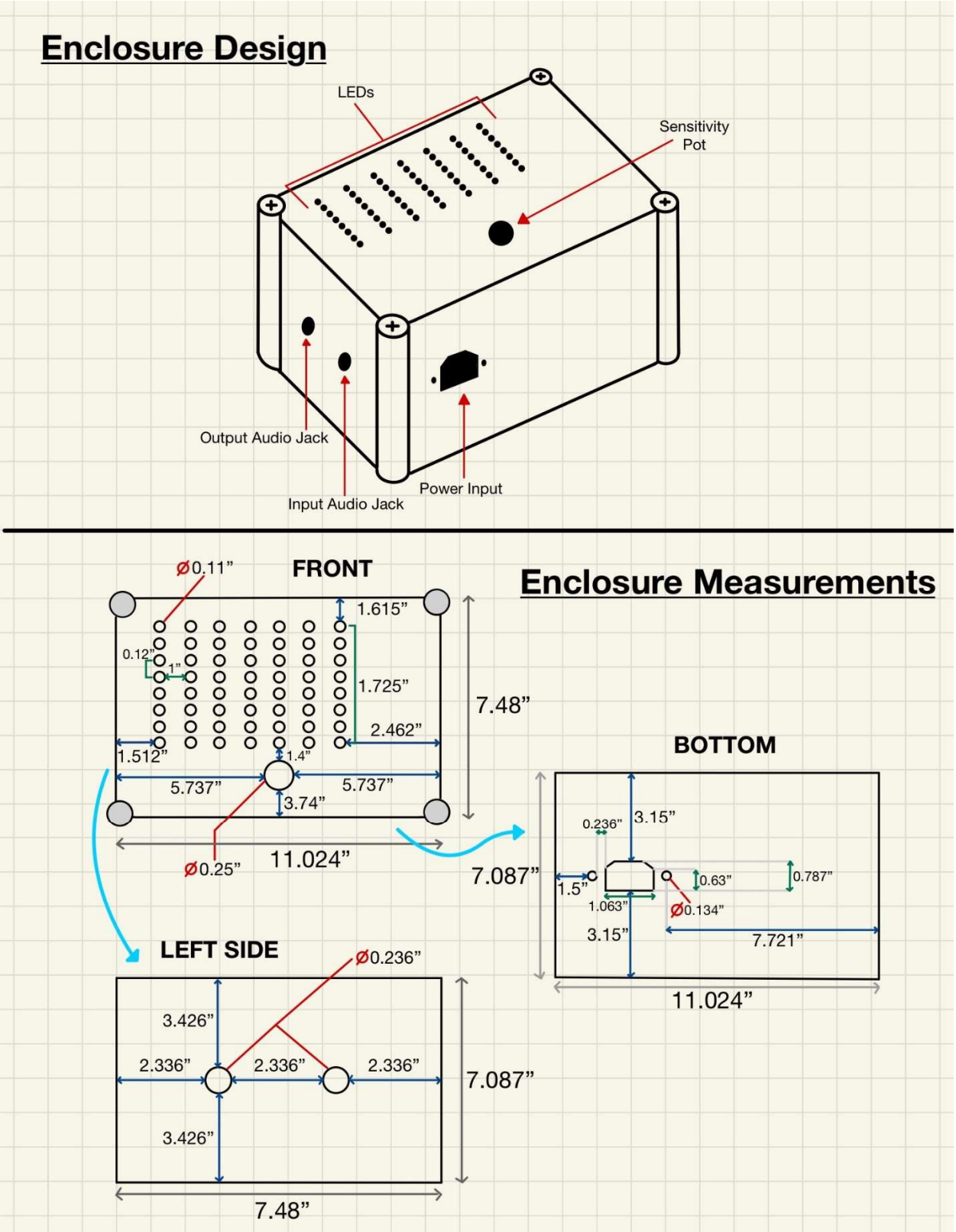

Figure 27 - Enclosure Diagram

For our enclosure, we are using a Boxco AGS-192818. This is a part we found in stock on Digi Key that meets our size and cost requirement. The image below labeled' Enclosure Design' shows an overview of the different modifications we will be making to the enclosure. We will drill out a hole for each of our 56 LEDs, as well as cut space for our sensitivity potentiometer, our two 3.5mm audio jacks, and our power input. The image below labeled 'Enclosure Measurements' shows the measurements for each of these modifications. Once received, we will bring our enclosure to the SDSU machine shop to accurately do the necessary drilling.

Wiring Diagram

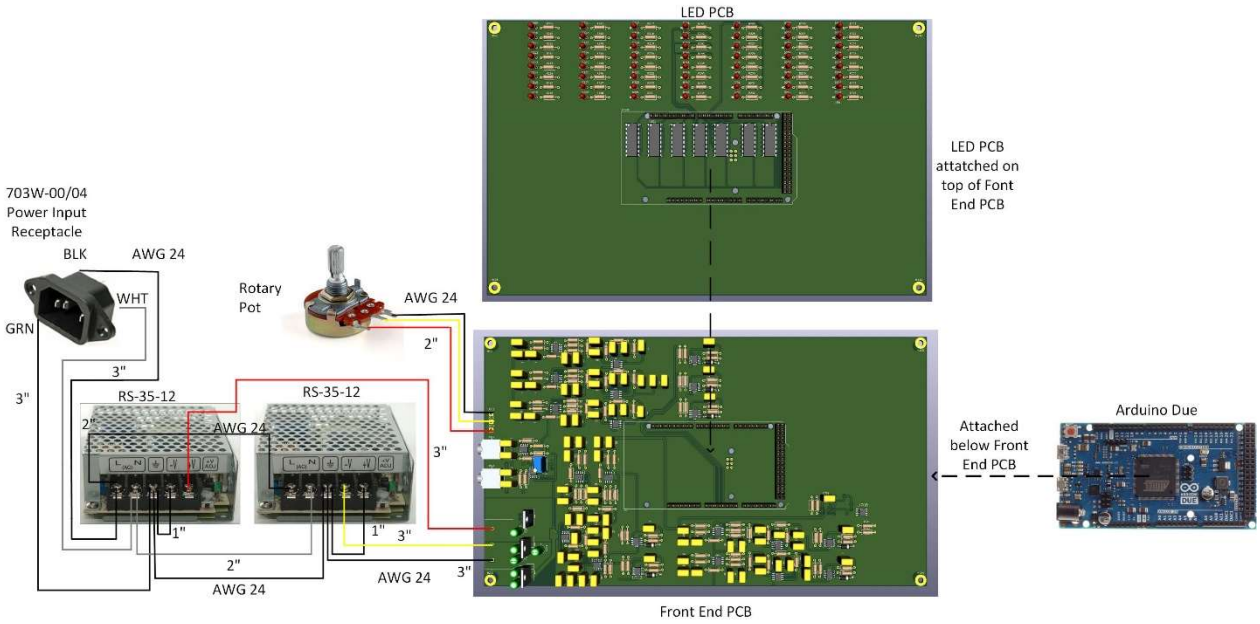

Figure 28 - Wiring Diagram

Hardware Test Plan

Test Name	Supported Specification	Procedure and Equipment	Expected Result
Arduino Shields Test Fit	Internal	Insert the Arduino Shields on top of the Arduino Due to form a stack. Visually verify that the Arduino Shields are properly connected. Remove the Arduino Shields that formed the stack for the remainder of the tests.	The Arduino Shields should fit snuggly into the pin headers of the Arduino and the Arduino Shields.
Power Supply	Internal	Connect the ±12V supply to power connector J201. Use a voltmeter to measure the output of the	The output of U201 should be 5V, the output of U202 should be -5V, and the output of Q201 should be 9V.

		voltage regulators: U201, U202, and Q201.	
Summation Circuit	Internal	Set function generator to generate a 1kHz sine wave at 1V peak-to-peak at the input of U301A and U301B. Using an oscilloscope, measure the output of U302A.	The output of U302A should be 2V peak-to-peak at 1 kHz.
Active Bandpass Filter Sub-Bass	Internal	Set function generator to generate a 20Hz sine wave at 1V peak-to-peak at the input of C401. Using an oscilloscope, measure the output of U404B. Repeat this at 60Hz.	The output of U404B must be around 0.707V peak-to-peak.
Active Bandpass Filter Bass	Internal	Set function generator to generate a 60Hz sine wave at 1V peak-to-peak at the input of C402. Using an oscilloscope, measure the output of U403B. Repeat this at 250Hz.	The output of U404B must be around 0.707V peak-to-peak.
Active Bandpass Filter Low-Midrange	Internal	Set function generator to generate a 250Hz sine wave at 1V peak-to-peak at the input of C502. Using an oscilloscope, measure the output of U504B. Repeat this at 500Hz.	The output of U404B must be around 0.707V peak-to-peak.
Active Bandpass Filter Midrange	Internal	Set function generator to generate a 500Hz sine wave at 1V peak-to-peak at the input of C501. Using an oscilloscope, measure the output of U506B. Repeat this at 2kHz.	The output of U404B must be around 0.707V peak-to-peak.
Active Bandpass Filter Upper Midrange	Internal	Set function generator to generate a 2kHz sine wave at 1V peak-to-peak at the input of C503. Using an oscilloscope, measure the output of U505B. Repeat this at 4kHz.	The output of U404B must be around 0.707V peak-to-peak.

Active Bandpass Filter Presence	Internal	Set function generator to generate a 4kHz sine wave at 1V peak-to-peak at the input of C602. Using an oscilloscope, measure the output of U603B. Repeat this at 6kHz.	The output of U404B must be around 0.707V peak-to-peak.
Active Bandpass Filter Brilliance	Internal	Set function generator to generate a 6kHz sine wave at 1V peak-to-peak at the input of C601. Using an oscilloscope, measure the output of U604B. Repeat this at 20kHz.	The output of U404B must be around 0.707V peak-to-peak.
Rectification/RC Circuit (All Circuits)	Internal	Set function generator to generate a 1kHz at 5V peak-to-peak at the input of U702C. Using an oscilloscope, measure the output of R716. Repeat this at 20Hz, 10kHz, and 20kHz	The output of R716 must be 3V DC.
Signal Conditioning Circuit	Internal	Set function generator to generate a 1kHz at 5V peak-to-peak at the input of R717. Using an oscilloscope, measure the output of R726. Repeat this at 20Hz, 10kHz, and 20kHz.	The output of R726 must be an ac signal with a peak voltage of 3.3V and a DC bias of 1.6V.
LED Matrix	Internal	Apply a 3.3V DC signal at the input of the ADCs and visually verify that all LEDs remain turn ON. Decrease the DC signal by 100mV until all LEDs turn OFF.	The LEDs should turn OFF one by one when DC sweep is performed.

Parts List

Index	Quantity	Part Number	Description	DigiKey/Mouser	Unit Price	External Price
1	5	399-13901-ND	CAP CER IUF 50V X7R RADIAL	399-13901-ND	$1.85	$9.25
2	5	399-14397-1-ND	CAP CER 0.22UF 25V X8R RADIAL	399-14397-1-ND	$0.7	$3.5
3	50	399-14398-1-ND	CAP CER 0.1UF 200V X8R RADIAL	399-14398-1-ND	$0.374	$18.70
4	5	399-14022-ND	CAP CER 0.056UF 5% 50V X7R RAD	399-14022-ND	$0.46	$2.30
5	5	399-C322C333J5R5TA-ND	CAP CER 0.033UF 50V X7R RADIAL	399-C322C333J5R5TA-ND	$0.46	$2.30
6	5	399-9828-ND	CAP CER 0.027UF 100V NP0 RADIAL	399-9828-ND	$1.99	$9.95
7	5	399-11996-ND	CAP CER 0.012UF 1KV C0G/NP0 RAD	399-11996-ND	$6.19	30.95$
8	5	399-9792-ND	CAP CER 10000PF 100V X7R RADIAL	399-9792-ND	$0.48	$2.40
9	5	399-13911-ND	CAP CER 5600PF 5% 100V C0G RAD	399-13911-ND	$0.74	$3.70
10	5	399-14077-ND	CAP CER 2700PF 5% 100V C0G RAD	399-14077-ND	$0.53	$2.65
11	5	399-9810-ND	CAP CER 470PF 100V NP0 RADIAL	399-9810-ND	$0.45	$2.25
12	5	399-14031-ND	CAP CER 820PF 5% 100V C0G RADIAL	399-14031-ND	$0.44	$2.20

13	5	399-4212-ND	CAP CER 150PF 200V NP0 RADIAL	399-4212-ND	$0.53	$2.65
14	5	399-13993-ND	CAP CER 0.33UF 5% 50V X7R RADIAL	399-13993-ND	$0.6	$3.00
15	2	SJ1-3524NG	CONN JACK STEREO 3.5MM R/A	SJ1-3524NG	$0.81	$1.62
16	30	TLLR4400-ND	LED RED DIFFUSED 3MM T/H	TLLR4400-ND	$0.398	$11.93
17	30	TLLY4400-ND	LED YELLOW DIFFUSED 3MM T/H	TLLY4400-ND	$0.339	$10.17
18	20	TLLG4400	LED GREEN DIFFUSED 3MM T/H	TLLG4400	$0.358	$7.16
19	10	296-36142-5-ND	IC SHIFT REGISTER 8BIT 16-DIP	296-36142-5-ND	$0.647	$6.47
20	20	296-53513-1-ND	IC OPAMP GP 2 CIRCUIT 8SOIC	296-53513-1-ND	$0.866	$17.32
21	10	LMC6482IMXCT-ND	IC OPAMP GP 2 CIRCUIT 8SOIC	LMC6482IMXCT-ND	$2.57	$25.70
22	10	1N4148-T26ACT-ND	DIODE GEN PURP 100V 200MA DO35	1N4148-T26ACT-ND	$0.071	40.71
23	5	C330C474J5R5TA	CAP 50V 0.47uF X7R 5% LS	C330C474J5R5TA	$1.01	$5.01
24	5	C330C394J5R5TA	CAP 50V 0.39uF X7R 5% LS	C330C394J5R5TA	$1.09	$5.45
25	5	C330C274J5R5HA	CAP 50V 0.27uF X7R 5% LS	C330C274J5R5HA	$1.09	$5.45
26	5	C336C823J2G5TA	CAP 200V 0.082uF C0G 5%	C336C823J2G5TA	$1.88	$9.40
27	5	C322C393J5R5TA	CAP 50V 0.039uF X7R 5% L	C322C393J5R5TA	$0.52	$2.60

28	5	C330C183J1G5TA	CAP 100V 0.018uF C0G 5%	C330C183J1G5TA	$1.89	$9.45
29	5	C330C912JAG5TA	CAP 250V 9100pF C0G 5% L	C330C912JAG5TA	$0.75	$3.75
30	5	C330C752JAG5TA	CAP 250V 7500pF C0G 5% L	C330C752JAG5TA	$0.75	$3.75
31	5	C318C362J5G5TA	CAP 50V 3600pF C0G 5% LS	C318C362J5G5TA	$0.45	$2.25
32	5	C317C910JAG5TA	CAP 250V 91pF C0G 5% LS	C317C910JAG5TA	$0.45	$2.25
33	5	C322C301JCG5TA	CAP 500V 300pF C0G 5% LS	C322C301JCG5TA	$1.90	$9.50
34	5	C322C122J5G5TA	CAP 50V 1200pF C0G 5% LS	C322C122J5G5TA	$0.53	$2.65
35	2	LM341T-5.0/NOPB	IC REG LINEAR 5V 500MA TO220-3	LM341T-5.0/NOPB	1.69	$3.38
36	2	L78M09CV	IC REG LINEAR 9V 500MA TO220AB	L78M09CV	$0.73	$1.46
37	2	RS-35-12	AC/DC CONVERTER 12V 36W	RS-35-12	$16.08	$32.16
38	1	3296W-1-103RLF	TRIMMER 10K OHM 0.5W PC PIN TOP	3296W-1-103RLF	$3.74	$3.74
39	1	PDB241-GTR01-504A2	POT 500K OHM 1/4W CARBON LOG	PDB241-GTR01-504A2	$3.81	$3.81
40	2	6PCV-03-006	CONN BARRIER STRIP 3CIRC 0.375"	6PCV-03-006	$2.23	$4.46
41	2	MC79M05CTG	IC REG LINEAR -5V 500MA TO220AB	MC79M05CTG	$0.8	$1.60
42	1	BC-AGS-192818	Box Plastic, ABS Light	BC-AGS-192818	$37.05	$37.05

			Grey Lift-Off Screw Cover11.024" Lx7.480"W(280.00mmx190.00 mm) x7.087"			
43	3	920-0086-01	Jumber wires Qty 6, Eight Pin STK Hdrs for Arduino	920-0086-01	$5.00	$15.00
44	1	920-0087-01	Jumper Wires Qty 6, Ten Pin Stkbl Headers for Arduino	920-0087-01	$5.00	$5.00
45	5	UVR2AR33MDD	CAP ALUM 0.33UF 20% 100V RADIAL	UVR2AR33MDD	$0.29	$1.45
46	5	UVR2A0R1MDD	CAP ALUM 0.1UF 20% 100V RADIAL	UVR2A0R1MDD	$0.27	$1.35
47	5	C322C106K3R5TA	CAP CER 10UF 25V X7R RADIAL	C322C106K3R5TA	$0.86	$4.30