Firmware Updates

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Master TTC Emulator

How it works:

if enabled, masks TTC signals from TIM, and start cycling:

1) (optional): sends ECR + waits 2 ms
2) sends BCR
3) sends triggers according to Trigger Pattern (2496 BCs -> to be changed to ~3552 BCs)
4) stops OR goes to step 2

TO DO: enable possibility of looping N times, with N fixed value

Master TTC Emulator registers

Two new registers:

1) fake_trig_ctrl (0x60):
- **bit 31: enable mechanism (loop starts on rising_edge)**
- **bit 30: when 0 → one loop then stops**
  when 1 → continuous loop
- **bit 29: when 1 → sends ECR at the beginning**
- **bits [6 – 0] : trigger pattern address**

2) fake_trig_val (0x61):
- **bits [31 – 0]: trigger pattern value**

How to set trigger pattern

Note: trigger not set  **bit = 1**

trigger set **bit = 0**

E.g. set trigger at BC number K:

trigger pattern address = (unsigned int) (K/32)
trigger pattern value = trigger pattern value and not (1 << (unsigned int)(K%32))

NOTE: the trigger pattern is updated after every write operation in the fake_trig_val register

TESTS

Test 1: 27 consecutive triggers (6 BC pause after each other) + long pause (>10000 BC) + 20 “slow” triggers

Simulation: because of MCC emulator, some triggers are lost (skipped trigger information is not propagated)

Data taking with BOC emulator: same behavior as simulation

Data taking with detector (no occupancy): MCC sends back the first 27 triggers (including skipped) and then is frozen till next ECR

TESTS

Test 2: 11 consecutive triggers (6 BC pause after each other) + long pause (>10000 BC) + 20 “slow” triggers

Data taking with detector (no occupancy): 21 triggers back as expected

Test 3: 22 consecutive triggers (6 BC pause after each other) + long pause (>10000 BC) + 20 “slow” triggers

Data taking with detector (no occupancy): 42 triggers back (including skipped) as expected

TESTS

Test 4: 27 consecutive triggers (6 BC pause after each other) + short pause (2000 Bcs) + 1 trigger + long pause (>10000 BC) + 20 “slow” triggers

Data taking with detector (no occupancy): 28 trigger backs (MCC “stucked” till next ECR)

TESTS

Test 5: 27 consecutive triggers (6 BC pause after each other) + short pause (2000 Bcs) + long pause (>10000 BC) + 20 “slow” triggers (same as test 1) but with SMART L1ID Mechanism activated (threshold = 15 pending triggers)

Data taking with detector (no occupancy): 47 trigger backs (including skipped) as expected

Notes

The MCC always has the same response with the same trigger pattern.

Hard to predict what trigger pattern will “freeze” the MCC.

However, test conditions very harsh, far from ATLAS data-taking. Test needed with realistic Complex dead time (15/3600)