Observation of ROD histogrammer issues on noise mask 2/11/2021

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To be tested/validated at CERN

- Recently, we changed procedure to mask noisy pixels in the detector … A) ➔ B)

A) Recording raw data from a standard detector data taking with

HV ON and Preamps On without beam in the machine

➔ starting from the raw data, produce the occupancy histos for each FE

➔ find the pixels in each FE that have a occ > noise level(~10^{-6})

➔produce and apply the mask in the module configuration tag!

B) Start the Histogrammer (Sampling mode) in the ROD Slave

Start the data taking (no need for recording, higher trigger rate achievable)

Stop data taking

Stop the Histogrammer (Readout mode)

➔ find in the occupancy histos the pixels that have a occ > noise level (~10^{-6})

➔ produce and apply the mask in the module configuration tag!

To be tested/validated at CERN

- To assess if a pixel is noisy or not (occupancy > 10^{-6}), we want to take 10^{7} events and mark as ***noisy*** all the pixels that show ***>=10 hits*** in the occupancy histos.

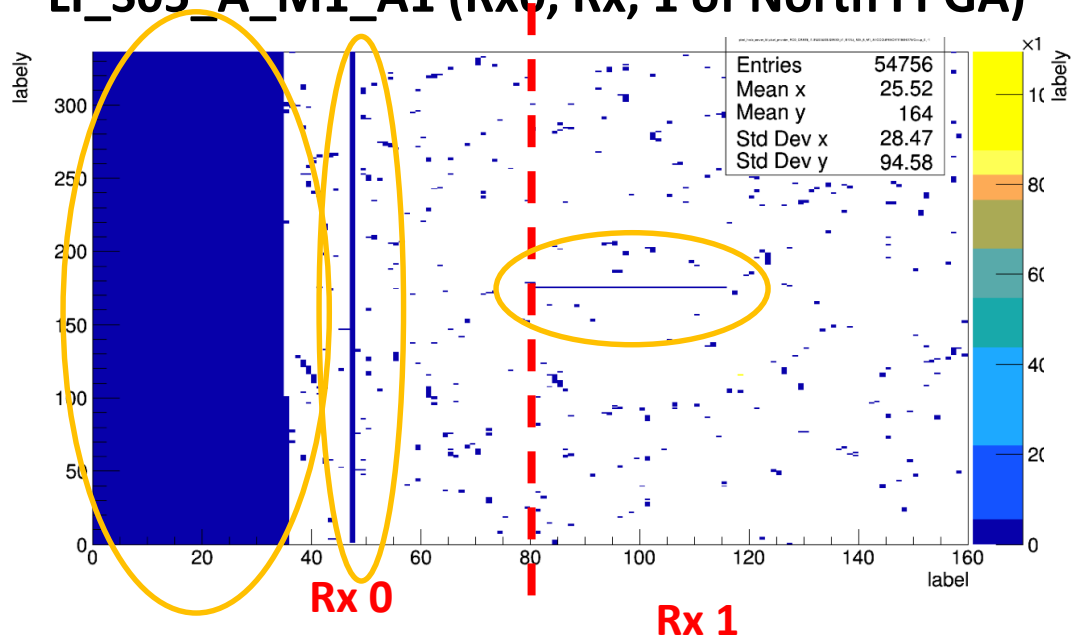
..From the E-logs…

- IBL Run 400832 ~ **18 million events at 3 kHz to 4 kHz trigger rate**
  - Pattern observed on many FEs with about 120-130 hits in those patterns
  - Noise mask set to 150/18M ~ $1E^{-5}$
- IBL Run 400850 ~ **10 million events at trigger rate of 14.5 kHz**
  - Pattern (although slightly different) also seen --> seems to happen in same modules
- Stops us from going below 1E-5 in the noise mask

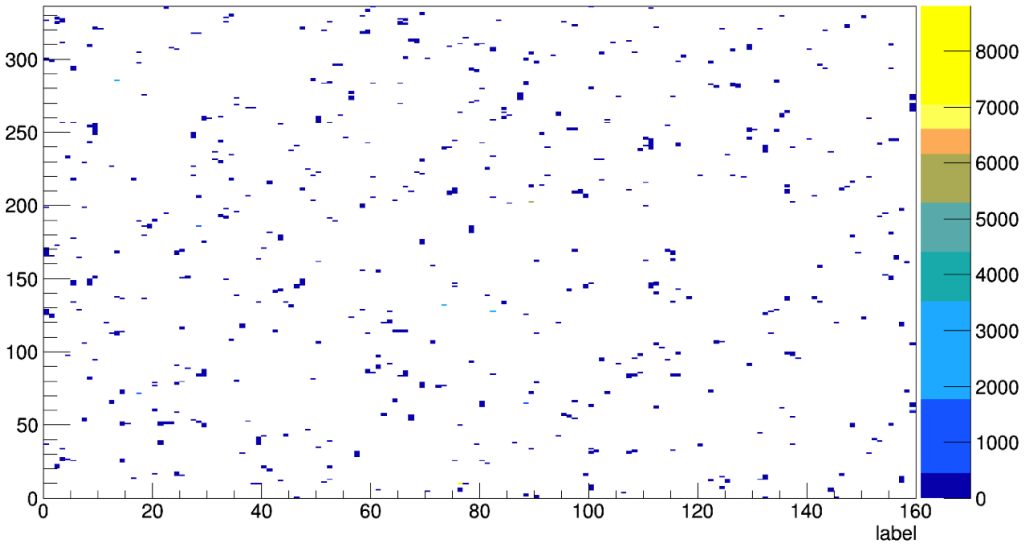
➔ It seemed ok up to 5 millions with 13 kHz.

IBL Run 400832

LI_S05_A_M1_A1 (Rx0, Rx, 1 of North FPGA)

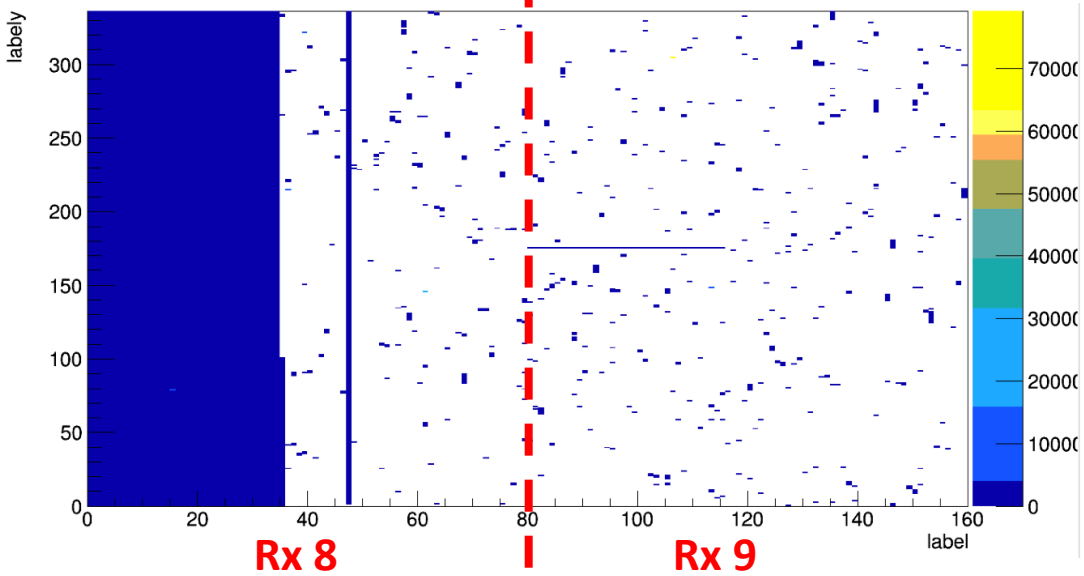


LI_S05_A_M1_M2 ..(Rx 2,..7 of North FPGA



~ 18 million events at 3- 4 kHz trigger rate

LI_S05_A_M3_A5 (Rx8, Rx 9 of North FPGA)

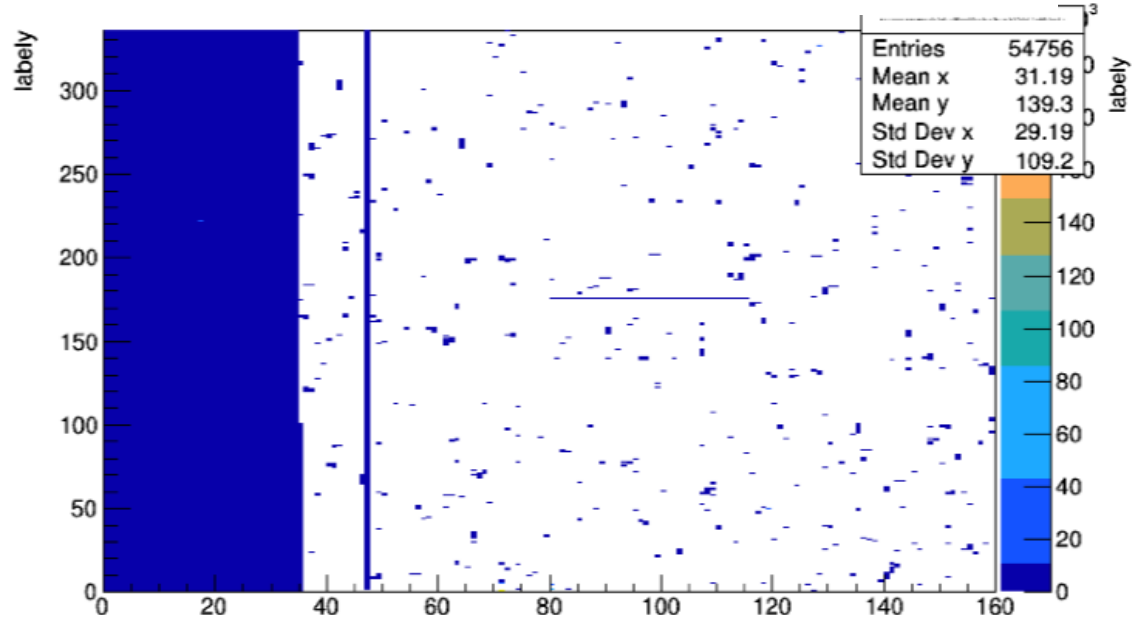


Pattern seen in RX channels 0,1 and 8,9 for IBL Stave 5 , A side (ROD FPGA North).

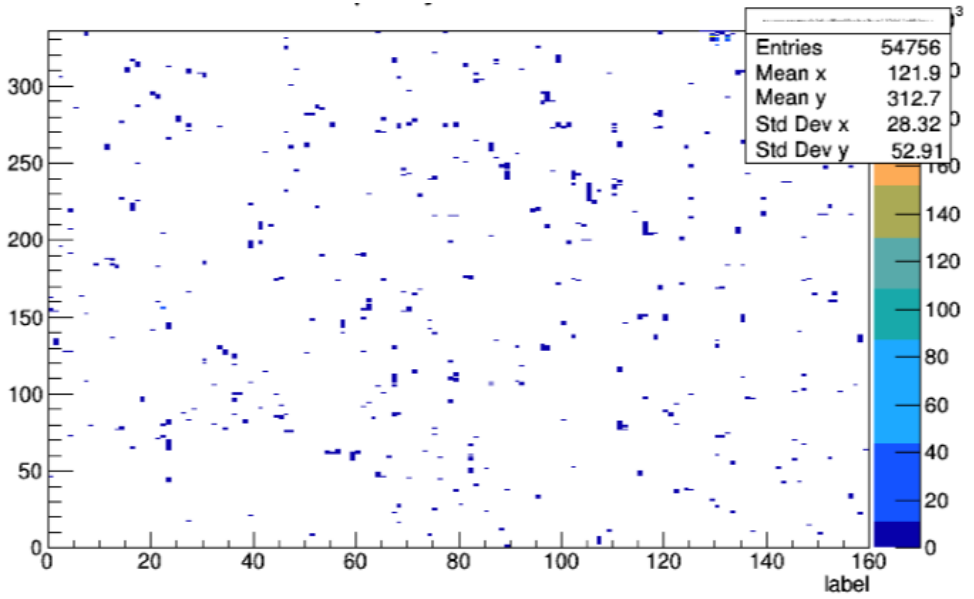
- 3 macro regions corrupted

What about other stave side (ROD FPGA)?

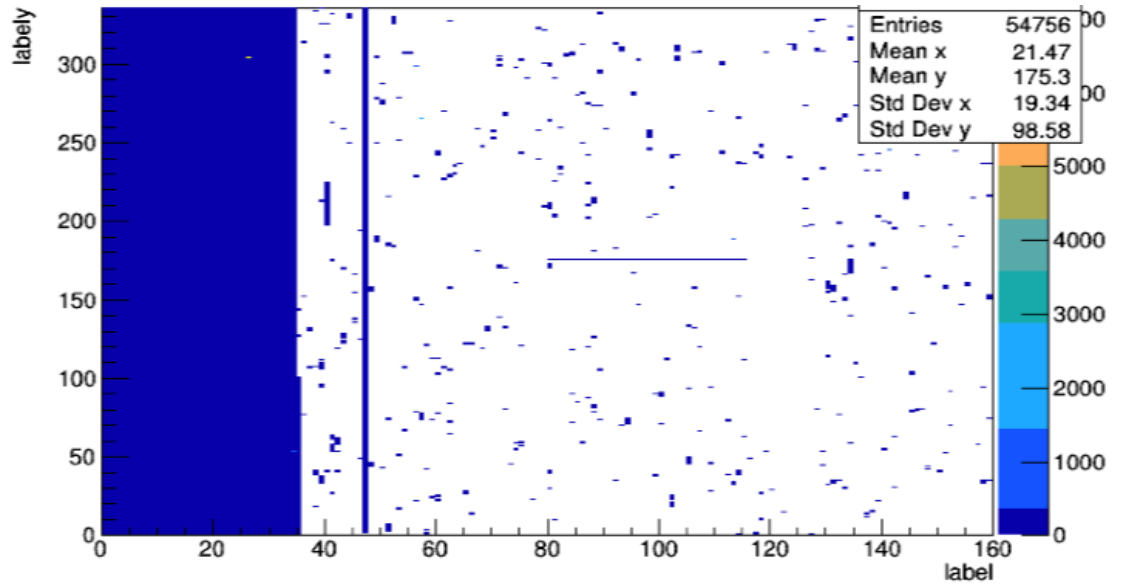
LI_S05_C_M4_C8 (Rx0, Rx, 1 of South FPGA)



LI_S05_C_M4, M3 (Rx 2,….7 South FPGA



LI_S05_C_M2_C4 (Rx8, Rx 9 of South FPGA)



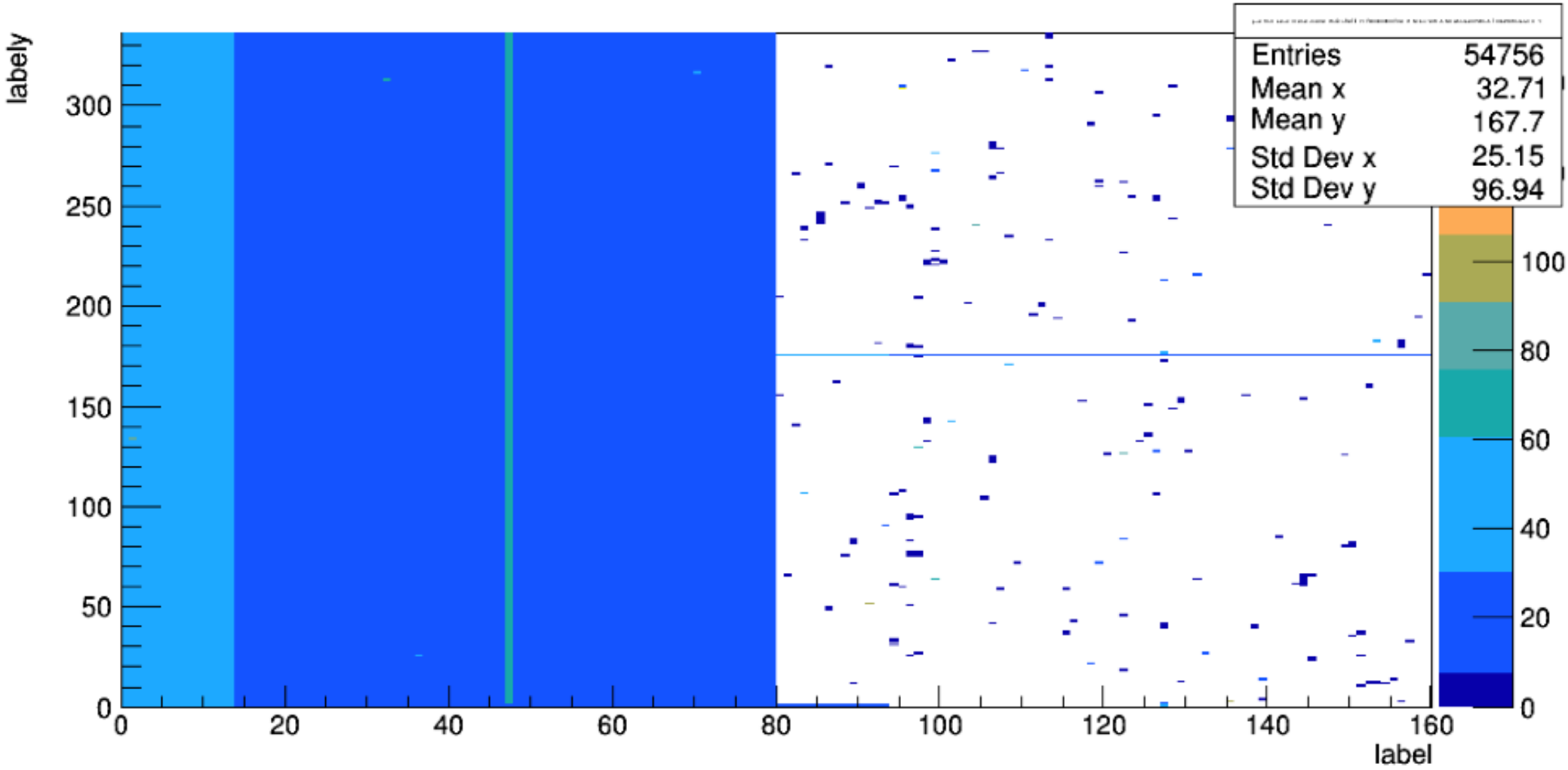
Same pattern observed in the same RX channels, in the south FPGA!

➔ This correspond to the begin of the memory mapping for the **Histogrammer 0** and **Histogrammer 1** units in the FPGA

➔ **Same issue present in other Staves/RODs**

What about Run IBL Run 400850

~ 10 million events at trigger rate of 14.5 kHz



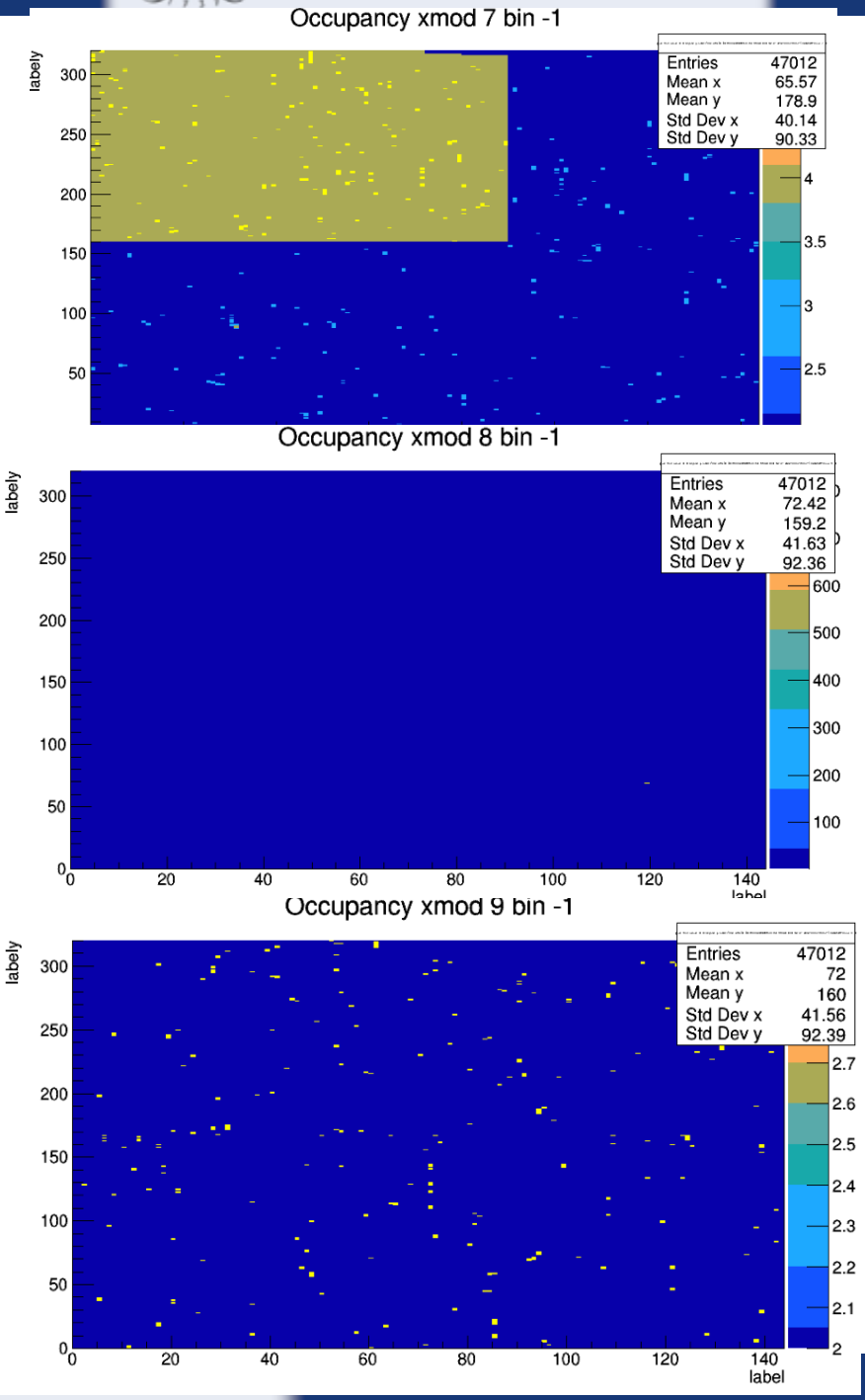
Same problem, same granularity, slightly different pattern indeed.

What about Pixel noise RUNs?

- Pixel Run 404598 **~ 10 million events at 11 kHz**
  - 6778 masked pixels from 1667 modules
  - Pattern seen in histograms, rerunning - but number of masked pixels seems reasonable
- Pixel Run 404613 **~ 10 million events at 11 kHz**

  6560 masked pixels from 1667 modules
  - Pattern still seem sometimes, but not at high enough an offset to add pixels as far as we can tel

Pixel Run 404598



~ 10 million events at 11 kHz

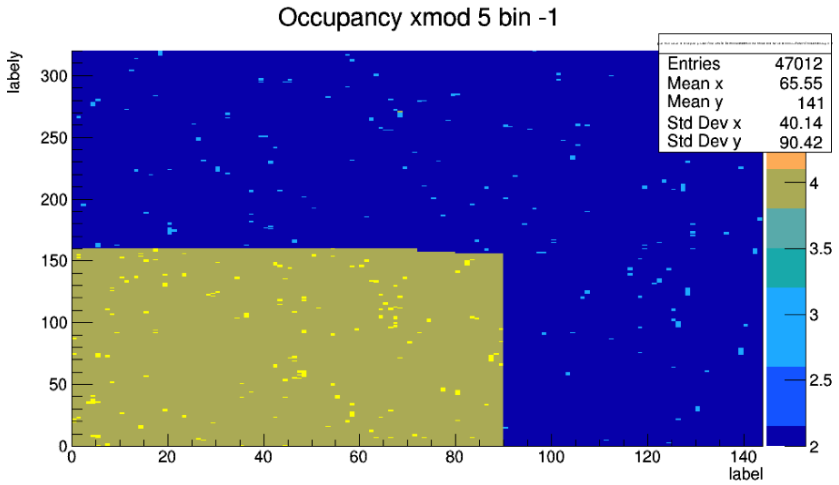
North FPGA

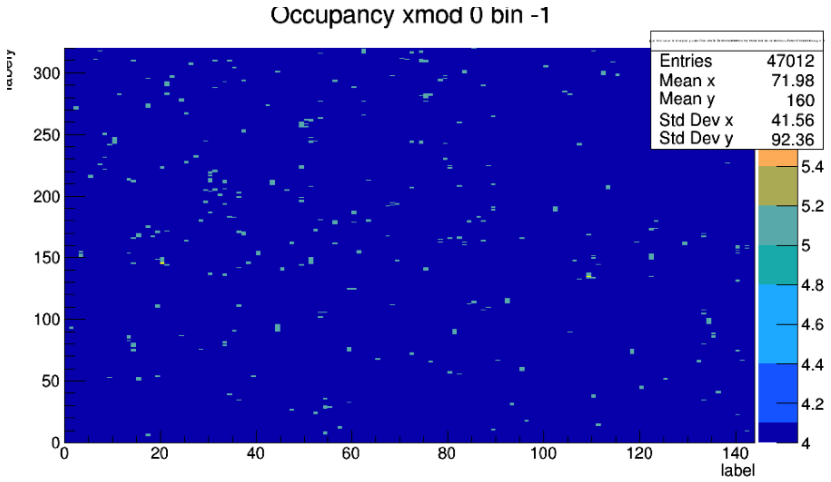
- L0_B04_S2_A7_M1A Rx13
- L0_B04_S2_A7_M2A Rx12
- ……..
- ……..
- …….
- L0_B04_S2_A7_M6A Rx8

Pattern present in the entire PP0,
several modules (Rx) involved

➔ It seems an overall baseline of few hits is artificially created everywhere

~ 10 million events at 11 kHz





South FPGA

L0_B04_S2_C6_M1C Rx9

L0_B04_S2_C6_M6C Rx13

Pattern present in the entire PP0,
several modules (Rx) involved

➔ It seems an overall baseline of few hits is artificially created everywhere

Summary

- Issue with memory transfer/mapping in the Histogrammer observed
  - No debugging since many years…so time needed to recreate “expertise”
  - Custom fw with Chipscope needed….should be reproducible also in SR1 or PIT with emulator.

  ➔ Issue to be add to the validation tests list via CI.
- JIRA ticket created
- https://gitlab.cern.ch/atlas-pixel/daq/pixelrod_firmware/RodSlave/-/issues/8
- Issue to be solved before next detector turn on (Feb2022)