“Smart L1A forwarding” finalization and validation tests

During Run 3 (2022-2024), the LHC will deliver high instantaneous luminosity (L ~$2 \cdot 10^{34} cm^{-2}\ s^{-1}$) and pile-up (μ ~55) for long periods of time (luminosity-levelling should last up to ~12 hours). High Level1 (L1A) trigger rates are foreseen during these periods (up to ~100 kHz).

Therefore, the Pixel/IBL Front-End chips (FE) are expected to face very challenging conditions, at their performance limit. FE processing high number of hits do not always reply in time to the DAQ chain which continuously sends L1A triggers to the modules. As a result, some triggers might get skipped, inducing a desynchronization (or misalignment) in the data stream if the number of skipped triggers is not accounted for correctly in the FE and Read-Out Driver (ROD).

In general, such information is sent by the Pixel Micro Controller Chip (MCC) to the ROD with a specific “skipped triggers” counter in the data stream. However, discrepancies in this quantity have been observed during Run 2 (2015-2018). The desynchronization induced by a wrong skipped trigger counter would last until next ATLAS wide re-synchronization signal (the Event-Counter Reset signal, or ECR in jargon) which happens every 5 seconds (leading to ~10^3 events desynchronized each time).

The ATLAS Bologna group has in hand a full simulation of the MCC and is investigating the reasons for which a wrong skipped trigger counter value is occasionally reported by the MCC in the data stream.

The candidate of this project should first help to characterize the occurrence of such discrepancies in the skipped trigger counter (for which trigger pattern, FE occupancy, latency and read out window), using mainly the SR1 test setup.

At the same time, he/she should thoroughly test and validate the first implementation of a new mitigation mechanism named “Smart L1A forwarding” that was recently introduced in the ROD Fw. The main concept of this mechanism is to temporarily stop sending L1A to the modules that have not sent data for a certain number of triggers yet, introducing a deterministic (driven by the Fw), small (localized) and short (for a few L1A) inefficiency. To maintain synchronicity in the data stream, dummy fragments are added by the ROD Fw for the triggers that are not sent.

The first tests in the SR1 setup showed encouraging results but a proper characterization of this feature is still needed.
Finally, a mitigation strategy using the “Smart L1A forwarding” mechanism is expected by the summer 2022, before the deployment and operation at Point 1.

Documentation:

https://indico.cern.ch/event/793417/contributions/3296050/attachments/1786984/2909877/ROD_FW_status.pdf

https://indico.cern.ch/event/803412/contributions/3340913/attachments/1830842/2998261/Smart_l1ID_status_16_april.pdf

https://indico.cern.ch/event/803415/contributions/3340919/attachments/1852073/3041226/Results.pdf

https://indico.cern.ch/event/803422/contributions/3340933/attachments/1895044/3126212/Firware_Update.pdf

https://indico.cern.ch/event/875292/contributions/3688974/attachments/2023901/3385118/Firware_Update.pdf

Requirements:

- Previous knowledge of VHDL and/or Verilog would be an advantage.
- Presence at CERN during the testing/deployment phase (4 months at least).

Time: 1 year if QT (50% FTE) or 6 months full time otherwise.