ATLAS On-detector Electronics Architecture

The overall architecture of the ATLAS Pixel on-detector electronics is summarized here in order to provide a context for understanding the requirements and design of the FE chip.

The ATLAS on-detector electronics consists of pixel modules and pixel opto-boards. The pixel opto-board supports the transmission of clock and control information to the pixel modules and the transmission of pixel data off-detector. The pixel module includes sixteen FE chips bump-bonded to a common high-resistivity sensor substrate, and one MCC chip bonded to a Flex Hybrid which provides the interconnections between the seventeen chips which comprise a module. The basic connectivity and interfaces are summarized in Fig. 1.

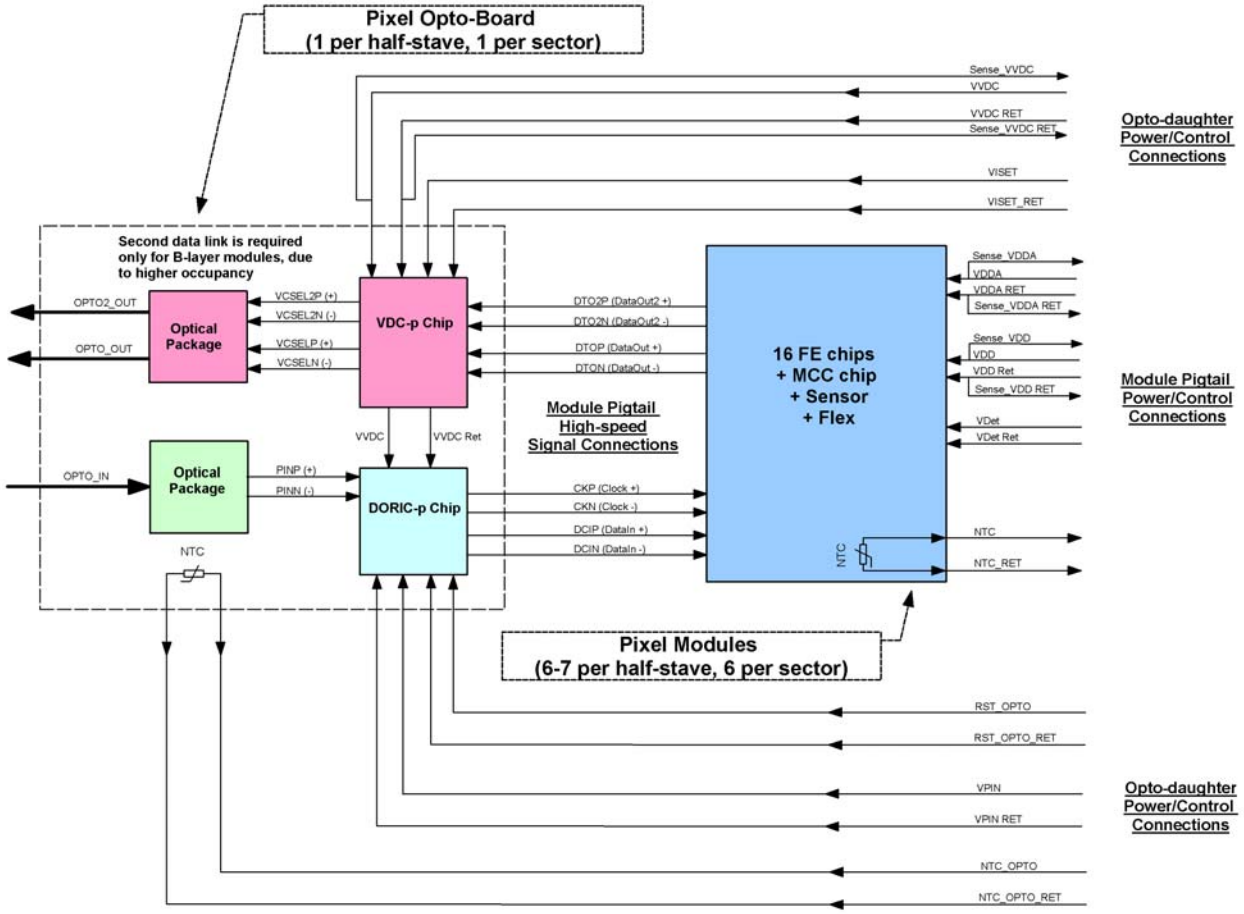


Figure 1 Schematic view of the basic connectivity of the ATLAS pixel on-detector electronics. Basic blocks are the opto-board (left) and the pixel module (right).

The power supply connections are all floating at the supply end, with all grounding/referencing performed on the pixel module or the opto-card. This is the only way to cope with the large voltage drops in the supply cables, as well as providing a consistent single-point grounding scheme. The opto-card received bi-phase mark (BPM) encoded clock and command information

on a single input fiber per module. This encoded information is decoded by the DORIC, which in turn provides the Clock (CK) and Command (DCI) information to the individual modules. This information is transmitted over a short (about 1 meter) twisted pair electrical cable, using LVDS signaling, to the modules. In the opposite direction, the module transmits a single data stream (DTO or DTO2) for the outer pixel layers and a double data stream (DTO and DTO2) for the B-layer. This is transmitted in LVDS form, using an NRZ protocol, and is then directly encoded optically by the VDC. Typically, a digital zero becomes a 1mA current through the VCSEL transmitter (off) and a digital one becomes a 10mA current through the VCSEL (well above threshold). The actual on-current is programmable using the VISET control voltage. Additional control signals include the opto-reset to ensure that the DORIC is properly locked to the 40MHz clock following a power-up sequence, the VPIN voltage to bias the silicon PIN diodes used to convert the clock and command information from optical to electrical form, and the supply voltage VVDC used to power the DORIC, the VDC, and indirectly, the VCSEL transmitter arrays. The temperature of the opto-card is monitored using a 10KΩ NTC ceramic thermistor. The device used has an intrinsic precision of 1% and is very radiation hard. It is used as both a monitor and a temperature interlock to prevent overheating.

The pixel module itself requires two low voltage supplies, VDD is the digital supply and VDDA is the analog supply. The grounds of these two supplies are normally connected together on the Flex Hybrid for the module, which is the single-point ground for an individual module. These supplies are fully separated inside each front-end chip, and there is independent decoupling close to each FE chip for the two power supplies. Noise immunity between these supplies is then created by the inductance of the power bond wires and the separate decoupling and power nets on the module. In order to compensate for the large voltage drops in the low-mass services (the last 12m of the services chain), the two module power supplies are individually regulated to the correct value on the Flex Hybrid using remote sense lines to ST rad-tolerant regulators. In the longer services, these sense wires are twisted together with the supply lines in a quad twist cable. For simplicity in the micro-cables, they are simply a second twisted pair. The decoupling scheme for each module includes an individual 10μF 10V ceramic capacitor for each low voltage supply on the module flex hybrid, as well as a 0.1μF 10V ceramic capacitor for each low voltage supply near each individual FE chip. The additional sensor bias supply VDet, is referenced to VDDA (not Analog ground) to optimize the noise rejection of the front-end electronics, since the preamplifier in the FE chip uses a PMOS input device whose source is connected to VDDA. This relatively low-current supply is isolated by individual 10KΩ series resistors on each of the two inputs, followed by a 1nF 1KV ceramic capacitor to bypass input noise current on the VDet supply before they reach the sensor itself. The temperature of the pixel module is monitored using a 10KΩ NTC ceramic thermistor mounted on the flex hybrid. The device used has an intrinsic precision of 1% and is very radiation hard. It is used as both a monitor and a temperature interlock to prevent overheating.

The pixel module controller chip has been carefully designed to avoid the need for a reset signal, and this has been demonstrated over long periods of operation, including radiation testing. The communication with the module occurs using LVDS-based differential signals. The driver/receiver circuits implement a fairly standard steered current 3.5mA output, which will swing around a mid-point of approximately VDD/2. The empirically determined cable impedance for the micro-cables from the pixel module to the opto-card is about 75Ω, so

corresponding values of the termination resistors are used on the module flex hybrid and the opto-card.

The pixel module connectivity is summarized in Fig. 2, showing the FE chips and the MCC chip, and their required interconnects. The MCC carries out slow control (configuration) of the sixteen FE chips by sending serial commands, using a simple protocol based on a geographical address (a broadcast bit is also available), a command field, and a data field. The signaling is CMOS-based to minimize pin-count, since this slow control path is never active when the FE chips are actually taking data. These three signals are bussed from the MCC to all sixteen of the FE chips on a module. The real-time control and synchronization of the pixel module is carried out using three fast (LVDS) signals. The LV1 signal is used to identify which beam crossings have corresponding Level1 triggers, the SYNC signal provides a hierarchy of synchronous resets to the FE chips, and the STR signal provides the timing for calibrations of the FE chips. These three LVDS signals are also commonly bussed on the flex hybrid. Finally, the output data line from each individual FE chip is connected directly to a corresponding input to the MCC chip. These outputs are single, short point-to-point links and use a lower power LVDS driver with a steered current of only 0.5mA, which is then terminated in 600Ω to provide the nominal LVDS voltage swing at the receiver. The FE output data is multiplexed from a variety of internal sources, but is always synchronized with the CK clock.

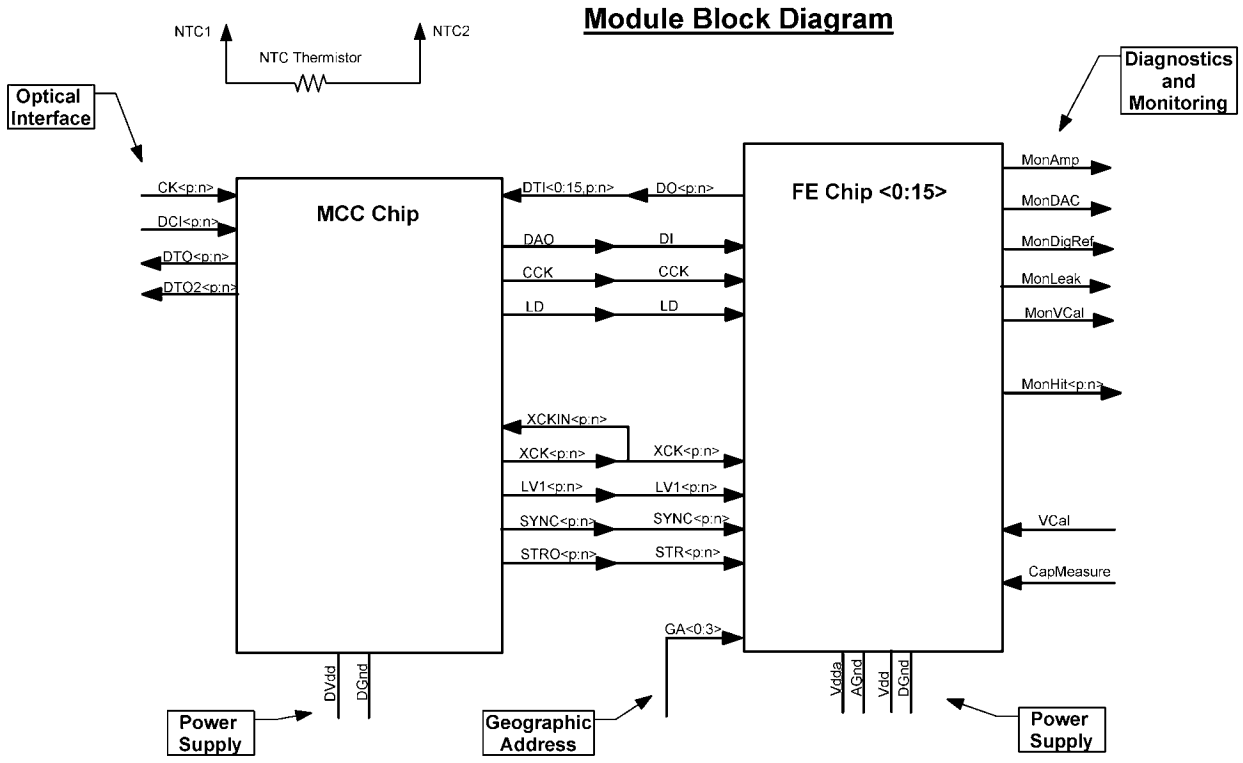


Figure 2 Schematic view of the basic connectivity of the ATLAS pixel module. Basic blocks are the MCC chip (left) and the FE chip (right).

ATLAS Pixel FE-I Chip: Design Requirements

The ATLAS Pixel FE chip, implemented in 0.25μ IBM CMOS6SF technology, must satisfy a number of performance requirements for ATLAS.

In the following, the orientation of the FE chip is always assumed to be with the wire bond pages located at the bottom of the die.

Geometry

The pixel FE chip implements the standard ATLAS pixel geometry. This is based on 18 columns of 160 pixels each. The pixels have a vertical pitch of 50μ and a horizontal pitch of 400μ. They are organized internally into 9 column pairs. Within each column pair, pixels are placed with their inputs at the outside boundary of the column pair, so that the pixel pitch in the horizontal direction is 750μ.

The input pads are 20μ top metal octagons with a 12μ opening in the passivation.

When diced, nothing is allowed to extend more than 100μ beyond the active pixel area on the sides and top of the FE chip. This severely limits the addition of any circuitry in these edges of the design. In practice, in order to satisfy the IBM design rules, a ChipGuard structure is implemented 38μ from the edge of the design.

The peripheral logic and I/O pads are allowed an additional 2800μ of space at the bottom of the die, making the final design size 7200μ by 10800μ. This leads to a maximum diced part size of 7400μ by 11000μ.

The I/O pad structure is standardized around a large pad of 100μ by 200μ on a 150μ pitch. There are 47 pads allowed in the die layout (the original 48th pad has been taken over by the required IBM logo in the lower left corner of the die). The large I/O pads are present to provide sufficient area for the multiple needle probing (initial wafer probe, single bumped die probe, bare module probe) required during production, while still providing adequate surface area for at least two wire-bond attempts. In addition to the wire-bonding pads, a standard 4-bump bump-bonding I/O pad is attached to each I/O pad. This is used for prototyping of MCM-D module in which all FE chip I/O pads are connected via bump-bonds instead of wire-bonds. As this is not our production configuration at this time, we presently use the 17 bump-bond pads outside the standard 30-pad region to redundantly encode the reticle number from which each die came (no bumps is a zero and 4 bumps is a one). This encoding is built into the bumping mask.

Due to the tight constraints on the module envelope required in the barrel region of the pixel detector, only the central 30 wire-bond pads are connected in an actual module. The additional pads are provided for additional (backup) features, as well as diagnostic and monitoring pins that play a critical role during design testing and evaluation.

Power Consumption and Power Management

The voltage design goals for the FE-I chips were to stay safely below the nominal process operating voltage of 2.5V in order to leave significant margin for remote power distribution as well as radiation effects. The design targets for the operating voltages were VDD = 2.0V and VDDA = 1.6V. The current budget used for the FE design was based on experience with designs

in 0.8μ processes. For the analog supply, the goal was a nominal current of 60mA and a maximum current of 80mA. For the digital supply, the goal was a nominal current of 25mA and a worse case current of 40mA. For the digital supply in particular, the target was not something fully under our control. The final current consumption for FE-I3 is roughly 75mA on VDDA and 35mA on VDD. The maximum operating voltage for VDD was taken to be the maximum nominal process operating voltage of 2.5V (in principle, one is allowed to operate up to 2.7V and still meet process lifetime specifications from the vendor). It was required that the design should operate up to this maximum VDD for any nominal analog supply voltage, as it might prove necessary to raise VDD after irradiation in order to achieve appropriate levels of performance.

Radiation Hardness and SEU Tolerance

The requirements for total dose tolerance over the ATLAS pixel detector lifetime have been estimated to be 50MRad of ionizing radiation, including modest safety factors as specified by the ATLAS radiation hardness policy. This policy requires us to check the radiation hardness of sample assemblies from each delivered set of wafer lots (pixels is expecting to break up the 250 wafer order into five lots of 48 wafers each). As the on-detector electronics is implemented in a pure CMOS process, we are not required to qualify the electronics designs separately with photon and neutron sources as well. We have chosen to carry out all of our qualification work at the CERN PS, using 20-24 GeV protons, which provide a mixture of ionization and displacement damage (K factor is 0.5 for these protons).

The requirements for SEU tolerance are not so clearly specified. There are several general considerations. First, the large amount of configuration information stored in the FE and MCC chips should not be corrupted by SEU effects at a rate that has a significant effect on module operation. For pixel-level configuration information, where the time required to refresh the values for an entire module is large, the bit flip rate should be low enough to prevent small numbers of individual pixels from developing low thresholds or other pathologies. This storage must be very compact, and the SEU-tolerance is best achieved by a robust latch design. For Global chip-level configuration, a greater level of hardness is necessary to avoid bit-flips that can completely disrupt the operation of a module. In this case, space is less critical, and triple redundancy is the best solution. Note it is also necessary to protect the write and reset circuits used for the configuration data, as they provide a simple mechanism for corruption or modification of large numbers of configuration bits.

It is also important to design in robustness against upset of clocked logic as well as static configuration. State machines should be robust against SEU events, and should not have hidden states or other unpredictable behavior if individual DFF change state due to SEU. In addition, critical state machines and logic should use a more robust approach. After some study, we have adopted an SEU-tolerant DFF design as the simplest path to achieve this result. Note also that SEU effects should in general not lead to the loss of synchronization in the data stream, but only to the corruption or loss of individual hits.

Peak fluences in the B-layer are about 10^8 particles/cm^2/sec. There are 286 pixel modules in the B-layer. The upset rate in a B-layer module for errors which would require module reconfiguration should be low enough that stable operation of the complete B-layer for order 1000 seconds is possible. This would require that for a typical case of 300 bits of critical global configuration, the SEU cross-section should be less than about 10^{-16} cm^2/bit. For the pixel

configuration data, where there is about 50K bits of data in the same area, a similar bit-flip cross-section would lead to an upset about once per 10 seconds in the entire B-layer. However, as such upsets are relatively harmless in most cases, an SEU cross-section of about 10^{-15} cm^2/bit would be acceptable. For reference, the approximate re-configure times for the FE Global Registers in a module are about 1ms, and for the Pixel Registers are about 200ms.

Front-end Performance Requirements

Noise Performance versus CDet and Ileak

Based on early comparisons of noise and capacitance in test chips with noise in bump-bonded pixel chips, have adopted design target of 400fF for normal and long pixels. This is increased to about 700fF for the inter-ganged pixels and about 1000fF for the ganged pixels. Both input transistor size and input transistor bias current have been scaled to cope with this range of input loads.

In addition, the presence of leakage current at the preamplifier input introduces parallel noise in the preamplifier. The front-end design must be able to cope with leakage currents up to about 50nA per pixel (typically, after beneficial annealing, a leakage current of about 25nA per pixel is expected at the nominal –7C operating temperature). A leakage current tolerance up to 100nA per pixel would be preferred in order to provide additional margin for possible operation at slightly higher temperatures (up to 0C).

The total noise induced in the preamplifier, referenced to the input, should then be less than about 400e, so that a total "noise" including the threshold dispersion would be less than 500e, allowing six sigma of separation from the noise floor when operating at a nominal 3000e threshold.

Threshold Performance

The threshold should be adjustable over a range up to about 6Ke, to provide good margin for controlling the noise occupancy.

The dispersion of the tuned threshold should be less than about 200-300e, including irradiation and temperature dependent effects. This, in quadrature with the single pixel noise above, would provide a total "equivalent" noise of less than 500e.

Timing, Timewalk, and In-time Threshold Performance

The expected signal from the sensors after the lifetime dose of 10^{15} NIEL equivalent is about 10-15Ke. In order to efficiently detect the passage of any particle depositing this energy into the sensor, it is necessary to achieve an in-time threshold of about 5Ke.

The operational definition of the in-time threshold is the following. First, the asymptotic response of a single pixel to a large charge of about 100Ke (4 MIP) is used to define a reference time t0. Then, a total of 20ns of the available 25ns is allocated to the single pixel for its pulse-height slewing (timewalk) budget. Therefore, the in-time threshold is the lowest charge that can be injected into a pixel in order to give an output pulse within 20ns of the asymptotic t0. If the pixel module is operated at a threshold of 3Ke, then the in-time threshold requirement of 5Ke corresponds to an overdrive requirement of 2Ke. Note the definition of the threshold here is the

smallest charge required to fire a pixel 50% of the time, where one is willing to wait as long as necessary for the pixel to actually fire.

A second critical issue is the dispersion of t0 values throughout a module. This should be less than 1ns RMS, or about 3ns peak-to-peak, in order to avoid further compromising the timing budget for a module.

Noise Occupancy

Noise occupancy should be less than 10^{-6} hits/pixel/crossing. This would correspond to about 0.05 hits/crossing/module. This would be the maximum level to avoid excessive numbers of noise hits that would confuse the pattern recognition. Note that the charge information can also be used to help identify noise hits once the data is read out, since noise hits will usually be close to threshold. A noise occupany lower by another 1-2 orders of magnitude would be very advantageous to obtain a very clean system.

Crosstalk

Crosstalk is defined as the charge that must be injected into a neighboring pixel in order to fire a reference pixel. It is expressed in percent, which is the ratio of the injected charge into the neighbor, divided by the threshold of the reference pixel. The cross-talk should be less than 5-10% to avoid excessive numbers of spurious hits in high-occupancy events due to the Landau tail of the charge distribution. A 3Ke nominal threshold represents about 15% of the mean charge of a single MIP particle, so 5% crosstalk results in a small probability for extra hits.

Double Pulse Resolution

The separation between the rising edges of two pulses that should still be resolvable by the readout electronics is determined by the pixel occupancy and deadtime efficiency goals. For the maximum incident fluence in the B-layer, there could be 10^8 particles/cm^2/sec, and there are 5000 pixels/cm^2, so the average counting rate on a pixel is 20KHz. A 0.5μs deadtime per hit then leads to a 1% overall deadtime. In the outer layers, or at a lower luminosity, a 2μs deadtime per hit would be tolerable.

In the FE-I readout architecture, there is no support for multiple hits on a pixel. Once a pixel is hit, its hit must be transferred out of the pixel and into the EOC buffers, so the time required from the arrival of a hit until the pixel is available for another hit consists of two components. The first is the width of the discriminator (TOT) pulse, which is adjustable by controlling the preamplifier feedback current. The second is the time to transfer the hit to the EOC buffers. This depends on the column occupancy, which in turn depends on the rate of column pair readout. This readout rate is programmable, up to a maximum of 50ns per hit. This rate is determined by the need to evacuate the necessary number of hits from the column pair before the nominal LVL1 latency of 3.2μs.

The requirement for the FE-I design is then that the single pixel output pulse width, tuned by adjusting the feedback current that returns the preamplifier to baseline, can be set to the required small value without any stability, threshold, or noise problems. It is required that it is possible to adjust this return to baseline to be less than 500ns for a 1 MIP charge, and that when this is done, the rest of the readout system is capable of processing two hits on the same channel within 500ns of each other.

Charge (TOT) Measurement

The FE chip is required to provide a charge measurement in the form of a time-over-threshold value. This measurement is approximately linear in charge over a large range in the FE-I design. This linearity imposes limits on the maximum charge hit that can be registered within a given trigger latency, since TOT pulses that are too long will arrive too late at the EOC buffers and miss their LVL1 trigger accept. When set for maximum charge resolution, the FE-I chip will then have the MIP peak set at about 25-30 crossings, and a maximum charge range of approximately 4-5MIP. Further increasing the feedback current reduces the charge resolution, but provides for a larger dynamic range.

In order to minimize the complexity of data calibration required off-chip to achieve the required modest charge resolution performance, it is important to be able to tune the charge response of different pixels in one chip, and between different chips. The inter-chip TOT performance can be tuned using the global feedback current. The individual pixel response can be tuned using the individual feedback current DACs (FDACs) in each pixel. It should be possible to adjust the response of different pixels within one chip to a uniformity of about 10% in order to avoid the need for calibrations of individual pixels off-chip.

Internal and External Calibrations

There should be two different mechanisms for injecting charge into a selected pattern of pixels in the FE chip. The standard method, to be used in the final pixel module, relies on an internal VCal DAC in each FE chip to provide a programmable voltage. A FET switch in each pixel is used to generate a voltage step from VDDA down to VCal. This voltage step is applied across an injection capacitor to produce the charge pulse into the preamplifier.

In order to achieve adequate dynamic range for the charge injection system, it is required to provide two separate ranges. One is optimized for the low charge region, and for threshold scans in particular, where a step size of about 50e is required to be able to measure the noise in individual pixels by fitting their threshold turn-on curves. The other is optimized for the high charge region required for studies of TOT or timing, and should extend well above 100Ke in order to characterize the asymptotic performance of the FE chip.

A second means of charge injection should also be provided for more specialized measurements. This second method involves the external generation of an appropriate voltage step, which is then applied directly to an input pin on the FE chip. This allows greater control, and lower systematics, for more detailed studies of the response of the electronics. This external injection path within the FE chip should be optimized for excellent high-frequency response for the fast pulse edge, so the trace needs to be wide enough to minimize RC transmission line effects, and to be well-shielded to avoid creating crosstalk from it, as well as avoiding pickup from other signals.

Digital Readout Requirements

The digital readout architecture must provide a unique association of each hit seen by the front-end with a 40MHz beam crossing. This should be performed with a single, SEU-tolerant, 8-bit timestamp or BCID for each FE chip. The FE chip must then store the hits for long enough to make a coincidence with a LVL1 trigger with a latency up to 3.2μs. It must provide adequate buffering of these hits prior to the arrival of the trigger to avoid hit losses at the highest B-layer

luminosity. Simulations have indicated that 40 buffers or more per column pair are required to achieve this performance.

Note that effective zero suppression is required to reduce the hit processing requirement for a column pair from the nominal rate of 320 pixels every 25ns to the expected hit rate of about 0.15 hits per crossing per column pair at the highest B-layer fluence. However, our noise occupancy requirements place the strongest constraints on the zero-suppression.

In order to carefully validate the integrity of the transmitted data stream, it is critical to embed lots of redundant information. Each hit shall be tagged with the 4 LSB of the 40MHz BCID, in order to verify that all hits within a given event transmitted by a module do in fact come from the same beam crossing. This also requires a reliable mechanism to synchronize the beam crossing counter between different FE chips.

Control Requirements

Global Control and Global Register

The overall control of the FE chip parameters requires the presence of a Global Register. This register must be readable as well as writable. It also should be implemented as a shadow register, so that data can be shifted in, and then transferred to the actual latched register with a single strobe, to avoid inconsistent values of the different bits in the register during updating.

This register must be extremely SEU-tolerant, to avoid corruption of critical FE operating parameters by SEU. In addition, it will implement a simple parity check to allow detection of single-bit flips. This will require an additional user bit to force the parity of the register to be even, plus a mechanism for calculating the overall register parity and reporting errors.

In order to achieve the necessary SEU-tolerance, the register will be implemented using a triple-redundant latch with majority logic. An additional bit flip output will be generated from each triple latch, which will be set if the three internal latches do not have an identical state. This will allow testing of the redundancy, as well as monitoring the rate of internal upsets that do not change the state of a bit, but which eliminate the redundancy.

Pixel Control and Pixel Register

The control of the configuration of each individual pixel should be implemented using a single shift register to access individual latches inside each pixel. This shift register must be configurable so that defective column pairs can be bypassed, to avoid the loss of a complete chip due to the loss of a single bit in this shift register. It should be possible to read out the contents of the shift register, and a mechanism should also be implemented to allow readback of the individual latch contents by a parallel load of the shift register. The shift register itself does not require significant SEU-tolerance, because data is not stored in the register for more than 1ms under normal conditions. However, the pixel latches must store the configuration during operation of the chip, and must be as SEU-tolerant as possible within the modest available space.

Front-end Bias Generation

The front-end biasing will be generated on-chip without requiring any external analog signals. The nominal values should be defined by an internal current reference, which should be reasonably stable under irradiation and temperature variations. The actual bias values for all key currents for the analog front-end should be programmable by 8-bit current-mode DACs. It must

be possible to multiplex out the current provided by each DAC through a monitoring pin in order to allow full analog characterization of the DACs.

Reset Generation

There are several hierarchical, synchronous resets which should be generated inside the FE chip upon receipt of relevant signals from the SYNC input pin.

First is a Sync Reset, which resets the internal trigger FIFO, and clears all memory of the events currently stored in the FE chip.

Second is a Soft Reset, which should reset all of the digital readout circuitry into the "empty" state. This includes resetting the hit logic in individual pixels, as well as resetting the circuitry which transfers hits down the column pair, and the EOC buffers themselves. Very significantly, the internal BCID counter must also be reset to zero. Therefore issuing a SYNC pulse of te appropriate width to a module will synchronize all BCID counters for the sixteen FE chips in the module. All internal state machines are also reset into their idle state. No configuration should be affected by issuing a Soft Reset, so after issuing such a reset, it should be possible to continue issuing LVL1 triggers to the FE chip without re-writing any registers.

Finally, a Hard Reset is implemented. This performs all of the features of the Soft Reset, and in addition, resets the Global configuration information, defining the low power power-on state of the FE chip.

An internal power-on reset circuit holds on the Hard Reset signal during power up to ensure that the chip is always powered up into the reset state.

Which reset is issued is determined by the width of the SYNC pulse. Pulse widths below 4 crossings result in a Sync Reset, below 8 crossings result in a Soft Reset, and with 8 or more crossings, result in a Hard Reset. The width of the internal reset pulse is defined by the width of the SYNC pulse once it satisfies the appropriate requirements, for example a width of 4 crossings would result in a 25ns internal Soft Reset, whereas a width of 5 crossings would result in a 50ns internal Soft Reset.

Self-Trigger Capability

A self-trigger capability is implemented to support calibrations of individual FE chips with an X-ray source. This makes use of an internal fast OR of all discriminator outputs (each pixel can be programmed to participate or not in this OR) to generate a LVL1 trigger directly after a programmable latency. In order to avoid uncontrolled generation of triggers, this circuit requires arming with an external LVL1 trigger, after which the next internal fast OR will generate a self-trigger, and the data can be recorded. The self-trigger will not fire again until armed with another external LVL1 signal.

Leakage Current Measurement

Capacitance Measurement

Auto-tune Capability

Testability Requirements

Analog (DACs, references, test pixel)

Digital (digital inject, CEU MUX,

ATLAS Pixel FE-I3 Chip: Design Description

The ATLAS Pixel FE-I3 chip is a front-end chip designed to digitize information from pixelated silicon sensors. The chip has an active dimension of 7.2mm wide and 10.8mm tall, and contains about 3.5M transistors. It is the third generation ATLAS pixel design in the IBM CMOS6SF process, but now about the sixth generation of the underlying design. The chip contains 2880 channels of charge sensitive amplifiers attached to fast digital readout. The digital readout operates from a 40MHz clock, referred to as the crossing clock, or XCK. The channels (pixels) are arranged in a two dimensional array of eighteen columns, each containing 160 pixels. The pixel dimension is 50μ high and 400μ wide.

The chip is designed for use in a pixelated silicon particle detector that will be installed in the ATLAS experiment at the CERN LHC. In this application, it must detect the passage of charged particles that are produced at the beam interaction rate of the LHC (40MHz). A pixel module is constructed using fine-pitch bump-bonding (50μ pitch) to connect 16 FE chips to a single 300μ thick pixelated silicon sensor. This provides a module with very low mass, and an active area of 10 square centimeters, divided into roughly 46K pixels. A total of about 1750 such modules will be arrayed into cylinders and disks to create an effective particle physics detector that can cope with the roughly 500-1000 charged particles that are produced every 25ns at the LHC. The pixel detector is located as close to the beam as possible, and therefore must withstand a lifetime ionizing radiation dose of 50MRad. In order to achieve this, special layout rules have been used in which all NMOS are annular, and are individually surrounded by guard rings in order to control any leakage paths that develop in the thick oxides during irradiation.

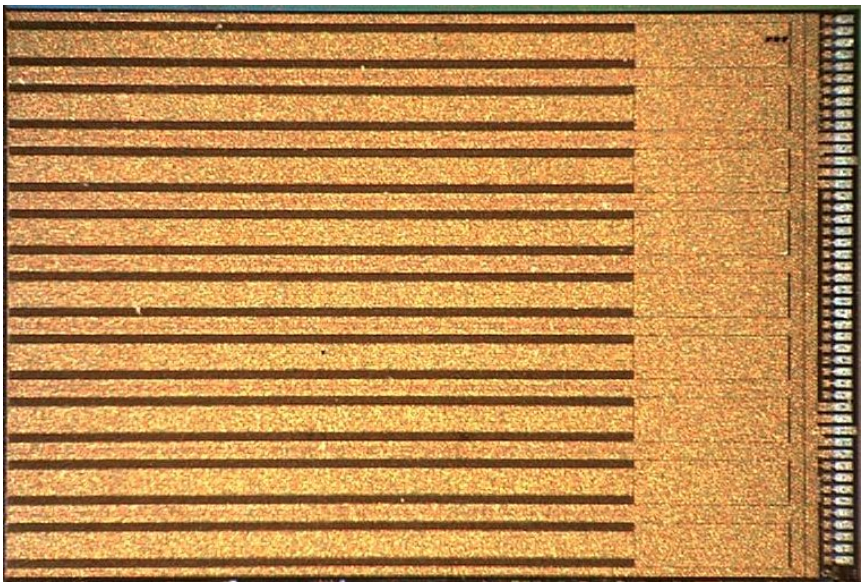


Figure 3 Photomicrograph of FE-I1 chip.

The Pad Frame

The pad frame for the FE-I1 chip contains 47 I/O pads located at the bottom of the chip. These pads implement all recommended IBM ESD design rules, suitably modified for radiation hard designs.

All high-speed I/O to and from the chip is performed using LVDS-compatible differential drivers and receivers. The biasing of these blocks is controlled by a current reference to reduce sensitivity to process variations. The output drivers use a reduced output current of 0.5mA instead of the 3.5mA standard, and are normally terminated using 600Ω resistors to produce the standard 300mV signal swing at the receiver. They also swing about an offset voltage of half the digital supply voltage, rather than the 1.2V LVDS standard. However, commercial LVDS receivers terminated with a 600Ω resistor work well with the FE chip.

Less critical I/O is performed using CMOS pads, some of which use pull-up or pull-down resistors to determine their default state.

The FE chip uses two power supplies. The digital supply is referred to as VDD. It is referenced to DGND, and has a nominal operating value of 2.0V, although the chip works over the full range from about 1.4V to 2.5V. The analog supply is referred to as VDDA. It is referenced to AGND, and has a nominal operating value of 1.6V. There is an additional power net referred to as VDDREF, which is used to provide power only to the preamplifier. This net is used as the final shield layer for the FE chip (essentially all of the top metal layer is VDDREF), and is the reference for the preamplifier input. For normal chip operation, VDDA and VDDREF are connected together outside the chip (through the wire-bond inductances). All three power supplies have two input pads for redundancy and reduced internal voltage drops. These pads are positioned at approximately the ¼ and ¾ points in the pad frame. The VDD and VDDA power supplies are protected by an IBM-recommended transient clamp to provide additional ESD protection in case a discharge occurs directly to a power supply pad. The VDDREF supply is diode-clamped to the VDDA supply.

The AGND net is connected to the sources of the relevant transistors, and is in turn connected directly to the substrate near the pad frame. The bodies of the analog transistors are connected to a separate net, which is also connected to AGND near the pad frame. The DGND net is electrically separate and is connected to the sources of the digital NMOS. The bodies of the digital transistors are connected to a separate net, which is also connected to AGND near the pad frame. All of the ESD protection diodes are also referenced directly to the substrate as recommended by IBM. This scheme has been adopted to try to isolate large transient digital currents to the greatest possible extent from the analog circuitry. Given the complex grounding scheme described above, it is always necessary to connect AGND and DGND together before applying power to the FE chip, even if only the digital supply is powered.

There are a number of current references in FE-I3, all with the same basic design using a poly resistor and a MOS in weak inversion. There is a “digital” reference in the pad frame for the LVDS I/O pads. It also provides bias generation for the sense amplifiers in the column pair readout and for the HitBus receivers in each column. There is a master analog reference in the bottom of column region that provides a reference for the twelve current-mode DACs (with the exception of the MonLeak DAC), and also provides bias generation for the digital decoupling capacitors and for the active bias compensation circuitry in each pixel. There is an additional analog reference used for the MonLeak DAC. In FE-I1, the sense amplifiers, the HitBus receivers, and the decoupling capacitors used three separate references that were strongly voltage

dependent. This has been improved for FE-I2 and FE-I3 with the voltage-independent references, in order to allow the use of the IBM burn-in protocol at elevated supply voltage. Finally, each of the two regulators has a separate bandgap reference to define the regulator output voltages.

The locations and meanings of the I/O pads are defined in Appendix 1.

The Analog Front-end

Each individual front-end consists of a high-gain, fast preamplifier using a feedback capacitance of nominally 5fF, and a DC feedback scheme capable of compensating for DC leakage currents of more than 100nA on the preamplifier input. Note that the leakage compensation only works for "negative" leakage current, such as that generated by a large resistance from the preamplifier input to ground. "positive" leakage current is not compensated, and will stop normal preamplifier operation. Typical input signals from a silicon sensor are about 3.5fC, or 20Ke equivalent. The preamplifier is followed by a DC-coupled differential second stage and a fast differential discriminator. The discriminator threshold can be varied over a range from 0 to about 1fC, with a normal operating threshold of about 0.5fC. The biasing of critical nodes in the preamplifier and discriminator, as well as the threshold adjustment, is controlled by a total of eleven on-chip 8-bit current mode DACs, which are in turn supplied by a current reference.

The sensors used in ATLAS have two classes of special pixels, both of which create increased capacitive loading of the preamplifier input. All pixels in column 0 and 17 are 600μ long instead of 400μ long. This loading is not large enough to require a design change. In addition, there are special ganged pixels at the top of each column, where two pixel implants are connected to a single electronics channel. This is true for row 153, 155, 157, and 159. Because of the metal interconnections on the sensor, the "inter-ganged" pixels in rows 154, 156, and 158 also see an increased capacitive load. For this reason, in FE-I2 and FE-I3, the ganged pixels in row 153, 155, 157, and 159 have 4 times the nominal IP current and have an input transistor that is 3 times the nominal size. The inter-ganged pixels in row 152, 154, 156, and 158 have 2 times the nominal IP current and have an input transistor that is 2 times the nominal size. Although row 152 is not an inter-ganged pixel, it was modified to preserve the symmetry of the layout (there are 4 pixel pairs of the inter-ganged/ganged type and 76 pixel pairs of the normal type in a column).

The bias generation circuitry is all contained in the region just below the pixel channels, which we refer to as the bottom-of-column region. The bias voltages are distributed throughout the two dimensional array using a set of horizontal busses located at the very top of the chip. The biases are distributed as the Vgs of a diode-connected FET in the bottom of column region. A matching mirror transistor in each pixel then uses the Vgs voltage to regenerate the current locally. In FE-I1, there were significant variations in the local bias currents due to the voltage drops in the AGnd and VDDA power distribution nets (the AGnd net has particularly little metal, but conducts the combined current from VDDA and VDDREF, so it has the largest drops). A new bias distribution scheme was developed for FE-I2 and FE-I3 that uses an active voltage drop compensation technique to reconstruct the correct bias current in each pixel. This scheme has been applied to the two large currents which are AGnd referenced, namely IP and IL2. There is a single bias compensation circuit in each pixel, and even rows have the IL2 compensation circuit and odd rows have the IP compensation circuit. An IP/IL2 monitoring scheme, similar to the one used for MonLeak, has been implemented to check how well the bias distribution is working in FE-I2 and FE-I3. This monitoring scheme allows the user to multiplex out the IP or IL2 current

from any individual pixel pair in the FE-I3 chip through the MonDAC pin for measurement. These measurements show that the bias compensation circuitry works very well, and provides a very uniform IP and IL2 current for all pixels (sigma/mean is about 5%).

The threshold control has also been significantly improved for FE-I2 and FE-I3. There is now a global 5-bit threshold DAC (GDAC) with local circuitry in each pixel (the global 5-bit digital setting is distributed to a local 5-bit DAC in each pixel). This DAC allows one to adjust the overall threshold for the FE chip in a very linear and fine-grained way. Figure 2 shows the expected behavior of the threshold as a function of the setting of this DAC. There is also now a 7-bit local TDAC in each pixel (the DAC is actually six bits, but the seventh bit is available "for free" by choosing into which of two nodes to inject the TDAC current). Figure 3 and Figure 4 show the expected behavior of the threshold as a function of the TDAC setting and the GDAC setting. The rough slope for the TDAC is expected to be 75e per count for values close to the midpoint of the TDAC.

All DACs in FE-I3 (FDAC, GDAC, and TDAC) are defined to have positive polarity, so that increasing the FDAC will increase the feedback current, and increasing the GDAC or the TDAC will increase the threshold.

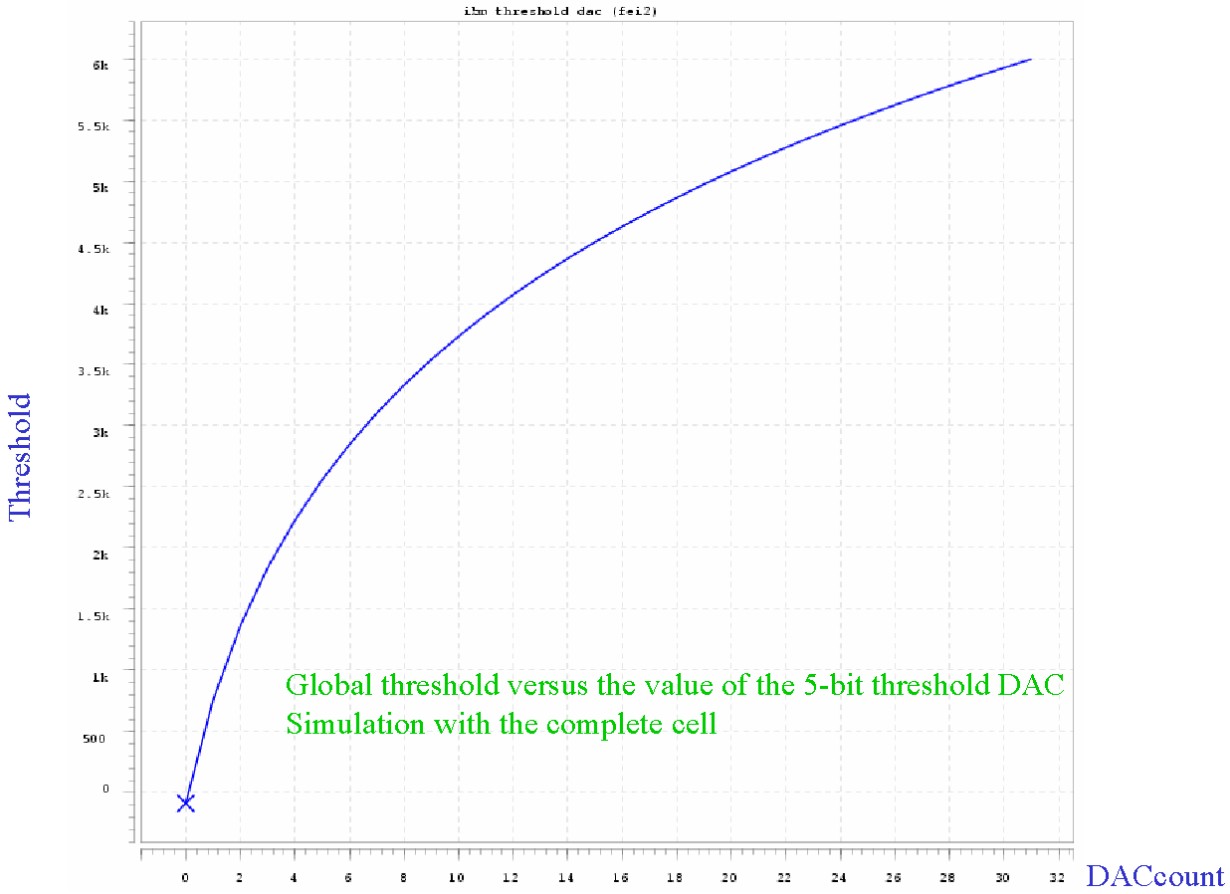


Figure 4 Simulated response of 5-bit GDAC on threshold.

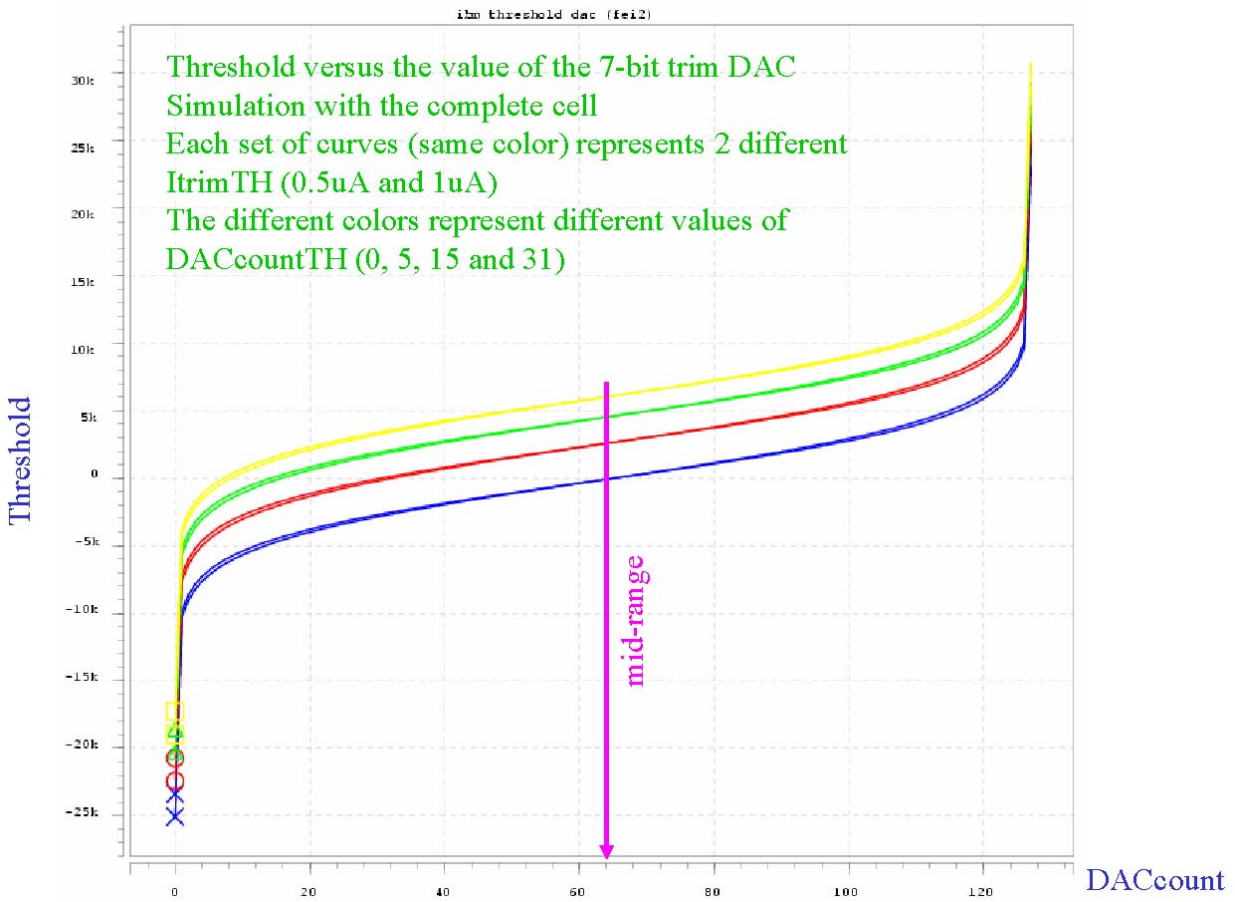


Figure 5 Simulated response of 7-bit TDAC on the pixel threshold. Different curves represent different values of the GDAC.

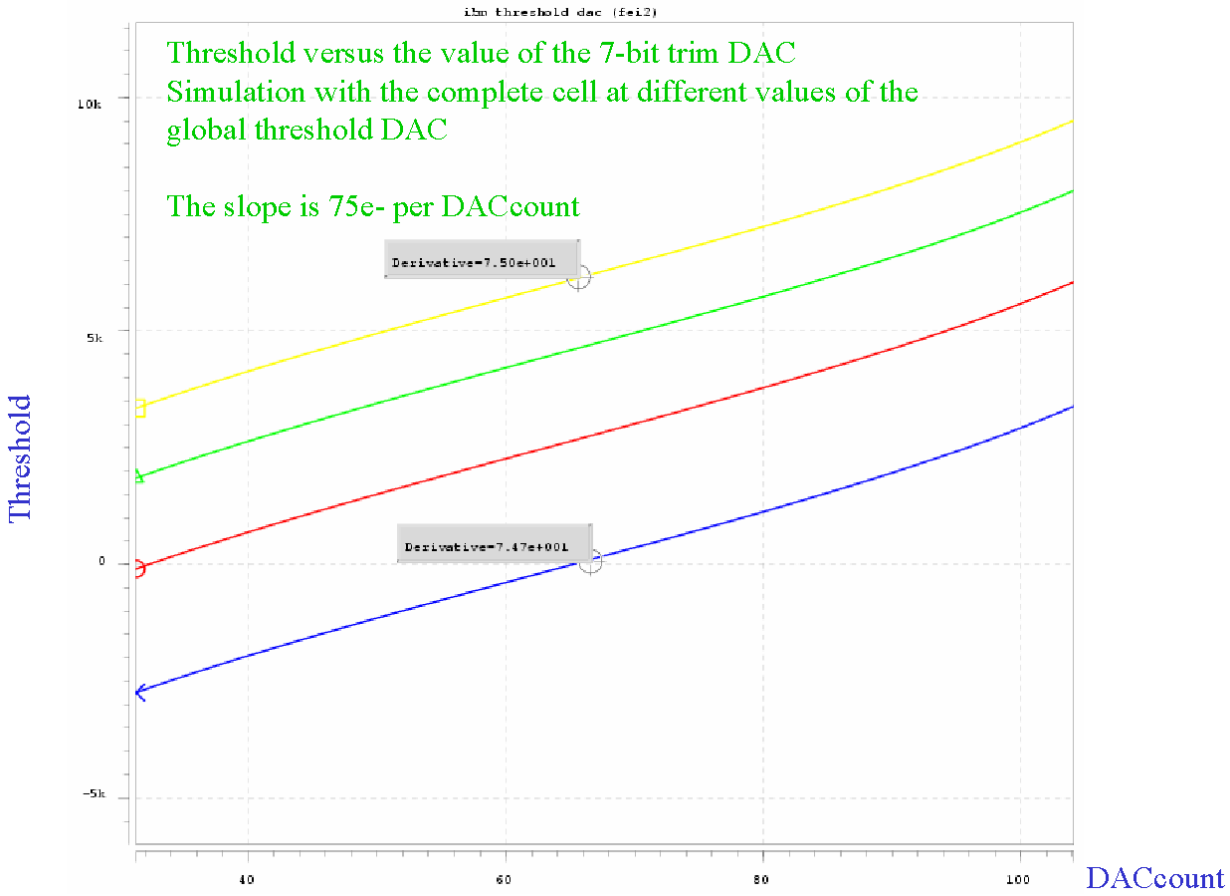


Figure 6 Simulated response of 7-bit TDAC on the pixel threshold, zoomed view near TDAC midpoint.

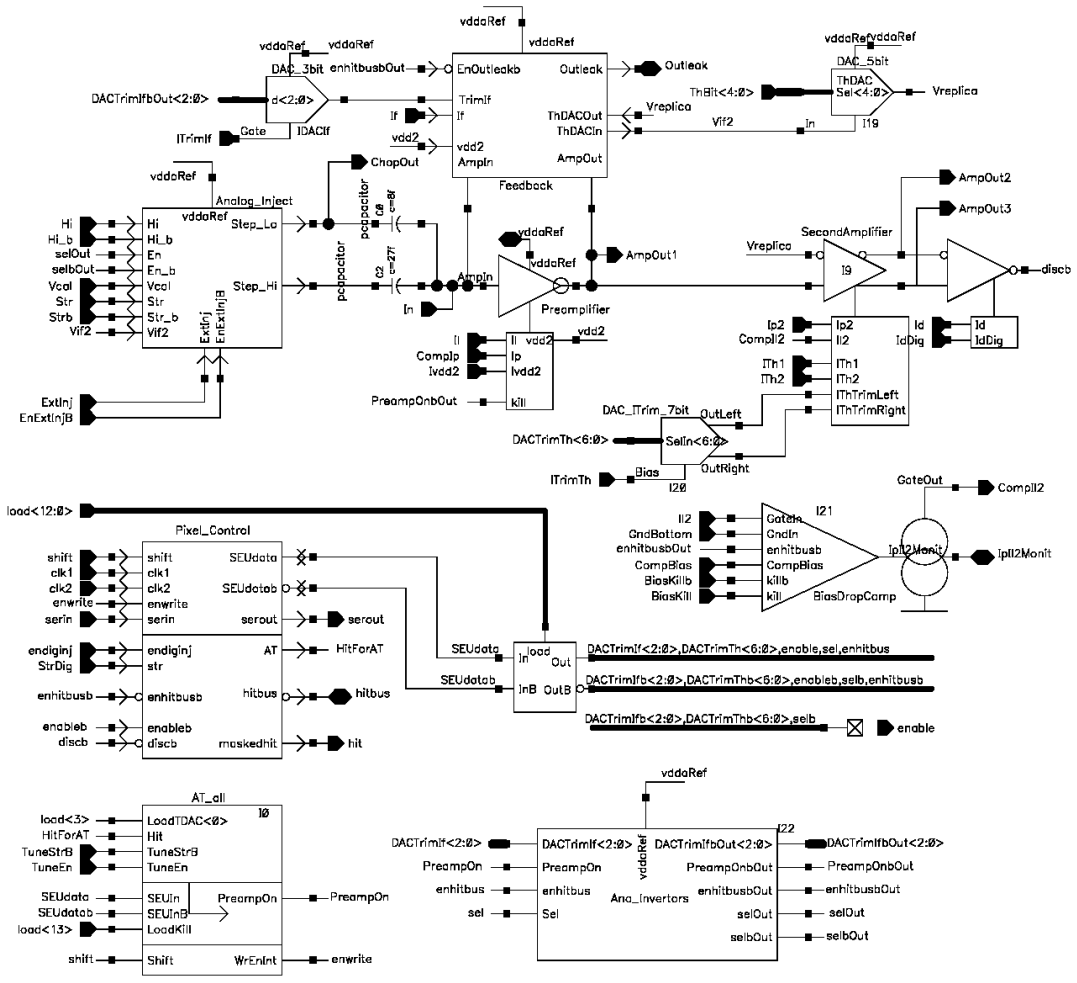


Figure 7 Schematic of Pixel Front-end and Control blocks

Figure 2 shows a high-level schematic of the pixel cell. The preamplifier is seen in the center, with its related bias connections for IP, IL, and IVDD2. The Kill control bit is also applied to the preamplifier block to disable the preamp without changing its power consumption. The complex feedback circuit, including the 3-bit FDAC and the 5-bit global threshold DAC (GDAC), is shown as a large block. The bias currents IF and ItrimIf are used to adjust the actual preamplifier feedback current. The complete preamplifier and feedback circuits operate from the VDDREF supply. This supply would normally be connected to VDDA at the wire-bonding stage. The injection circuit, along with the two separate injection capacitors, is shown on the left. This circuit either allows a direct pulse on the ExtInj line to enter into the injection capacitors, or it generates a voltage step by using the Str signal to switch the injection capacitors from VDDREF down to the VCal voltage provided by a DAC in the bottom of column region. The nominal values for the injection capacitances in FE-I2 and FE-I3 are 8fF for Clo and 40fF for Clo+Chi. The second stage amplifier and discriminator are shown on the right, along with their bias connections and the 7-bit TDAC used to control the threshold. Finally, the control logic and the associated 14 latch bits are shown at the bottom. The control logic also implements the digital injection mode, where the pulse on the StrDig line is injected directly into the pixel hit Logic to simulate the output of the front-end discriminator, as well as the HitBus FastOR logic. Note that

everything in the top of this schematic operates from VDDA and VDDREF, whereas the Control block is a mixed-voltage block that operates on both VDD and VDDA. All of the storage latches operate on VDD, and their outputs are coupled to the front-end through analog inverters to provide isolation from possible noise on the digital supply. Finally, there is a prototype auto-tune block to allow a quasi-automated scan of the threshold of the pixel. The operation of this block is described in more detail in Appendix 4.

The Control Circuitry

The FE chip is controlled by three registers: the Command Register, the Global Register, and the Pixel Register. The interface to these three registers is based on a simple serial protocol that uses three CMOS inputs. There is a slow clock (CCK = Command Clock) that operates at 5MHz. The presence of the command clock activates the command decoder in the FE chip. There is a data input (DI) and a load (LD) signal to complete the interface. Individual chips are addressed using a 4-bit geographical address (GA), which uniquely identifies each chip in a sixteen-chip multi-chip module assembly. Each FE chip has four GA CMOS inputs with pull-up resistors. Their default state provides a "one" for the address bit. A "zero" value for an address bit is created by wire-bonding the relevant pad to digital ground. For a sixteen-chip module, each FE chip has a distinct GA address, which can then be used to direct individual commands to a specific FE chip.

Commands consist of a command field, consisting of 29 bits transmitted when LD is low, followed by a data field of arbitrary length, transmitted when LD is high. The bits in the command field are stored in the Command Register, which is implemented as a series of standard cell DFF to form a shift register, and a special SEU-tolerant latch to store the data. The rising edge of the LD signal latches the shift register data into the Command Register Latches. The Command Register bits determine whether the chip is addressed, and whether data bits are expected, and what their meaning will be. The bits in the Command Register are defined in Appendix 2. Note that the implementation of the Command Register is such that it only retains the most recent 29 bits. If a longer bit string is send before the LD goes high, the results will still be fine as long as the useful bits are transmitted last (the excess bits just fall off the end of the shift register).

The Global Register is a 231 bit long register that is implemented as a shift register using DFF standard cells, and a special SEU-tolerant latch that is used for the actual data storage. Data is first shifted into the Global Shift Register, and then a WriteGlobal strobe is used to transfer the data into the Global Register Latches. Readback capability is implemented to allow transfer of data from the Global Register Latches back to the Global Shift Register using the ReadGlobal strobe. These two strobes are implemented as bits in the Command Register.

A typical command sequence to test the Global Register would involve the following:

- Issue a **ClockGlobal** command with 29 command bits and 231 data bits to shift the desired values into the Global Shift Register. Note that in order to read the data back later on, it is necessary to make sure that value DOMUX = 15 has been set, otherwise the interesting data will not be accessible.
- Issue a **WriteGlobal** command with 29 command bits and no data bits. This will transfer the contents of the Global Shift Register into the real Global Register latches. Note that

even when no data bits are transmitted, it is always necessary to bring LD high for at least one CCK period in order to properly latch the command bits into the Command Register.

- Issue another **ClockGlobal** command with all zero values in order to flush the Global Shift Register and make the test more reliable.
- Issue a **ReadGlobal** command with 29 command bits and no data bits. This will transfer the contents of the Global Register latches back into the Global Shift Register.
- Issue another **ClockGlobal** command to read out the 231 data bits from the Global Shift Register. Compare these bits against the values originally clocked into the shift register with the first **ClockGlobal** command.

The individual bits in the Global Register are placed close to the circuitry that they control. The result is that the Global Register is distributed throughout the bottom of the chip (the region which is 2.8mm high and 7.2mm wide that is below the active pixel matrix). The meaning of the individual bits is given in Appendix 2.

Each pixel contains a total of 14 configuration bits. These are implemented as SEU-tolerant latches as well. Access to these configuration latches is provided by the Pixel Shift Register. This is a 2880-bit long shift register implemented using simple MUX cells and a global two-phase clock generator in order to guarantee very conservative timing. In order to write a set of latches, data is loaded into the Pixel Shift Register, and then a Load strobe from the Command Register is used to latch the Pixel Shift Register contents into the selected latch simultaneously in each pixel. A parallel-load capability is implemented to allow readback of data from a selected latch in each pixel, where the selection is made by setting the relevant Load strobe in the Command Register. There are a total of 14 Load strobes corresponding to the 14 different latches in the pixel. The meanings of these 14 bits are defined in Appendix 2.

The Pixel Shift Register is divided into nine independent segments, one for each column pair. By setting bits in the Global Register, it is possible to enable each column pair. If no column pairs are enabled, data entering the Pixel Shift Register appears immediately at the output, providing a pass-through mode that allows checking of the basic input and output connections to the Pixel Shift Register. Each column pair can be individually enabled, allowing us to test the 2880-bit long register in nine individual 320-bit segments.

A typical command sequence to test the Pixel Shift Register would involve the following:

- Issue a **ClockGlobal** command with 29 command bits and 231 data bits to shift the desired values into the Global Shift Register. This will set the appropriate ColumnEnable bits to activate the different segments of the Pixel Shift Register (by default, the entire register is configured into bypass mode at power-up). Note that in order to read the data back later on, it is necessary to make sure that value DOMUX = 11 has been set, in order to enable the Pixel Shift Register data out of the DO output pad.
- Issue a **ClockPixel** command with 29 command bits and 320*n data bits, where n is the number of enabled column pairs defined in the Global Register.
- Issue another **ClockPixel** command to read out the 320*n data bits from the Global Shift Register. Compare these bits against the values originally clocked into the shift register with the first **ClockPixel** command.

In order to perform a more complete test by writing to, and reading from, a given set of pixel latches, a **Load** command must be issued to strobe the data into the latches. This is followed by clearing the Pixel Shift Register with another **ClockPixel** command and all zeros for the data. Finally, a **ReadPixel** command with the same **Load** strobe set is issued to transfer the latch data back into the Pixel Shift Register, followed by a final **ClockPixel** command to transfer the data off the chip.

Figure 3 Diagram of the path of the Pixel Shift Register as it snakes through the two dimensional matrix of pixel channels. Each column pair contains a U-shaped segment of the shift register as I goes up the left side and comes down the right side. The nine U-shaped segments in the chip can be separately enabled using the Global Register.

The Digital Readout Circuitry

The information produced by individual pixels includes the row/column address of the pixel, the time at which the hit occurred, and the charge of the hit. The Row field is 8 bits long and the column field is 5 bits long. The charge measured by the FE chip is given by the time-over-threshold (TOT) for the discriminator output pulse in units of the 40MHz crossing clock. This TOT field is 8 bits long. In order to measure the time and charge of the hit, each pixel contains two 8-bit SRAM cells, both of which are connected to an 8-bit wide Grey-coded bus which increments with each 25ns beam crossing. One SRAM is used to store the time of the leading edge of the discriminator pulse, and the second records the trailing edge time.

The address and timing/charge data is created by a pixel when its discriminator fires. As soon as the trailing edge of the discriminator pulse has occurred, this hit information is transferred from the individual pixel to End-of-Column (EOC) buffers at the bottom of each column pair of pixels. As the data passes through the bottom-of-column region, it is processed by a pipelined

TOT processor which converts the Grey-coded leading and trailing edge time to binary, subtracts them to get the TOT, and optionally applies a threshold or a single-crossing time slewing correction (small charges undergo more time slewing, and this can be approximately corrected by using the TOT to modify the leading edge time).

Once the hit information is stored in one of the 64 EOC Buffers at the bottom of each column pair (one for every 5 pixels in the column pair), it waits for a trigger. A second timing bus, delayed relative to the first one by a programmable latency, is used to monitor the age of each hit in the EOC Buffers. If the age is correct, and a trigger arrives, then the hit is preserved for readout. Otherwise, if the age is correct but no trigger arrives, the hit deletes itself and frees the EOC Buffer.

This mechanism allows storage of all hits in the chip until an externally generated trigger (with a fixed latency relative to the time at which the hits occurred) arrives to indicate that the hits for one particular 25ns crossing are worth reading out.

The FE chip contains a 16-word trigger FIFO that allows a given FE chip to be concurrently processing hits from up to 16 different triggered crossings. The readout controller on the FE chip will transmit the hit information from different triggers in the order those triggers arrive. The hit information associated with a particular trigger is scanned from the EOC buffers, starting with the leftmost column pair, and proceeding to the right.

The Injection Circuitry

FE-I3 has several techniques available to generate hits in the FE chips for testing purposes. The most predictable method is to use Digital Hit Injection. In this case, the FE chip has digital injection enabled (see the definition of the Global Register bits in Appendix 2). The Strobe signal is then routed to the pixel control logic, where it replaces the discriminator output from the front-end. The width of the injected strobe signal then determines the TOT of the hit injected into the column-pair readout. Note for this type of injection, if the Hitbus is enabled, it will be fired. The normal injection Select control is not used, so any pixel which is enabled for readout will have a hit injected. In this sense, the digital injection is slightly different from analog injection, where there are separate Select and Readout enables available.

The next

Finally, there is the external injection path. In this case, a pulse must be applied to the ExtInj pin of the FE chip. The high level for this signal should be VDDREF, and the step size is the magnitude of the negative step downwards from VDDREF towards AGND.

SEU-Hardening of FE-I3

FE-I3 includes significant additional circuitry to reduce the effects of SEU on the chip operation.

For the Pixel Register, where little additional space was available, the same basic SEU-tolerant latch design was used. However, the layout has been significantly changed. The layout uses an inter-digitated bit-pair to increase the distance between individual critical transistors. In addition, the layout was carefully optimized to place critical devices within one bit as far apart as possible.

This should significantly reduce the probability that one charge cluster can upset the two redundant nodes in the storage.

For the Global Register, a basic triple-redundancy scheme has been used, with two versions. One version is used in the Command Register and the 38 bits of the Global Register in the place and route Digital_Bottom block (in fact only 30 of these 38 bits are writable, and they are the only ones that are triply redundant – there is no redundancy used in the HitBus Scaler). The other version is used in the full-custom bit slice used for the remaining 193 bits of the Global Register. Functionally, the two bit slices are identical. However, there are several differences that should affect the SEU-hardness of the two designs. The full-custom slice uses a compact version of the SEU-latch for each of the three redundant storage elements. The place and route version uses a special standard cell that has a much larger physical separation between the two storage locations, and hence should have a lower upset rate. In addition, the shift register for the full-custom slice is made up of standard MUX cells, and should not have particularly good SEU-tolerance. For the place and route version, the special SEU-DFF is used, allowing us to measure the static SEU-hardness of this cell. The SEU-DFF uses a pair of SEU-latch cells in a master/slave configuration to provide improved hardness for the DFF. Finally, functionally identical logic in each bit-slice is used to create the majority-logic output, as well as a "bit-flip" signal that will flag when the three storage cells do not have identical values. When this signal is set, it indicates that the correct output is only obtained because of the majority logic correction, and there is no longer triple-redundancy. This can be used for an initial test of the circuitry, as well as a monitor of when the latches need to be re-loaded. It also allows a measurement of the SEU-hardness of the individual elements of the scheme to be measured. Finally, an overall parity is defined for the complete Global Register and Command Register combined. In the extremely unlikely event that a triple-redundant bit is ever flipped, this will flag the fact as a parity error.

In addition to hardening the storage used for the chip control, improvements have been made to harden the reset and load functions, since they are able to overwrite large amounts of data with a single SEU. For the Pixel Latches, there is no reset signal implemented, but only a load. The load is a bus connecting all 2880 latches of each type to the Command Register, and it is driven by a small buffer in the bottom of the chip in order to ensure the relatively slow risetime (much greater than 1ns) required for reliable operation of the SEU-latches. Therefore, these Pixel Latch Load lines are almost immune to SEU because they are incapable of transmitting spikes. The Global Register and Command Register bit slices implement redundant Load and Reset inputs, using the symmetries inherent in the SEU-latch. In this case, both Reset lines must be active in order to reset the triple-redundant latch, and similarly both Load lines must be active in order to load the triple-redundant latch. For the Global Register, the two Load lines are connected to the WriteGlobal1 and WriteGlobal2 command bits from the Command Register. Both bits must be set in order to write the Global Register. There are now two identical Reset Generator blocks in the new FE-I3, and both must be providing a reset in order for the Global Register to be reset. Note that this requires two independent power-on reset circuits as well. For the Command Register, there is a redundant reset coming from the redundant Reset Generators. The load for the Command Register comes from the simple address decoder used to compare the chip geographical address to the one transmitted with each command. The address decoder, and the corresponding bits for the Command Register have been completely duplicated, so that the address recognition occurs twice in parallel, and only if both address recognition circuits agree, then the Load of the Command Register takes place.

The readout circuitry of FE-I3 has been hardened in two ways beyond what was done in FE-I1. FE-I1 attempted to make sure that if bit flips did occur in critical state machines, there were no hidden states (so the chip could not hang), and that, in general, the effects would only be transient and would not require re-initialization or resetting of the chip. For FE-I3, additional steps were taken. First, the 9-bit wide Trigger FIFO used to store the TSC and Overflow information has been hardened by using a Hamming Code scheme. The FIFO has been widened to 13-bits, to include 4 Hamming code bits. This is sufficient to detect and correct all single-bit errors, and to detect, but not correct, many double bit errors. Since a bit flip in the FIFO should be a rare occurrence, this should be adequate to protect the chip operation against the majority of the SEU effects in the Trigger FIFO. Note that although the contents of the Trigger FIFO are not critical for the operation of the FE chip, the TSI provides the BCID used in tagging the event time, and these BCID are checked for consistency by the MCC during event building. Therefore, errors in the Trigger FIFO will cause the MCC to flag errors in the events, even though they are in fact built correctly. The second major improvement for SEU-hardness is the introduction of the SEU-DFF into all of the circuits used in the Digital_Bottom block. The only exception to this is the HitBus scaler. All other circuits in this block have their standard cell DFF substituted with the improved SEU-DFF. This FF has similar timing performance to the standard DFF, but it is based on an improved version of the SEU-latch implemented as a standard cell. The standard cell SEU-latch cell uses two redundant cells to store the information, just like the full-custom latch used in the pixel. However, it uses a more conventional design in which the cross-coupled inverters have their feedback broken during write (so the write does not require overcoming an inverter). The pixel latch eliminates this circuitry, and uses weak PMOS to allow the cell to be written without breaking the cross-coupled inverter feedback loop. A special DFF has been constructed by using these modified standard cell SEU-latches, and some special logic to combine the redundant outputs of the master and slave stages. This SEU-DFF has about 3 times the area of the standard DFF, but this is not a problem in the bottom of the chip. This SEU-DFF should be very SEU-tolerant, even when being clocked, and this should make all of the critical state machines, as well as the Grey Counter, and the FIFO pointer control logic very SEU-tolerant. Short of using a brute-force approach with redundant state machines and control logic, this was the simplest approach to improving the SEU-hardness of the readout logic.

Shielding Scheme

For hybrid pixel detectors, shielding of the active digital circuitry inside the pixels is critical to ensure that no digital activity is able to capacitively couple across the 10-20μ gap between the sensor and the electronics. With the use of a 5-metal (FE-I1) or 6-metal (FE-I2 and FE-I3) process, it is finally possible to implement a serious shielding scheme. However, the vendor-specified fill rules for the metal layers impose significant constraints. In particular, the requirement that a given metal layer must have no more than 70% coverage implies that shielding always requires at least two metal layers. Note that the shielding scheme used in FE-I1 has been only minimally changed in migrating to FE-I3. The extra metal layer was almost entirely consumed in providing the additional connectivity needed in the pixel front-ends for the total of 15-bits of DAC control, and larger transistor sizing for matching.

For the ATLAS Pixel FE Chip, a critical aspect of the shielding scheme is the use of a PMOS input transistor. With the particular, simple preamplifier design used here, this implies that there is very significant power-supply rejection for voltage variations on the AGND node, but rather poor supply rejection on the VDDREF node since it is connected directly to the source of the

input transistor. In order to ensure that the VDDREF net used for powering the preamplifier has the best noise immunity, we make it the reference for the entire chip (effectively, it plays the role of ground). This net is labeled VDDREF, because it is the reference VDDA for the preamplifier. It is brought out on separate power supply pads, and connected to VDDA off-chip. Thus it will be decoupled from any possible noise on VDDA by the series inductance of the FE wire-bonds. It is then natural that this reference layer would be placed as the top layer on the chip, using the thick LM metal choice. In fact, VDDREF is extended over the top of the entire FE chip, to minimize any damaging pickup between the chip and the sensor. The digital supply and return (VDD and DGND) are then buried in M3 or lower in the digital portion of the chip (column bus region). VDDA (the analog supply used to power the second stage and the discriminator) is used to cover the digital circuitry at M4, because there is very high power-supply rejection on this node. It serves as an intermediate shielding layer between the critical VDDREF, and what could be a rather noisy VDD net.

Note that the 70% maximum fill requirement for the CMOS6 process has significant implications for the shielding strategy. Basically, a large block in the middle of the pixel is allocated as the pixel latch and decoupling capacitor area, and the LM/M5 shield used over the rest of the pixel matrix descends down to M4/M3 in order to satisfy the fill rule. In this region, only M1, M2, and poly are available for circuit implementation. This region presently contains the SEU-tolerant latches, where a highly optimized layout has been used to fit into the M2 constraint and to reduce the possibility of SEU upsets.

The AGND node, which serves all of the analog front-end, has relatively good noise immunity. The VDDA net, used to supply power to the second stage and discriminator, is also quite noise immune, due to the differential designs used for these blocks. This makes the use of VDDA fairly natural for the first layer of shielding within the digital part of the pixel matrix. In addition, the high noise immunity of AGND also makes a design based on connecting AGND and DGND together fairly natural.

Appendix 1: I/O Pad Definitions for FE-I3

Here is an updated assignment of pins to pad type.

P2, p3 MonHit: propadLVDSd (LVDS output). This differential LVDS output pad pair is used to send the MonHit signal (or whichever internal signal is selected by the MONMUX) to the outside world.

P4 PowerOn: propadDigital (diodes to VDD/DGND). This special output pad is driven by a circuit that will hold the output low until a threshold voltage of about 1.4V is reached, after which it will go high. It is designed to be wire-bonded to the RSTb input pad. It serves to keep the chip in a RESET state until the digital supply voltage reaches the level where all the internal digital circuitry should be operational. At that point, it will release the RSTb pad so that the chip can operate normally. It is similar in concept to commercial Reset Generator chips.

P5 RSTb: propadInPU_RSTb (diodes to VDD/DGND + 100K pullup). This CMOS input pad is the only active low input on the FE chip. When low, it holds the FE chip in a reset state, in which all pixel hit logic, all global readout logic, the Global Register, and the Command Register are reset.

P6, p7 DshuntReg, DOverVoltage: propadDigital (diodes to VDD/DGND). These two pads contain prototype overvoltage protection circuits that use a diode for a reference to control large FET switches that can clamp overvoltages to ground. The ShuntReg pad has a nominal 2.0V threshold, and the OverVoltage pad has a nominal 2.7V threshold. These circuits are normally unconnected, and are implemented for test purposes.

P8, p9 DLinearRegOut, DLinearRegIn: propadVDDUR: These two pads provide access to a programmable linear regulator which is fully integrated with the VDD power bussing in the FE chip. This circuit has a nominal output voltage of about 1.8V, with Vtrim settings of 2.0V, 2.2V, and 2.4V. It has a nominal dropout of 400mV for a 100mA load current. If power is provided to the FE chip from the normal VDD pads, this circuit is unpowered and does nothing. If power is provided from the DLInearRegIn pad, the regulator will provide power to VDD. Extra series diodes have been added to the RegIn pad so that it should be able to withstand 4V. The RegOut pad is available for probe measurement of the regulator performance.

p10, p39 DGuard, DGrid: propadPassive (unprotected analog pad). These completely unprotected pads serve as a direct connection from the FE chip pad frame to the sensor guard ring and bias grid, once the FE chips have been bump-bonded to a sensor. The applied voltages should always be well below the inter-layer dielectric breakdown voltage for the CMOS6SF process.

p11, p38 VDDA: propadVDDA (analog power supply including transient clamp). These two pads provide the analog power to all of the analog circuitry in the FE chip with the exception of the preamplifier.

p12, p37 VDDREF: propadVREF (second analog power supply, diode protected to the first analog supply). The two pads provide analog power to the preamplifier. They would normally be connected to VDDA, with the wire-bond inductance providing additional isolation between the very sensitive preamplifier supply and the somewhat noisier standard analog supply.

p13, p36 AGnd: propadGND (analog ground). These two pads are connected to the analog ground of all of the analog circuits in the FE chip. They are also connected to the chip substrate, and the substrate in turn acts as the reference for all ESD diodes in the pad frame.

p14, p35 DGnd: propadGNDD (digital ground). These two pads are connected to the digital ground of all of the digital circuits in the FE chip.

p15, p34 VDD: propadVDDD (digital power supply, including transient clamp). These two pads provide the digital power to all circuitry in the FE chip.

p16, p17, p18, p19 GA0, GA1, GA2, GA3: propadInPU (CMOS input with pullup). These four pads provide the geographical address used for all command decoding. The pullup resistors supply a default "one" value, with wire-bonds to DGND providing "zero" values.

p20 VCal: propadAnalog (analog pad with diodes). This analog input pad is used to provide an external voltage step to the charge injection circuitry in each pixel. A voltage step from VDDA towards AGND will be applied directly to the internal injection capacitors in each pixel, when the appropriate control bits are set in the Global Register.

p21, p22, p23 CCK, DI, LD: propadInPD (CMOS input with pulldown). These three CMOS input pads provide the interface to the internal command decoder and configuration registers.

p24, p25 DO: propadLVDSd (LVDS output). This LVDS differential output pad pair provides the serial output data from the FE chip. The DOMUX bits in the Global Register determine which signal is actually transmitted, and whether the output is synchronized to the master XCK clock or not.

p26-p33 SYNC, XCK, LV1, STR: propadLVDSr (SYNC, XCK, LV1) and propadLVDSrStrong (LVDS input with no termination and 8x CMOS buffer). These LVDS input pad pairs provide the major timing and control signals to the FE chip. XCK is the 40MHz crossing clock. The other signals are levels that derive their timing from the rising edge of XCK. The LV1 signal provides LVL1 triggers to the readout circuitry to control which hits will be transferred off of the chip. The SYNC signal provides a generalized synchronous reset capability that supports three different levels of internal reset, depending on the length of the SYNC pulse. The STR signal provides the timing for the internal charge injection system. On the rising edge of the STR signal, a negative voltage step is injected into the preamplifier. The trailing edge of the STR signal has the opposite effect.

P40, p41 ALinearRegIn, ALinearRegOut: propadVDDUR: These two pads provide access to a programmable linear regulator which is fully integrated with the VDDA power bussing in the FE chip. This circuit has a nominal output voltage of about 1.5V, with Vtrim settings of 1.6V, 1.7V, and 1.8V. It has a nominal dropout of 400mV for a 100mA load current. If power is provided to the FE chip from the normal VDDA pads, this circuit is unpowered and does nothing. If power is provided from the ALInearRegIn pad, the regulator will provide power to VDDA. Extra series diodes have been added to the RegIn pad so that it should be able to withstand 4V. The RegOut pad is available for probe measurement of the regulator performance.

p42 AOverVoltage: propadAnalog. This pad contains a prototype overvoltage protection circuit that uses a diode for a reference to control large FET switches that can clamp overvoltages to ground. The nominal threshold for the circuit is 2.7V. This circuit is normally unconnected, and is implemented for test purposes.

p43, p44, p46 MonDAC, MonLeak, MonVCal: propadAnalog (diodes to VDDA/AGND). These three analog output pads allow direct measurements of internal analog signals. Using the Global Register, the MonDAC pin can be programmed to provide the output current from any of the twelve on-chip current-mode DACs, as well as the three current references, and the MonIPIL net. The MonLeak pin can be programmed to provide a mirrored copy of the compensation current in each preamplifier that is involved in the leakage current compensation. With no DC current input to the preamplifier, this node provides twice the feedback current. The HitBus control latch in each pixel also controls whether this current is multiplexed from a given pixel. Finally, the MonVCal pin can be programmed to provide a direct measurement of the voltage step applied to the charge injection capacitor in each preamplifier.

p45, p47, p48 MonDigRef, MonAmp, CapMeasure: propadDigital (diodes to VDD/DGND). These monitoring pins provide further access to the inside of the chip. The MonDigRef pin allows a direct measurement of the current reference used for the LVDS I/O drivers and receivers, without requiring any programming of the FE chip. Note however that loading this pin with a moderate resistance to ground will cause the LVDS I/O pads to stop working. The MonAmp pin can be programmed to examine the preamplifier, calibration chopper, or second stage amplifier waveforms for the pixel in the lower right corner of the active array (the so-called "test pixel"). It is driven by a large amplifier capable of driving a 100Ω termination. The amplifier and its inputs can be fully controlled from the Global Register. Finally, the CapMeasure pin is connected to an internal charge-pump capacitor measurement circuit. This circuit has 16 different test capacitors that can be measured, including in particular different numbers of copies of the key preamplifier capacitors. These capacitors are the preamplifier feedback capacitor (nominally 5fF or 10fF for the B and A versions of the FE chip respectively), the low-scale injection capacitor (nominally 5fF) and the sum of the low and high injection capacitors (nominally 40fF). The user provides a voltage of approximately 2.0V, and measures the DC current that must be sourced, as a function of the clock frequency of the charge pump. Control of this circuit is again performed using the Global Register.

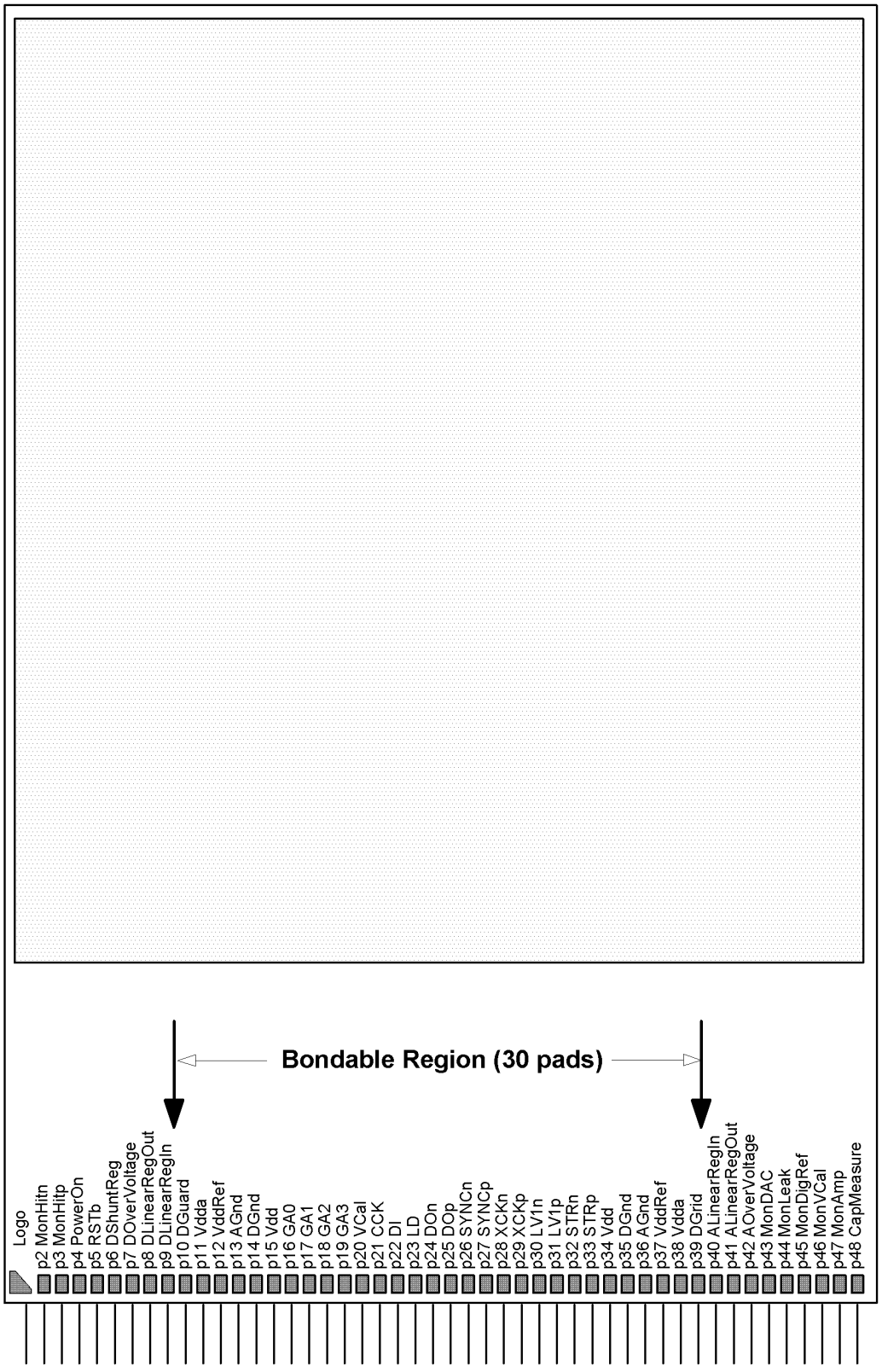


Figure 8 Geometry and Pin Definitions for FE-I3. Shaded region is active pixel area. Individual bond-pads are roughly 100μ by 200μ, and also include bump-bond pads.

Appendix 2: Register Bit Definitions for FE-I3

This is the complete and final list of all of the bits (and functions) defined for FE-I3 in the Command and Global Registers.

As we want to reset these two registers into an appropriate default state at chip power-up, all of the signals are defined to be active high, in such a way that the desired default state is represented by a low value.

Note that to take full advantage of this, unlike in earlier chips, we have implemented a PowerOn reset circuit in the chip, as well as a series of resistors that should under almost all conditions results in the chip powering up with a HardReset and a SoftReset performed. The Command and Global Register should then be powered up into the all-zero state, and the digital readout should be in a low-power configuration, with the TSI/TSC disabled, the EOC clock suppressed, and the CEU clock suppressed.

Internally, all storage cells in the Command Register and the Global Register use triple-redundancy for the latches (and the latches are already an SEU-tolerant design). Furthermore, all of these latches have two independent reset inputs and two independent load inputs. Both reset or load inputs must be active for the reset or load to succeed. The two reset inputs (used by both the Command Register and the Global Register) are created by two identical ResetGenerator blocks in FE-I3. The two load inputs for the Command Register are created by two duplicate Command Registers and Command decoders. Both Command Decoders must find an address match in order for the ChipSelect output to be valid, and for a given command to be executed by FE-I3. The two load inputs for the Global Register are created by two independent WriteGlobal command bits in the Command Register.

The order of the bits below is defined such that the MSB is the first bit shifted into the register, or equivalently, the LSB is the bit closest to the serial input of the register, which is the last bit shifted into the register.

Command Register (bit 0 = LSB):

bit 0 = **CommandParity:** this bit defines the overall parity for the Command Register contents. It should be set so that the sum of the 24 command bits is zero (there are an even number of ones in the register). The address bits (bits which are never latched into the Command Register itself) are not included in the parity sum. There is a common parity sum for the Command Register and Global Register, but there are separate Parity control bits since the registers are written separately.

bit 1 = **RefReset:** this command generates a reset signal to the LVDS I/O reference, in case there is a problem with starting this reference. Note if the reference does not start, all LVDS I/O is blocked, but the CMOS inputs to the Command Decoder will still work.

bit 2 = **SoftReset1:** soft reset for the chip, which resets all of the digital readout logic, but does not change any configuration bits. For SEU redundancy, there are now two signals, and both have to be set for the SoftReset command to execute.

bit 3 = **SoftReset2:** second strobe required to execute soft reset for the chip, which resets all of the digital readout logic, but does not change any configuration bits.

bit 4 = **ClockGlobal:** allow CCK to enter the Global Register shift register

bit 5 = **WriteGlobal1:** transfer the contents of the shift register into the SEU-latches of the Global Register. For SEU redundancy, there are now two signals, and both have to be set for the WriteGlobal command to execute.

bit 6 = **WriteGlobal2:** second strobe required to transfer the contents of the shift register into the SEU-latches of the Global Register

bit 7 = **ReadGlobal:** transfer the contents of the SEU-latches of the Global Register back into the shift register.

bit 8 = **ClockPixel:** allow CCK to enter the shift register in the pixel control block.

Note, for the following 14 load strobes, which transfer the contents of the Pixel Register into the the selected SEU-latches, the present design will not work if too many load strobes are issued at the same time. It is preferred to simply load one SEU-latch at a time to avoid problems.

bit 9 = **WriteHitbus:** the load strobe for the HitBusEnable bit in the pixel. Note this bit enables both the HitBus, the OutLeak switch, and the IPIL2Mon switch for the given pixel.

bit 10 = **WriteSelect:** the load strobe for the Select bit in the pixel.

bit 11 = **WriteMask:** the load strobe for the Mask bit in the pixel. Note that for historical reasons, the definition of this bit is ReadoutEnable (low will disable the pixel for readout).

bit 12 = **WriteTDAC0:** the load strobe for the TDAC0 bit in the pixel

bit 13 = **WriteTDAC1:** the load strobe for the TDAC1 bit in the pixel

bit 14 = **WriteTDAC2:** the load strobe for the TDAC2 bit in the pixel

bit 15 = **WriteTDAC3:** the load strobe for the TDAC3 bit in the pixel

bit 16 = **WriteTDAC4:** the load strobe for the TDAC4 bit in the pixel

bit 17 = **WriteTDAC5:** the load strobe for the TDAC5 bit in the pixel

bit 18 = **WriteTDAC6:** the load strobe for the TDAC6 bit in the pixel

bit 19 = **WriteFDAC0:** the load strobe for the FDAC0 bit in the pixel

bit 20 = **WriteFDAC1:** the load strobe for the FDAC1 bit in the pixel

bit 21 = **WriteFDAC2:** the load strobe for the FDAC2 bit in the pixel

bit 22 = **WriteKill:** the load strobe for the Kill bit in the pixel. Note the polarity of the Kill bit has been changed from FE-I1 (active = Kill) to FE-I2 and FE-I3 (active = EnablePreamp).

bit 23 = **ReadPixel:** the control for shift/readback in the pixel control block. Clearing this bit leaves the Pixel Register in Shift mode, so data can be shifted through. Setting this bit puts the Pixel Register in Readback mode, where the next CCK will cause the present contents of the selected pixel control bit to be latched back into the Pixel Register. The usage of this mode is peculiar. The recommended approach is to first issue a **ReadPixel** and **ClockPixel** command together, with the relevant load strobe, e.g. WriteTDAC0, and with DCNT=1. This should result

in the data of interest being latched back into the Pixel Register. After this, the usual ClockPixel command with DCNT=2880 and **ReadPixel** off again should allow the data to be clocked out. It is possible that the readback mechanism will not be fast enough to work in this way. In this case, it should be sufficient to issue two **ReadPixel+ClockPixel** commands in a row, each with DCNT=1. This will give the latch readback circuit a very long time to settle.

The total is 24 bits in the Command Register, not including the 5 address bits.

Global Register (bit 0 = LSB):

All bits in the Global Register are listed in order with the LSB = bit closest to the shift register input, as Bit 0. In general, column pairs in the chip are numbered from left to right, and from 0 to 8. The locations of the circuitry containing the bits are also given. Some bits are located in the synthesized block at the bottom of the chip, some are implemented in special analog blocks in the bottom of the chip, and the majority of the bits are located underneath the "analog column pairs" (bump-pad region). For reference, these "analog column pairs" are numbered from 1 to 10 from left to right.

Location = synthesized block in bottom of chip:

bit 0 = **GlobalParity:** this bit defines the overall parity for the Global Register contents. It should be set so that the sum of the 222 writable Global Register bits is zero (there are an even number of ones in the register), ignoring the 9 read-only bits which are not included in the parity check. There is a common parity sum for the Command Register and Global Register, but there are separate Parity control bits since the registers are written separately.

Reg(1:8) = **Latency(0:7):** program the delay, in beam crossing units, between the TSI timestamp sent to the pixel, and the TSC timestamp sent to the EOC buffers. The value 0 should represent a latency of 256 crossings.

Reg(9:12) = **SelfTriggerDelay(0:3):** a 4-bit field to program the delay used by the self-trigger circuitry before generating an internal LVL1 signal. The delay used is the value of this field times 16 (1 gives 16 crossing delay, 2 gives 32 crossing delay, 15 gives 240 crossing delay). FE-I1 was a sub-set of FE-I3, with this field fixed to 4 (64 crossings of delay).

Reg(13:16) = **SelfTriggerWidth(0:3):** a 4-bit field for the width of the internally generated L1 signal in self-trigger mode. The width is specified in beam crossing units from 0 to 15 (a value of 0 gives a width of 1 crossing, and 15 gives 16 crossings).

Reg(17) = **EnableSelfTrigger:** Enable the Self-Trigger circuit to generate LVL1 triggers automatically whenever the HitBus fires.

Reg(18) = **EnableHitParity:** enable generation of HitParity. The HitParity is stored in TOT<7>, and is defined so that the sum of all bits (including the HitParity itself) in Hit<20:0> should be zero. Additional bits are not included because they are discarded by the MCC during event building. The initial parity calculation is performed in the TOT processor, and includes

TOT<6:0> and Addr<8:0> (16 bits). When the data is transferred to the serializer, the HitParity is incrementally updated to include the full 13-bit address information (Hit<20:0> bits are all part of the HitParity). If a parity error occurs in the EOC buffers, this algorithm should preserve the error condition. These are the only bits that are passed through the MCC to the final output stream, and hence the only ones used in this check. If EnableHitParity is not set, then TOT<7> is used as a TOT bit just like in FE-I1.

Finally, if EnableHitParity is set, the HitParity is checked for all hits in a given event, and a ParityError is stored in the EOE Flag to indicate if a parity error has occurred. Note that this overall parity check does not include the EOE word. The EOE word has its own EOEParity bit, which is also controlled by the EnablehitParity.

Reg(19:22) = **Select_DO(0:3):** define which of 16 inputs is multiplexed out through the DO pins (DOMUX). The first 8 inputs are Direct and the second 8 inputs are synchronized to XCK with a DFF, just as in FE-D.

0 = RegClkIn, buffered CCK, gated for entry to Global Register

1 = HitBus

2 = Softreset1B, Inverted SoftReset1 signal

3 = SerData, data from digital readout of chip

4 = MonSel, Chip select status

5 = PixClk1, CCK, input to 2-phase clock for Pixel Register

6 = PixClk2, CCK, input to 2-phase clock for Pixel Register

7 = HardReset1bB, inverted HardReset1 signal

8 = SerData, data from digital readout of chip

9 = SerOutMain, output data from Command Register

10 = ReadFIFO, output from readout controller to read FIFO

11 = SerPix, output data from Pixel Register

12 = Accept, internal LVL1 signal for EOC control

13 = ROCK, internal readout clock for data transfer from EOC

14 = SerOutReg, output data from Global Register after place/route block (first 38 bits).

15 = GlobalOut, output data from Global Register after bottom of column.

Reg(23:26) = **Select_MonHit(0:3):** identical to Select_DO, except for the MonHit output pins.

Reg(27) = **TSI/TSC Enable:** Enable bit for the buffers on the output of the Grey Counter. When this bit is cleared, the TSI and TSC distribution to the column pair and EOC buffers is suppressed in order to reduce digital power consumption to a minimum.

Reg(28) = **SelectDataPhase:** In FE-I3, this bit selects whether the output data on DO changes on the rising edge of XCK or on the falling edge of XCK. The default value (0) corresponds to the previous convention used for FE-I1 and FE-I2 that the data changed on the rising edge of XCK. As this has the potential to cause race conditions at the MCC, setting this bit to 1 clocks the output DO with XCKbar so the data changes on the falling edge of XCK, and maximizes the timing margin available for data transfer from the FE chip to the MCC. This bit is a spare bit in FE-I2 and will be ignored.

Reg(29) = **EnableEOEParity:** In FE-I2, a single bit, EnableHitParity enabled the generation of the HitParity bit, which replaces the most-significant bit of the TOT<7:0> field, as well as the EOEParity bit which performs an equivalent function for the EOE word. However, due to mis-implementation of the check function in MCC-I2, any time the EOEParity bit is set in an EOE word, the MCC will flag this as an error condition (and due to an additional mistake, this is the one FE error condition which cannot be masked in the MCC-I2). Therefore, in order to avoid generating error flags for 50% of all EOE words, it is necessary to mask the EOEParity bit in the EOE word, while still allowing the rest of the HitParity machinery to work normally. This is now achieved in FE-I3 by setting the EnableHitParity bit and clearing the EnableEOEParity bit. This bit is a spare bit in FE-I2 and will be ignored.

Reg(30-37) = **HitBusScaler:** FE-I3 implements a HitBus scaler for location of hot pixels. This is an 8-bit scaler that is reset by WriteGlobal, and clocked by HitBus. The Hitbus increments the scaler only during the time when Strobe is active. The scaler output then appears as eight read-only bits in the Global Register. Note also that since these are readonly bits, they are not included in the parity chain or parity calculation for the Global Register, nor do they use SEU-hardened DFF.

Location = analog blocks at bottom of chip:

Reg(38:51) = **MonLeak ADC circuitry**. This is a simple circuit to digitize MonLeak over a range from 0.125nA to 128nA. A 10-bit current mode DAC with 0.5uA LSB (511uA full-scale) is used to drive a current mode comparator. The DAC is divided by 20 and the leakage current is multiplied by 200. The comparator status (on/off) is presented in a read-only bit in the Global Register. The group of pixels to monitor should be controlled by the HitBusEnable FF in each pixel. Note that the read-only register bit is NOT included in the overall parity check and sum for the Global Register.

MonLeakADC(0) = MonADCRefTest, control MUXing of reference monitor point to the global MonDAC pin.

MonLeakADC(1:10) = MonADCDAC, setting for 10-bit MonLeak DAC

MonLeakADC(11) = MonADCDACTest, control MUXing of DAC monitor point to the global MonDAC pin.

MonLeakADC(12) = EnableComparator, enable operation of current mode comparator. Note that this bit also disables the connection of the OutLeak current to the MonLeak pad.

MonLeakADC(13) = MonComp, read-only register bit containing the status of the MonLeak comparator.

Reg(52-53) = **ARegTrim:** Trim bits for the analog regulator output voltage. These bits set the nominal Areg output voltage to: 0 = 1.5V, 1 = 1.6V, 2 = 1.7V, and 3 = 1.8V. Note that this regulator is internally connected to power the VDDA net. The VDDREF net still needs to be externally connected to VDDA for the FE-I3 to operate properly.

Reg(54) = **EnableARegMeas:** Enable measurement path for the analog regulator output voltage. This output is multiplexed to the MonVCal pad

Reg(55-56) = **ARegMeas:** Select measurement for the analog regulator output voltage. The possible measurements are: 0 = internal regulator output, 1 = internal input to error amplifier, 2 = internal bandgap reference output, 3 = internal regulator ground.

Reg(57) = **EnableAReg:** Overall enable for the analog regulator output voltage.

Reg(58) = **EnableLVDSReferenceMeas:** Enable MUX for LVDS Reference output to MonDAC pad for measurement.

Reg(59-60) = **DRegTrim:** Trim bits for the digital regulator output voltage. These bits set the nominal Dreg output voltage to: 0 = 1.8V, 1 = 2.0V, 2 = 2.2V, and 3 = 2.4V.

Reg(61) = **EnableDRegMeas:** Enable measurement path for the digital regulator output voltage.

Reg(62-63) = **DRegMeas:** Select measurement for the digital regulator output voltage. The possible measurements are: 0 = internal regulator output, 1 = internal input to error amplifier, 2 = internal bandgap reference output, 3 = internal regulator ground.

Reg(64:69) = **CapMeasure Circuitry:** control bits to operate the charge pump capacitance measurement circuit for C(inj low), C(inj high), and C(FB). There are 4 select bits to chose one of 16 structures to measure the capacitance of. There are 2 frequency bits to control the non-overlapping clock generated from the 40MHz XCK. Values of XCK/4, XCK/8, XCK/16, and XCK/32 are possible.

Recall that the structure of the input pad is the following. M1+M3+M5 plates are all connected to the preamp input. The C(lo) capacitor is in M2. The C(hi) capacitor is implemented in poly, M2, and M4. The C(FB) capacitor is in M4. The poly plate has large dimensions to improve the shielding of the input plates from the substrate when not in calibration mode. The M2 and M4 plates are completely surrounded by the overhanging M1/M3/M5 plates to ensure that almost the entire fringe contribution is included into C(lo), C(hi), and C(FB).

C(lo) measurement technique: input to CapMeasure is the C(lo) capacitor. The rest of the structure (C(hi)+C(FB)+input plates) is grounded. The error in this technique is that the test structure measurement includes the C(lo)-C(hi) sidewall parasitic, whereas the injection circuit in FE-I is not sensitive to this. The gap between the C(lo) and the C(hi) plate was increased to reduce the magnitude of this error.

C(lo)+C(hi) measurement technique: input to CapMeasure is the C(fb) and input plates, and C(lo)+C(hi) are grounded to avoid having the very large poly-substrate capacitance appear as a stray capacitance for the test structure measurement. The error in this technique is that the test

structure measurement includes the C(FB)-C(hi) sidewall parasitic, whereas the injection circuit in FE-I is not sensitive to this. However, in FE-I, this parasitic will couple some of the charge injected with C(hi) directly to the preamp output. The gap between the C(FB) and the C(hi) plate was increased to reduce the magnitude of this error.

C(FB) measurement technique: input to CapMeasure is the C(FB) capacitor. The rest of the structure (C(lo)+C(hi)+input plates) is grounded. The error in this technique is that the test structure measurement includes the C(FB)-C(hi) sidewall parasitic, whereas the feedback circuit in FE-I is not sensitive to this. The gap between the C(FB) and the C(hi) plate was increased to reduce the magnitude of this error.

CapMeasure(0:3) = selection of device to measure:

DUT0: Empty for parasitic check

DUT1: n=4 for C(lo)

DUT2: n=2 for C(lo)

DUT3: n=1 for C(lo)

DUT4: Empty for parasitic check

DUT5: n=0 for C(lo)

DUT6: n=4 for C(FB)

DUT7: n=2 for C(FB)

DUT8: Empty for parasitic check

DUT9: n=1 for C(FB)

DUT10: n=0 for C(FB)

DUT11: n=4 for C(hi)+C(lo)

DUT12: Empty for parasitic check

DUT13: n=2 for C(hi)+C(lo)

DUT14: n=1 for C(hi)+C(lo)

DUT15: n=0 for C(hi)+C(lo)

CapMeasure(4:5) = selection of clocking speed

0 = XCK/32

1 = XCK/16

2 = XCK/8

3 = XCK/4

The input to the following register bits is connected to the output of the previous register, so the following Reg(0) is effectively Reg(70) of the previous register.

Note on EnableCol bits:

The single bit for each column pair controls the following related functions. First, it bypasses the Pixel Register for a given column pair (shortening the register by 320 locations). Second, it blocks the contribution of the HitBus for a given column pair to the global chip OR of the HitBus. Third, it blocks participation of the given Column Pair in the horizontal sparse scan at the bottom of column used to transfer the hits to the output serializer. Fourth, it blocks the output of the Overflow flag for the EOC buffers in a given column pair from contributing to the overall Overflow flag written into the EOE word. Fifth, it turns off the XCK used by the EOC buffers to run their state machines, effectively reducing the power consumption for the given EOC buffer block to a small value. Sixth, it blocks participation of the column pair in the MonLeak current summing, so that defective column pairs are prevented from supplying large currents which obscure the signal of interest.

Location = analog column 10:

Reg(0) = **EnableCapTest:** The capacitors are controlled by the CapTest signal. When this signal is high, it places all of the internal smart decoupling caps into a "test" state, in which even if they are shorted, they will draw no more than about 10nA from VDD. This effectively disconnects these capacitors. The CapTest signal is connected to a CMOS pad with pullup, so that its default state is to be high (disabling caps). An NMOS pass transistor is connected to CapTest, and controlled by the EnableCap Global Register bit. When the register is set, this enables the capacitors (disables CapTest), but the power-on state should always have the capacitors disabled.

Reg(1) = **EnableAnalogOut:** enable for the 50ohm buffer driving the test pixel signals off-chip. When the buffer is not enabled, it should consume a small amount of current (less than 1mA).

Reg(2:3) = **TestPixelMUX:** 2-bit input selection for the 50-ohm buffer. This circuit multiplexes the test points from the test pixel located at the lower right of the matrix (col 17 row 0).

0 = buffer chopper output

1 = buffer preamplifier output

2 = buffer second amplifier output

3 = buffer second amplifier inverted output

Reg(4) = **EnableVCalMeas:** set to enable VCal from internal DAC to MonVCal pad

Reg(5) = **EnableLeakMeas:** set to enable OutLeak from internal net to either MonLeak pad or MonLeak ADC. If this bit is set and the enable for the MonLeak Comparator is disabled, the OutLeak net goes to the MonLeak pad. If the comparator is enabled, the OutLeak net goes to the comparator but is disconnected from the output pad.

Reg(6) = **EnableBufferBoost:** set to enable doubling the 50-ohm buffer nominal bias current.

Location = analog column 9:

Reg(7) = **EnableCol8:** set to enable column pair 8 operation

Reg(8) = **TestDAC for IVDD2 DAC:** set to send this current to MONDAC pad

Reg(9-16) = **IVDD2 DAC** setting. The mirror for this DAC reduces the current by a factor 240, giving a default of 250nA for 64 DAC counts.

Reg(17-24) = **ID DAC** setting. The mirror for this DAC reduced the current by a factor 12, giving a default of 5.3μA for 64 DAC counts.

Reg(25) = **TestDAC for ID DAC:** set to send this current to MONDAC pad

Location = analog column 8:

Reg(26) = **EnableCol7:** set to enable column pair 7 operation

Reg(27) = **TestDAC for IP2 DAC:** set to send this current to MONDAC pad

Reg(28-35) = **IP2 DAC** setting. The mirror for this DAC reduces the current by a factor 16, giving a default of 4μA for 64 DAC counts.

Reg(36-43) = **IP DAC** setting. The mirror for this DAC reduces the current by a factor 8, giving a default of 8μA for 64 DAC counts.

Reg(44) = **TestDAC for IP DAC:** set to send this current to MONDAC pad

Location = analog column 7:

Reg(45) = **EnableCol6:** set to enable column pair 6 operation

Reg(46) = **TestDAC for ITrimTh DAC:** set to send this current to MONDAC pad

Reg(47-54) = **ITrimTh DAC** setting. The mirror for this DAC reduces the current by a factor 3200, giving a default of about 20nA for the TDAC LSB for 64 DAC counts.

Reg(55-62) = **IF DAC** setting. The mirror for this DAC reduces the current by a factor of 8000, giving a default of 8nA for 64 DAC counts. Note this is eight times larger than for FE-I1.

Reg(63) = **TestDAC for IF DAC:** set to send this current to MONDAC pad

Location = analog column 6:

Reg(64) = **EnableCol5:** set to enable column pair 5 operation

Reg(65) = **TestDAC for ITrimIf DAC:** set to send this current to MONDAC pad

Reg(66-73) = **ITrimIf DAC** setting. The mirror for this DAC reduces the current by a factor 64000, giving a default of 1nA for the FDAC LSB at 64 DAC counts.

Reg(74-83) = **VCal DAC** setting - NOTE this is a special 10-bit DAC with 0.5uA LSB and 511uA full-scale. A 1:1 mirror is used to apply the DAC current across a 1.67K resistor to VDDA. This gives a full-scale Vstep of roughly 850mV, and an LSB of roughly 0.84mV, or half the nominal value of the LSB for FE-I1.

Reg(84) = **TestDAC for VCal DAC:** set to send this current to MONDAC pad

Location = analog column 5:

Reg(85) = **EnableCol4:** set to enable column pair 4 operation

Reg(86) = **High injection cap selection**. If low, injection uses the low injection cap only. If high, both the low and high value injection caps are used.

Reg(87) = **EnableExtInj:** enable external injection using dedicated Vcal pad. This enables the injection of an analog step through the VCal pad, and directly into the selected pixels. The

behavior should be as for internal injection, where the Select bit in each pixel enables charge injection and the High/Low bit defines which injection capacitors are used. Note, there is no blocking mechanism for injection through the normal internal path when in this mode, except by the absence of STR. If STR is also sent, a second charge injection will occur.

Reg(88) = **Test Analog Reference:** set to send this current to MONDAC pad

Reg(89-90) = **EOC MUX control:** This controls which data the CEU passes on to the EOC buffers for storage in the TOT field of the hit data. The MUX of LE and TE information allows full verification of all storage bits in the pixel RAMs during chip testing, without the need to generate special values of TOT.

0 = Write TOT information into EOC buffers

1 = Write LE information from hit in column into EOC buffers

2 = Write TOT information into EOC buffers

3 = Write TE information from hit in column into EOC Buffers.

Reg(91-92) = **CEU Clock Control:** The CEU clock controls the speed of operation of the column pair readout.

0 = turn CEU clock off to save power

1 = CEU clock = 10MHz (5MHz column transfer rate)

2 = CEU clock = 20MHz (10MHz column transfer rate)

3 = CEU clock = 40MHz (20MHz column transfer rate)

Location = analog column 4:

Reg(93) = **Enable Digital Injection:** enable for passing the Strobe signal directly into the pixel hit logic for hit injection. When disabled, this will block the Strobe from going up the column to the digital injection circuit, in order to reduce any extra noise injected by this additional strobe. When enabled, the Strobe and Strobebar for the analog injection are not disabled, since digital injection should not be affected by the additional analog injection.

Reg(94) = **EnableCol3:** set to enable column pair 3 operation

Reg(95) = **TestDAC for ITH1 DAC:** set to send this current to MONDAC pad

Reg(96-103) = **ITH1 DAC** setting. The mirror for the DAC reduces the current by a factor of 60, giving a default value of about 1μA for 64 DAC counts.

Reg(104-111) = **ITH2 DAC** setting. The mirror for the DAC reduces the current by a factor of 100, giving a default value of about 0.6μA for 64 DAC counts.

Reg(112) = **TestDAC for ITH2 DAC:** set to send this current to MONDAC pad

Location = analog column 3:

Reg(113) = **EnableCol2:** set to enable column pair 2 operation

Reg(114) = **TestDAC for IL DAC:** set to send this current to MONDAC pad

Reg(115-122) = **IL DAC** setting. The mirror for the DAC reduces the current by a factor 42, giving a default value of 1.5μA for 64 DAC counts.

Reg(123-130) = **IL2 DAC** setting. The mirror for the DAC reduces the current by a factor 21, giving a default value of 3μA for 64 DAC counts.

Reg(131) = **TestDAC for IL2 DAC:** set to send this current to MONDAC pad

Location = analog column 2:

Reg(132) = **EnableCol1:** set to enable column pair 1 operation

Reg(133-140) = **THRMIN**, 8-bit minimum threshold register for CEU TOT processor

Reg(141-148) = **THRDUB**, 8-bit minimum threshold register for CEU hit doubling

Reg(149-150) = **ReadMode**, 2-bit control field:

0 = send hits to the EOC in the usual way

1 = apply THRMIN threshold to TOT value for each hit and only write those hits to the EOC which have TOT greater than THRMIN.

2 = for hits with TOT less than or equal to THRDUB, the hit will be sent twice to the EOC. One hit has the original LE timing information, and one hit has the LE timing information for the previous beam crossing. The CEU generates one cycle of wait state for the column readout in order to write twice to the EOC.

3 = perform both of the above operations

Location = analog column 1:

Reg(151) = **EnableCol0:** set to enable column pair 0 operation

Reg(152) = **HitBusEnable:** Enable bit for the Hitbus receiver blocks at the bottom of each column, and in the middle of the bottom of column region for the whole chip (19 circuits total). When this bit is turned on, each receiver with its input not active draws about 200μA from the digital supply (about 4mA total). Each receiver that has its input active draws about 400μA from the digital supply (about 8mA total). Since each pixel already has its own enable FF for the Hitbus, this global bit is provided mainly for power management.

Reg(153-157) = **GlobalTDAC:** 5-bit global threshold DAC setting. This value is transmitted via a global bus to all of the individual GDACs in each pixel.

Reg(158) = **EnableTune:** Enable automatic threshold tuning circuit.

Reg(159) = **EnableBiasCompensation:** Enable automatic bias voltage drop compensation circuit.

Reg(160) = **EnableIPMonitor:** Enable summing of IP or IL2 current onto MonIP node.

The total length of the Global Register is 70 + 161 = 231 bits in FE-I3.

Appendix 3: Data Output Formats for FE-I3:

This is a short description of the data formats produced by FE-I3. Note that in order to get data from the chip, the Global Register must be used to select one of the DOMUX positions in which useful data can be transmitted.

These settings are:

1) **Command Register output** (DOMUX=9):

Note that the Command Register is 29 bits long. The MSB is shifted in first, and hence will be the first bit out of the DOMUX. This register operates on the CCK clock, and output data will be valid on the first rising XCK edge after the rising CCK edge.

The format is:

MSB LSB

| ReadPixel | ..... | CommandParity | BCast | GA3 | ... | GA0 |

The LD signal must go high after the LSB of the Command Register is sent, indicating that any subsequent bits are to be interpreted as data and not command information.

2) **Global Register output** (DOMUX=15):

The Global Register is a complex register consisting of an input shift register and an associated SEU latch. The data contained in the input shift register only takes effect when it is loaded into the SEU latches by the WriteGlobal1 and WriteGlobal2 control bits in the Command Register. Data from the Global Register can be shifted out using the ClockGlobal command. A ReadGlobal command (with no data words) would normally be sent first in order to transfer the information from the SEU latches used for storage into the shift register used for readback. The length of the Global Register is 231 bits, so the data portion of the ClockGlobal command should have LD high for 231 CCK cycles. The data is shifted in with the MSB first, and hence the MSB is the first bit out of the DOMUX. In contrast to the Command Register, valid data will only appear after the 29 CCK of the command have been issued, and the LD signal goes high.

The format is:

MSB LSB

| EnableIPMonitor | ..... | GlobalParity |

3) **Pixel Register output** (DOMUX=11):

This register snakes through each individual pixel, starting from the input at the lower left corner to the output at the lower right corner of the matrix. It is a 2880-bit shift register. The contents of this register can be transferred into selected SEU latches in each pixel control block using the Loadxxx control bits in the Command Register. The individual SEU latches can also be read back into the Pixel Register using the Loadxxx signals and the ReadPixel control bit on the Command Register. Note that the Pixel Register is a simple shift register, and is not cleared by the SoftRest or HardReset signals.

The format is:

MSB LSB

| row0col17 | ... | row 159col17 | ... | row159col0 | ... | row0col0 |

4) **Event Data output** (DOMUX=8):

Event Data consists of Hit Words and End-of-Event Words (EOE words). Each word is 26 bits long, and always starts with a single header bit.

The format of the Hit Words is (HitParity not enabled):

MSB LSB

| Header | BCID<3:0> | Row<7:0> | Col<4:0> | TOT<7:0> |

Here, BCID is the 4 LSB of the timestamp used for the trigger comparison (TSC). This will be LSB of the binary equivalent of the initial 8-bit grey-code timestamp (TSI) when the hits for this event were recorded in the pixels. Note that this is a format change from earlier chips, which returned the L1ID instead. The BCID is more useful for the MCC to use in detecting possible synchronization errors between different chips in a module.

The format of the Hit Words is (HitParity enabled):

MSB LSB

| Header | BCID<3:0> | Row<7:0> | Col<4:0> | HitParity | TOT<6:0> |

Here, The HitParity bit is calculated so that the sum of the bits in the Row, Col, TOT and HitParity fields is zero (even number of ones present). The HitParity is calculated in two steps. The first is carried out in the TOT processor when the hit is created, and includes the TOT field, the ROW field, and the left/right Column information. The data is then stored in the EOC buffers. When the hit is being transferred to the serializer, the HitParity is incrementally updated using the final Column address (any errors which occurred in the EOC buffer should be preserved). Note that since operation in ATLAS would not normally involve latencies larger than 3.2μs, the use of the MSB of the original TOT field should not result in the loss of any useful information.

The format of the EOE Words is (HitParity disabled):

MSB LSB

| Header | BCID<3:0> | Flag<7:0> | 0 | L1ID<3:0> | BCID<7:4> | Warn<3:0> |

or (HitParity enabled):

MSB LSB

| Header | BCID<3:0> | Flag<7:0> | EOEParity | L1ID<3:0> | BCID<7:4> | Warn<3:0> |

Here, Flag has the value of 'F0'x for the case of an error free event. It has the value 'En'x for the case where an error has occurred. The error condition is flagged if any of the Error bits in the Flag field are set, or if any of the Warning bits in the Warn field are set.

The defined errors for FE-I3 include:

n = 1: EOC Buffer Overflow condition was detected at the time the L1 trigger was issued for this event. Note that this condition exists if some time in the previous 256 beam crossings, a request was made to write into an EOC buffer that was the last free EOC buffer in some column pair. The presence of this flag only indicates that hits might have been lost from the present event, not that they were lost due to a real buffer overflow.

n=2: Hamming Code error was detected in decoding the data from the Trigger FIFO. This FIFO contains 9 bits of data (TSC timestamp for a given trigger, and EOC Buffer Overflow error flag status at the time of the trigger). An additional 4-bit error correction field is included (Hamming code), making the actual FIFO 13-bits wide. These correction bits are generated at the time the Trigger FIFO is written, and then decoded at the time the FIFO is read. This 4-bit code allows all single-bit errors to be corrected. If more than one bit is flipped, then the algorithm will fail to properly correct the data. The error flag is set any time a bit-flip is detected. If it is a single bit-flip, the data should be properly corrected, and the error can be ignored.

n=4: Command/Global Register Parity Error was detected at the time of data serialization. This parity check is performed by a running OR throughout the combined Command and Global Register. The Command Register calculation is done for the 24

real command bits. The Global Register calculation ignores the 9 read-only bits that exist (MonLeakADC readback and 8-bit HitBus scaler readback). Note that independent control of the parity of the Command and Global Registers is implemented as the first bit in each register. The parity should always be set so that the sum of all ones in the register, including the parity bit, is zero (even number of ones present).

n=8: HitParity errors were detected while transmitting the current event. While each hit for a given event is being transmitted, the HitParity is recalculated. An error is flagged if the parity is not even in any of the hits belonging to the current event (excluding the EOE itself). Note that this calculation is only performed using the HitParity from the TOT processor (TOT<6:0> and Addr<8:0> = Row plus left/right column), because the additional parity information for the full Column field is only inserted in each hit as it is transmitted by the serializer. Therefore, this check will detect errors occurring in the EOC Buffer storage. The check is an OR of the individual parity check for each hit, and so any number of errors greater than zero will cause a single parity error result. Also note that this check does not include the EOEParity. Finally, note that by default, the HitParity check is disabled, and so this error cannot occur, and the HitParity field in each hit will be filled by TOT<7>, and the EOEParity field in the EOE word will be set to zero. Enabling the HitParity check in the Global Register will enable all of the actions above.

Warn=1: BitFlipError was detected at the time of data serialization. There is a running OR chain of the EXOR of the three latches in each triple-redundancy storage cell of the Command Register and the Global Register. If any one of these storage cells has an inconsistency in its three internal latches, this error will be set. Note that if the inconsistency is only caused by a single latch flip, then it will be properly corrected by the majority logic. However, at this point there is no remaining redundancy left in the storage cell, so any further upsets will cause a real error. It is best to re-write the corresponding registers relatively soon to clear this condition.

EOEParity is calculated just like HitParity. It includes EOE<20:0>, which is everything except the BCID and the header. It is calculated at the last moment, after all of the error information has properly settled.

L1ID is the value of the trigger FIFO pointer used to store this event. This pointer starts at 0 after a SYNC reset, and then increments by one for each new L1 trigger seen by the FE chip. It must have a unique value for each of the 16 possible events that can be stored at the same time in an FE chip (something which is not true of the BCID).

BCID<7:0> is the 8-bit binary timestamp used for the trigger comparison (TSC). This will be the binary equivalent of the initial 8-bit grey-code timestamp (TSI) when the hits for this event were recorded in the pixels. It starts from 0 after a SoftReset clears the Grey counter, and increments by one each beam crossing (XCK period).

Appendix 4: Operation of Auto-tuning for FE-I3:

This section gives a brief overview of the new auto-tune circuit in each pixel in FE-I3, and how it should be operated.

The auto-tune circuit block is a small collection of circuits implemented in each pixel to optimize the process of finding the TDAC value that sets the threshold as close as possible to a target threshold. In order for it to work properly, it is necessary that the threshold is a monotonic function of the TDAC value, since the auto-tune will choose the highest TDAC value for which the pixel threshold is less than or equal to the target threshold (actually for which the pixel disriminator on-fraction is larger than 50%).

The auto-tune block is based around a 5-bit up-down counter, which is either incremented or decremented by one each time a Strobe is issued. If the discriminator fires at least once while the Strobe is active, this will cause the up-down counter to increment. Otherwise, it will decrement. The counter is preset to its mid-point (MSB only is set), so if the discrimiantor fires more than 50% of the time for a large number of strobes, then the MSB will remain set. Otherwise, the MSB will be cleared. The status of the up-down counter MSB defines whether a pixel with a given TDAC setting is above or below threshold.

The auto-tune circuit is integrated closely with the pixel control section, to allow it to modify the behavior of the pixel when it is operated in auto-tune mode. In particular, the auto-tune circuitry (only when auto-tune mode is enabled) is able to block any subsequent writes to the latches for the given pixel, and hence freeze its configuration.

Operating sequence:

1. Set the VCal for the chopper to inject a charge corresponding to the target threshold for the threshold tuning.
2. Disable the Readout for all pixels to avoid producing any data, which will generate additional digital noise. It would also require slowing down the strobe rate of the auto-tune scan to allow transfer of the data.
3. Disable the Hitbus for all pixels as well, as it is not needed for auto-tuning.
4. Disable Auto-tune in the Global Register.
5. Set the Select for all pixels that should participate in the auto-tune scan. In principle, this could be all pixels in a given FE chip, or it could be a subset corresponding to some mask stage, depending on the stability of the FE chip during auto-tuning.
6. Clear the Kill bit (write EnablePreamp = 1) for all pixels that should participate in the auto-tune scan, and set the Kill bit (write EnablePreamp = 0) for all other pixels. Note that in Auto-tune enable mode, all write access to the pixel latches is blocked, in order to prevent the TDAC values from being overwritten during the auto-tune scan.
7. Enable Auto-tune mode in the Global Register.
8. Load the TDACs for the given iteration of the auto-tune. When first starting the scan, the TDACs are all loaded to their maximum value, corresponding to the maximum threshold. Note that by setting the LoadTDAC0 strobe, the up-down counter in each pixel used to record the state of the auto-tuning is automatically preset to its mid-

point (only the MSB is set). This is required before each new iteration in the auto-tune. For each new iteration, the TDACs should all be reloaded with the next lower TDAC value. Note that this code can use an optimized algorithm for writing the TDACs because all TDACs are being set to the same value. For example, one could load the Pixel Shift Register with all zero's, and then issue LoadTDACn for all those bits that should be set to zero. The Pixel Shift Register can then be set to all one's, and again LoadTDACn issued for all bits that should be set to one. Note it is best to issue only one LoadTDACn at a time to ensure there are no loading problems in writing the SEU-latches.

9. Issue order of 100 Strobes. The interval between strobes can be set by the need for the FE to settle from the wrong-sign pulse created by the internal strobe. An interval of order 20μs should be adequate (TurboDAQ interval = 50), provided that the strobe width is set accordingly (to about half of the interval) (TDAQ width of 500). For each case where the discriminator in a given pixel fires, the up-down counter will count up. Otherwise, it will count down.
10. Issue a LoadKill strobe in order to store the final state of the up-down counter into the Kill latch. If a pixel is above threshold, then it is expected that after a reasonable number of strobes, the up-down counter will still be above its mid-point (MSB set). If the MSB is set, then the Kill bit will also be set. While the auto-tune mode is active, if the Kill bit is set, this will in turn block any attempts to overwrite the other latches in the pixel. In particular, this means that the TDAC value will be left at the value for which the Kill bit first became set, because further writes to these latches are blocked.
11. Keep looping over the last three steps (8, 9, and 10) until the TDAC value has been decremented down to zero.
12. Keep looping from step 4 onwards over all mask stages used to build up the complete scan. Steps 4, 5, and 6 are the mask staging, which must be done with Auto-tune disabled in order to access the pixel latches.
13. Disable the auto-tune mode, and read back the TDAC values for each pixel. The value for a given pixel will correspond to the setting for which the discriminator first fired more than 50% of the time. At this time, all of the Kill bits and other latch bits should also be re-written to useful values. The TDACs do not need to be loaded, as they are already set to the correct values, so an immediate verification threshold scan can be performed.

Appendix 5: Finding Hot Pixels and Stuck-on Pixels for FE-I3:

This section gives a brief overview of the use of the HitBus Scaler circuit and the Auto-Tune circuit to identify pixels with high occupancy in an FE-I3 module.

Finding Hot Pixels:

The HitBus Scaler is a circuit block intended to allow measuring pixels firing on noise at rates as low as 1 Hz. It consists of an 8-bit scaler, built up from DFF. The Hitbus clocks the Clock input, and the Strobe input controls the Data input to enable and disable the counting. By programming the width of the strobe generated by the MCC-I, which is a 16-bit value in 40MHz crossings, one can control the integration time for the HitBus Scaler. The scaler is designed so that when it reaches the full scale value of 255, it blocks further counting and retains this "overflow" value.

This block would be used in a "Hitbus Scaler" scan, in which one pixel per FE chip has its Hitbus enabled. The run would be initiated by writing to the Global Register (the WriteGlobal2 signal clears the Hitbus Scaler). The user might then issue 100 strobes of 1 msec duration in order to provide a total integration time of 100 msec. The Global Register is then read back to see how many hits this pixel had in the last 100 msec. With this technique, a concurrent scan for a full module could be performed in order to find the Hitbus counting rate for each pixel. Such a scan would take about 5 minutes to reach this level of sensitivity. Greater sensitivity can be achieved by using more strobes.

Note that the auto-tune circuitry could also be used for the purpose of finding hot pixels, in the same way that it is used for the stuck-on pixel scan. The use of a 1 msec strobe would allow isolating pixels that have more than 50% occupancy in a 1 msec interval. The advantage of using the auto-tune is that all pixels are processed in parallel, so it is very fast. The disadvantage is that the lowest occupancy that can be identified is 50% in the maximum strobe duration of about 1.6 msec. Therefore, only the Hitbus Scaler will have the sensitivity required for achieving the noise occupancies needed by ATLAS. The specification of less than 10^{-6} hits/pixel/crossing corresponds to about 1 noise hit per 300 events at a 100KHz trigger rate. This occupancy corresponds to less than a 40Hz counting rate for a pixel. This is beyond the reach of the auto-tune approach, but safely within the reach of the 5 minute Hitbus Scaler scan defined above.

Finding Stuck-on Pixels:

This type of defect seems to occur predominantly in IZM-bumped modules. It results in pixels which are always on. These pixels cause self-triggers when in the self-trigger mode, but do not produce data which is in time with the internal LVL1 trigger. This makes it very difficult to isolate them and disable them for either source scans or for normal module operation.

Since these pixels are very high occupancy (in principle, 100%), they can be easily detected by the auto-tune circuitry. In this case, the following sequence of steps can be used:

1. Clear the Kill bit (write 1 = EnablePreamp) for all pixels

2. Set the VCal for the chopper to inject zero charge (DAC=0), since we want to find pixels that are always on, there should be no need to inject charge.
3. Set the Select for all pixels that should participate in the auto-tune scan. For this case, this should be all pixels in a given FE chip, since we do not expect many pixels to be on.
4. Disable the Readout for all pixels to avoid producing any data, which will generate additional digital noise. It would also require slowing down the strobe rate of the auto-tune scan to allow transfer of the data.
5. Disable the Hitbus as well, as it is not needed for auto-tuning.
6. Enable Auto-tune mode in the Global Register.
7. Load the TDACs with some large value, which should cause all channels to sit well above the noise level. The correct value may not be the maximum TDAC value, but only something larger than 50% of full scale. Note that by setting the LoadTDAC0 strobe, the up-down counter in each pixel used to record the state of the auto-tuning is automatically preset to its mid-point (only the MSB is set).
8. Issue order of 100 Strobes. The interval between strobes can be set by the need for the FE to settle from the wrong-sign pulse created by the internal strobe. An interval of order 10-20μs should be adequate (TurboDAQ interval = 50), provided that the strobe width is set accordingly (to about half of the interval) (TurboDAQ width of 500). For each case where the discriminator in a given pixel fires, the up-down counter will count up. Otherwise, it will count down.
9. Issue a LoadKill strobe in order to store the final state of the up-down counter into the Kill latch. If a pixel has fired more than 50% of the time, then the Kill bit should be set. Since we are injecting no charge, and have chosen a large TDAC value, only the stuck-on pixels should satisfy this condition.
10. Disable the Auto-tune mode, and read back the Kill bit state for each pixel. The Kill should be set (read back as zero) only for those pixels that had more than 50% occupancy during this tune sequence, which should be only the stuck-on pixels.

Appendix 6: Reticle and Wafer Layout for FE-I3:

This section summarizes the reticle layout and the wafer layout for the FE-I3 production run. In this run, there are two indentical FE-I3 chips in the reticle. However, for historical reasons, they are labeled as FE-I3A and FE-I3B (the only difference is in the logo area).

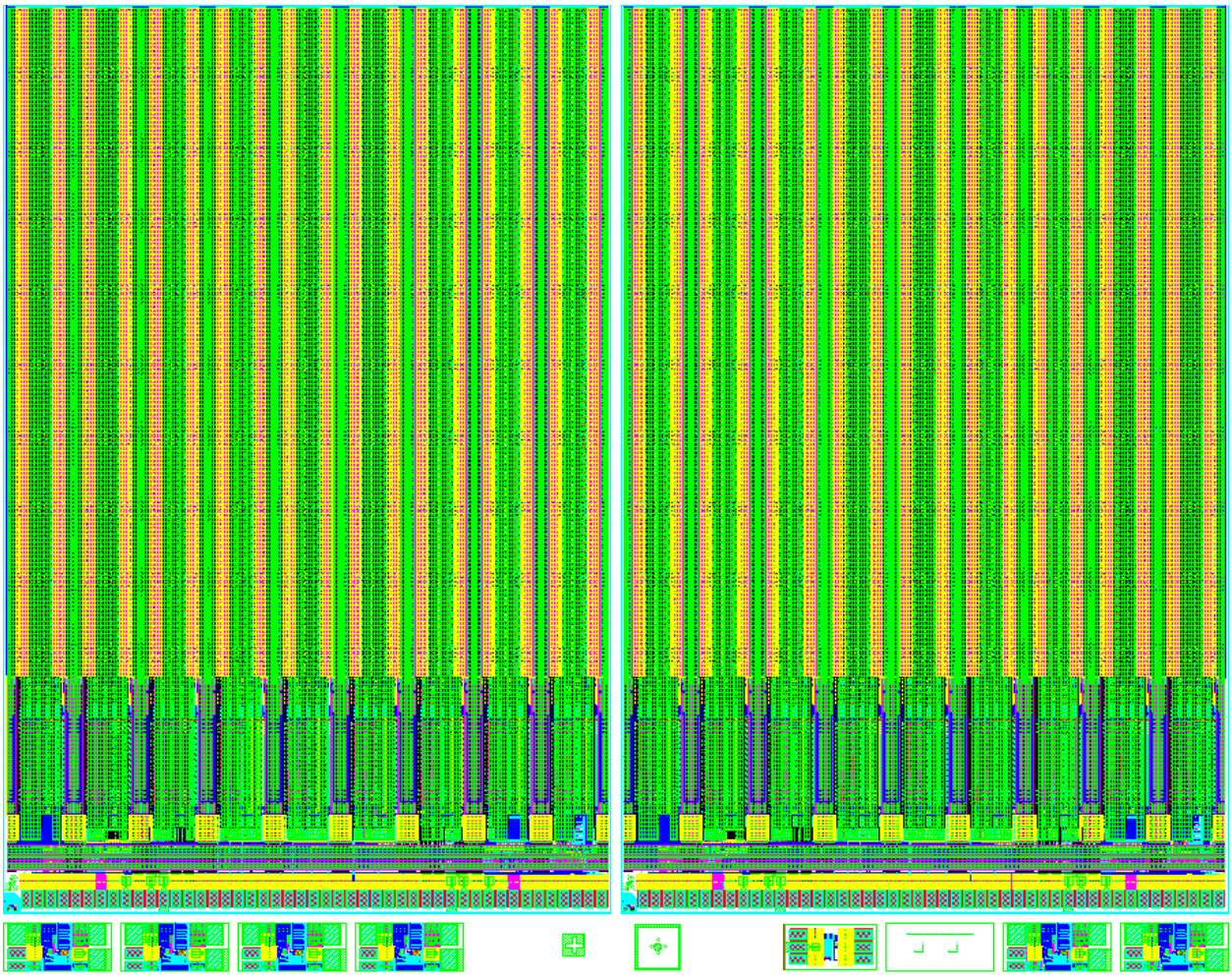


Figure 9 GDS image for the FE-I3 Reticle.

The reticle contains three copies of a digital regulator chip and three copies of an analog regulator chip. In addition, there is a simple test chip for the new bias compensation circuit. Finally, there is a bump-test structure for IZM, and two global alignment marks for the two bumping vendors (AMS uses the small cross on the left, IZM uses the larger structure on the right). An image of the GDS file is shown in Fig. 7. A sketch of the reticle and how it should be diced is shown in Fig. 8.

IBM Reticle Layout for FE-I2 (ATLASPIX2.0) Run. Drawn to scale, 100u gap between Chipedge of designs

Nominal Rules:

* **ChipEdge is 9.5u outside ChipGuard, and defines design size given below.**
* **Different designs are separated by 100μ gap between ChipEdges.**
* **Reticle is defined by Chipedge around the perimeter, overlapping the individual Chipedge of each design.**
* **Reticle was submitted rotated by 90 degrees counter-clockwise, so (0,0) is in the upper left corner. This results in the reticle on the wafer having the orientation shown here, with the wafer notch down.**

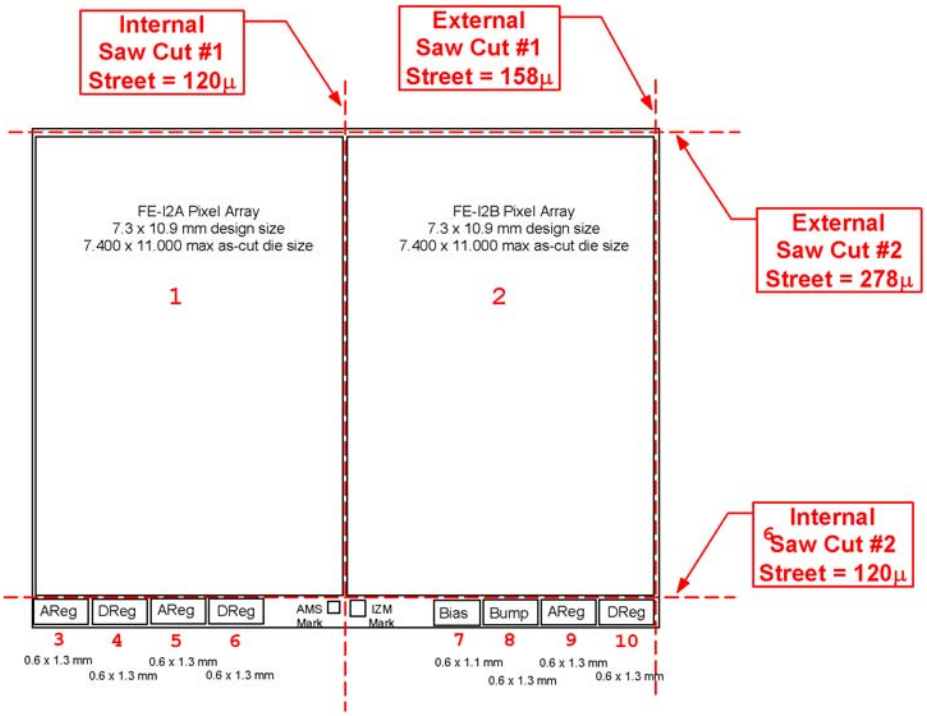
Reticle size is: 14.700 (W) x 11.600 (H) mm

IBM adds 138μ in one direction and 258μ in the other direction.
We choose to have the 138μ added to the left/right of the reticle shown here,
and to have the 258μ added above/below the reticle shown here.

This allows us to meet critical die dimension requirements on Die #1 and #2 with standard dicing procedure.

Reticle stepping increments with these rules would be: 14.838 (W) x 11.858 (H) mm

Internal Cut #2 and External Cut #2 are separated by only about 1000μ (outer edge to outer edge), so care is required.



3

Figure 10 Sketch of FE-I3 Reticle, including dicing instructions.

Finally, the wafer layout consists of 144 copies of the reticle stepped across the wafer. The arrangement of these reticles is shown in Fig. 9. The numbering convention starts in the lower left corner, where the first good reticle is (5,1). The first digit is the x coordinate, the second is the y coordinate. The last good reticle in the upper right corner is (9,15). When the wafer is viewed with the notch down, the reticle orientation is as shown in Fig. 7 and Fig. 8. Note that the

reticles and die labeled as “E” are edge reticles that are not completely processed by IBM, and therefore are “known bad”. These reticles are not numbered and will not be tested during the wafer probing.

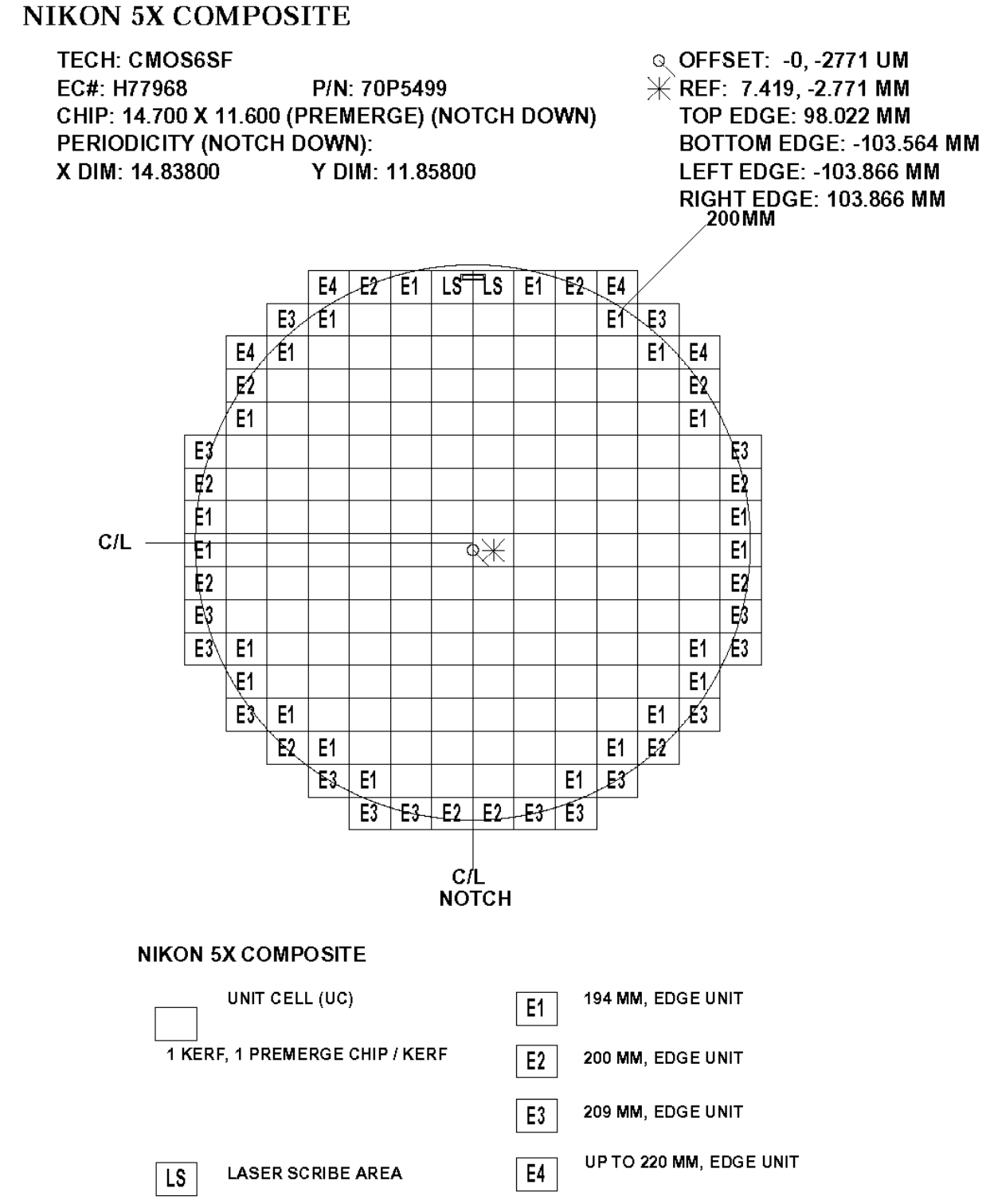


Figure 11 Arrangement of FE-I3 Reticles on the wafer.

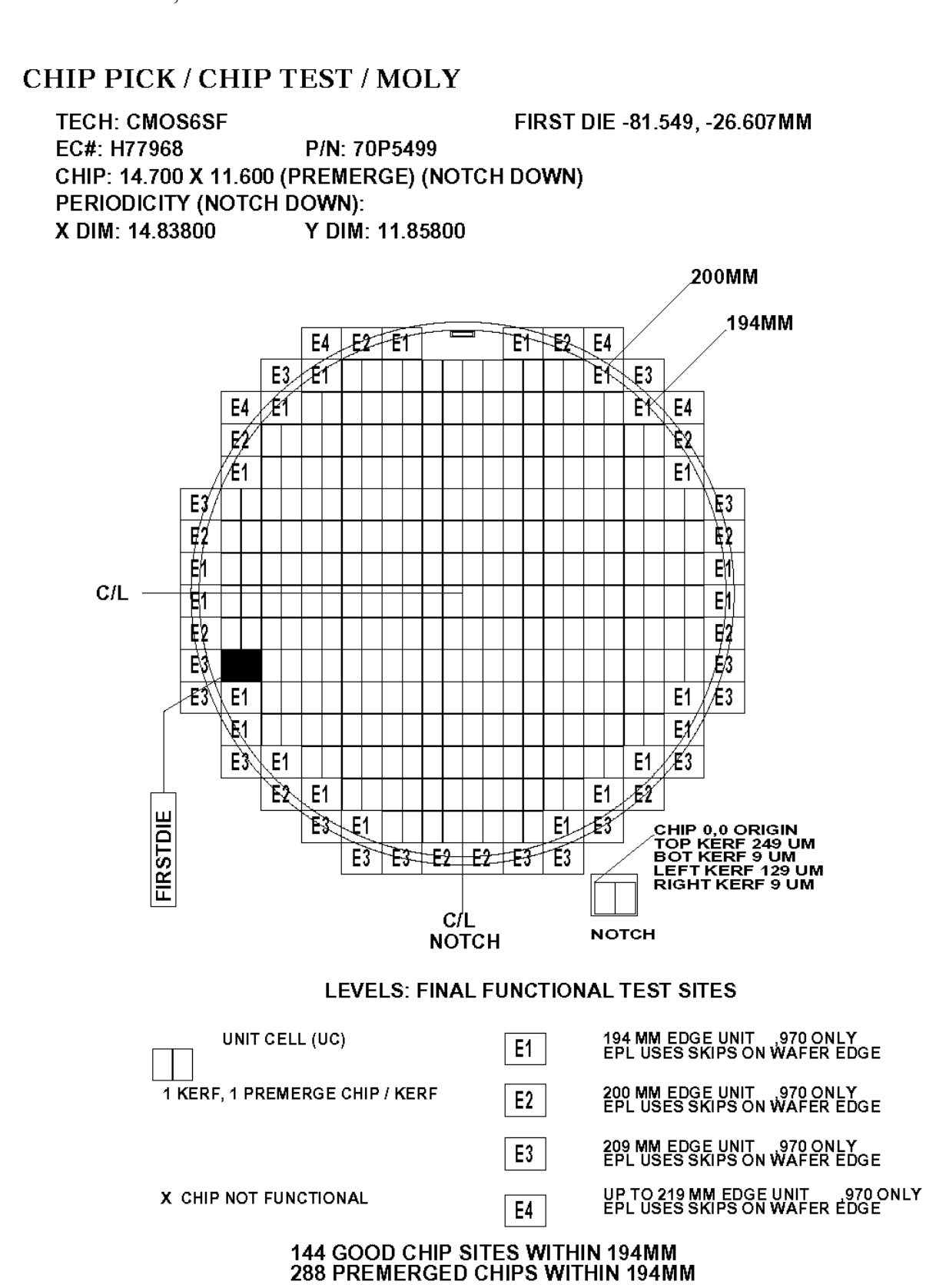


Figure 12 Location of individual FE-I3 die on the wafer.