Xilinx ILA (Integrated Logic Analyzer)

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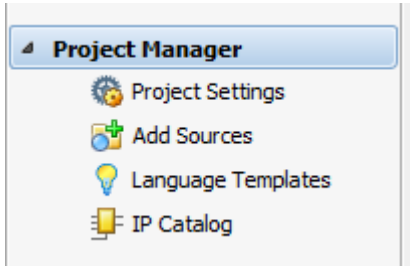
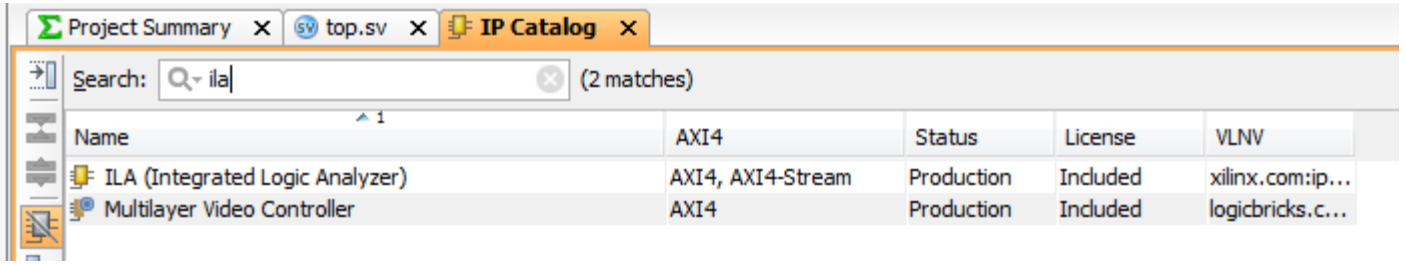
Introduction

- Logic Analyzers allow for monitoring of internal signals of a design
- ILA is a core in the Xilinx IP Catalog
- Inputs can be specified as probes
- Advanced options such as triggers allow for targeted testing
- VIO (Virtual Input Output) can be used in conjunction with the ILA

Setup

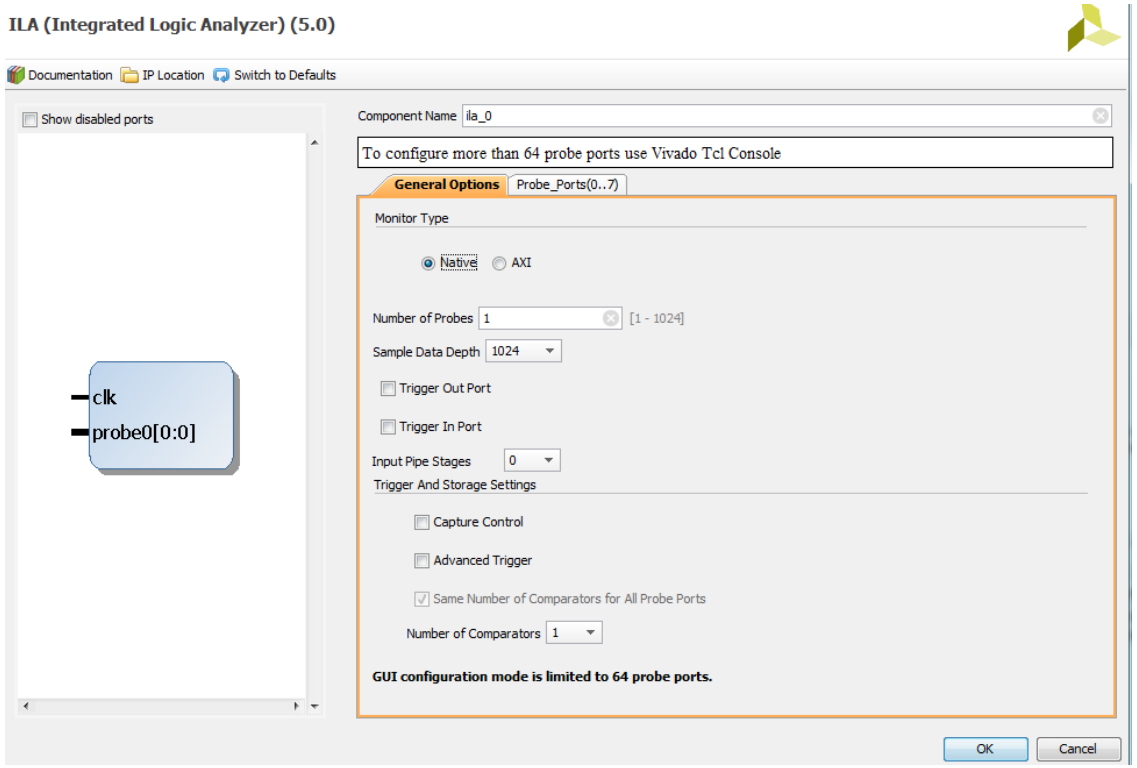


Find IP Catalog under Project Manager

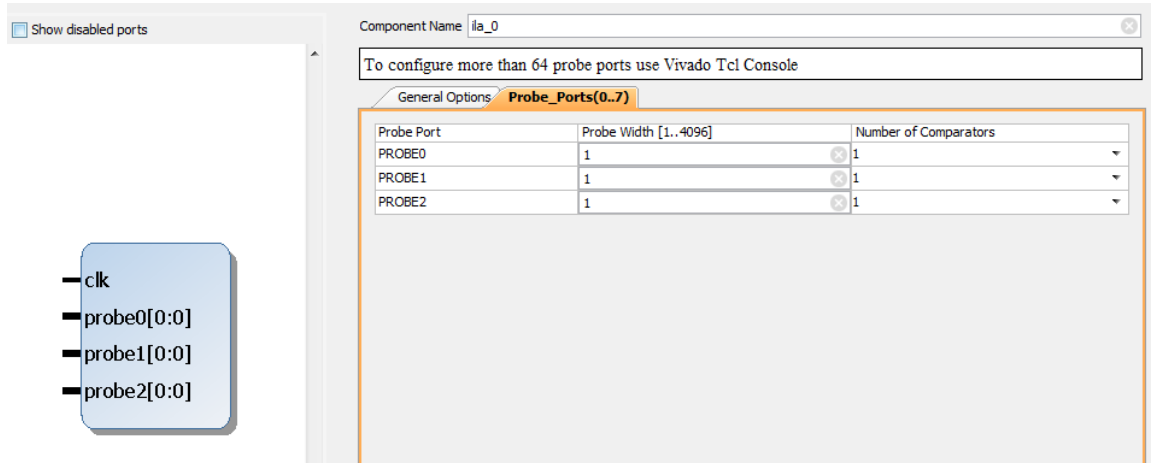


Search for ILA and click ILA (Integrated Logic Analyzer)

Setup cont.



Specify settings for the ILA. Number of Probes and Sample Data Depth are important aspects



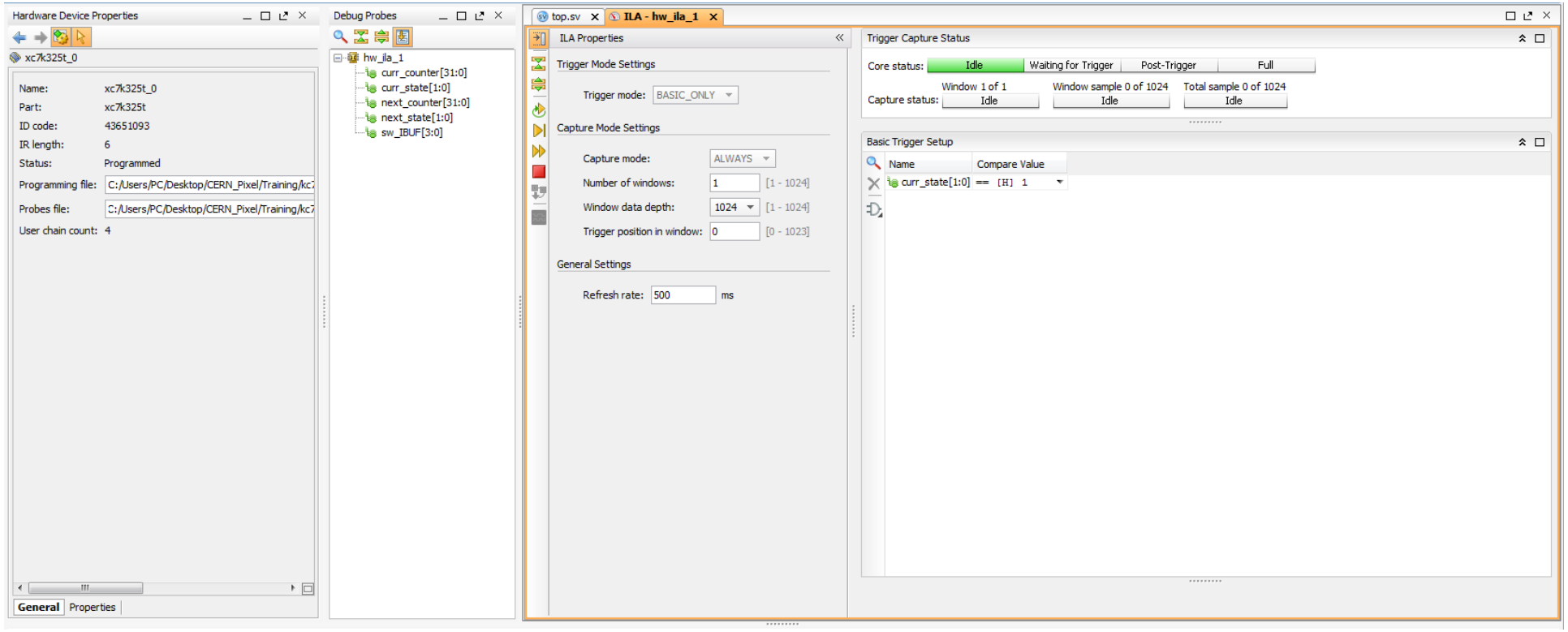
Specify the probe width for each corresponding probe

Instantiate ILA

```
ila_0 ila_debug(
    .clk(sysclk),
    .probe0(curr_state),
    .probe1(next_state),
    .probe2(curr_counter),
    .probe3(next_counter),
    .probe4(sw)
    );
```

- The clock going into the ILA should be at least the frequency of the clock in the design
- Higher frequencies allow for higher sampling rates

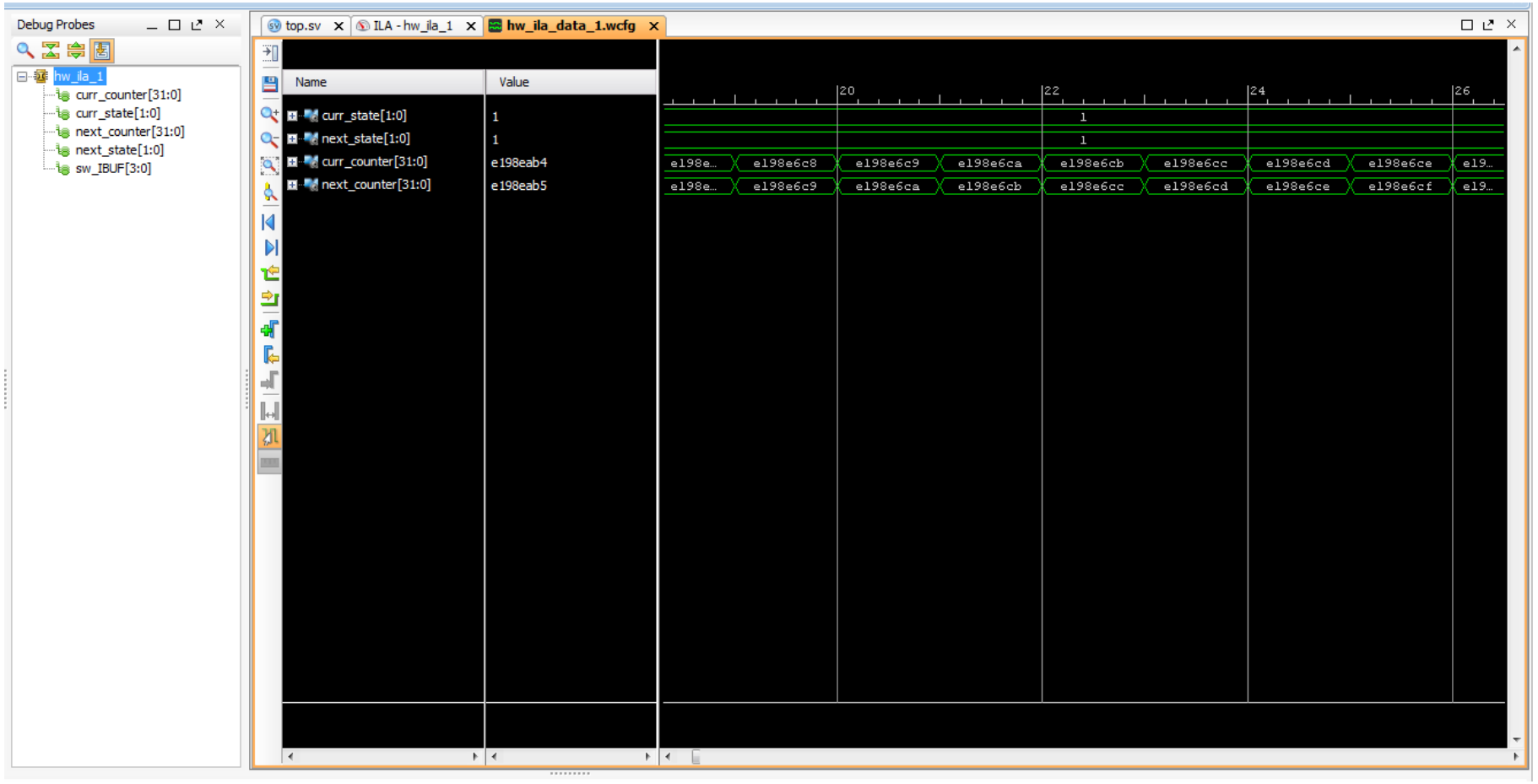
Generate Bitstream and use ILA



Configure trigger and arm the core

ILA Waveform

- View waveform after trigger fires



References

- https://www.xilinx.com/support/documentation/ip_documentation/ila/v6_1/pg172-ila.pdf