Pixel scan structure addendum

The DSP scan engine of the current Pixel ROD is extensively described in ref. [1] and that of the IBL ROD for FE-I4 in ref. [2]. The following is meant to provide additional information on the mask shifting, i.e. on processing of the mask loop level as illustrated by figure 7 in [1] and Figure 2 in [2].

Mask loop for FE-I3: uses the enable pixel register (typ. digital-injection-based scans), optionally in combination with the injection (select) pixel register for analogue-injection-based scans, to turn on a sub-set of all pixels in a regular pattern. An n-step-mask means that every n-th pixel is turned on, starting at rows 0,n,2n,... in even columns, and starting at rows 1, n+1,2n+1,... in odd columns[1]. At each mask step, a "0" is added at the input of the shift register after latching the pixel register content into it. As consequence, the mask pattern is shifted to higher row indices in even and to lower row indices in odd columns[2], see figure 1.

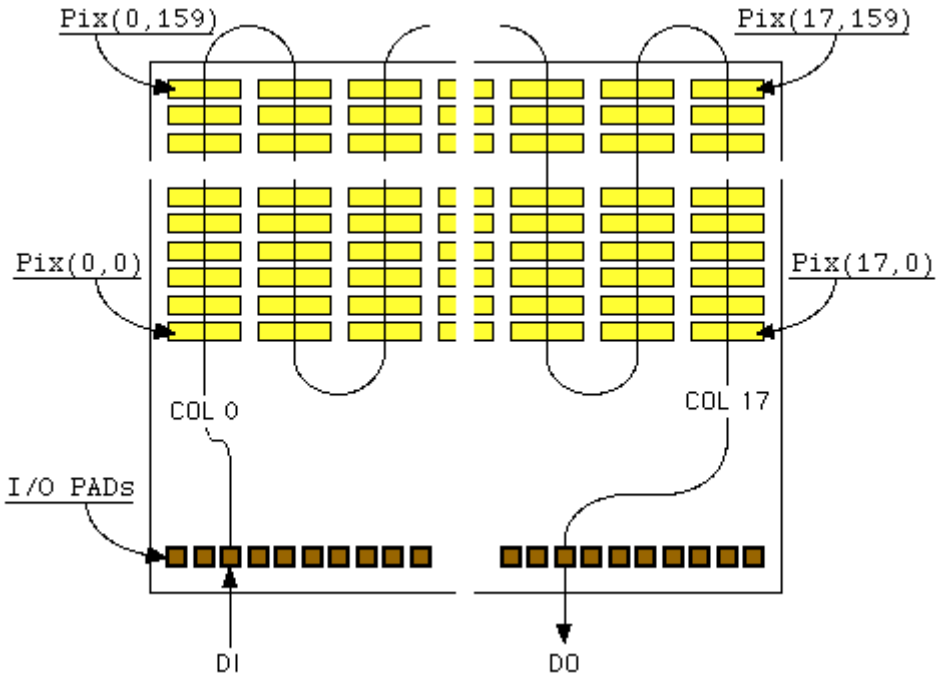

Figure 1: Diagram of the path of the FE-I3 pixel shift register as it snakes through the two dimensional matrix of pixel channels. Each column pair contains a U-shaped segment of the shift register as it goes up the left side and comes down the right side. The nine U-shaped segments in the chip can be separately enabled using the Global Register [3].

Comparison of FE-I3 and FE-I4: Row and column ID of each pixel are counted differently for the two FE flavours used in the pixel detector. FE-I3 starts both from 0 (column up to 17 and row up to 159) with pixel (0,0) being located at the bottom left when the wire bond pads mark the bottom edge. In contrast, FE-I4 starts both indices from 1 (column up to 80 and row up to 336) and pixel (1,1) is located at the top left (again, wire bond pads marking the bottom edge). Both FEs start writing and shifting of pixel registers from the wire bond pads. Shifting the pixel register content as used in the mask stage loop of a scan moves the mask pattern away from the pads in even-numbered columns (left-most column, its 2nd neighbour to the right etc.) and towards the pads in odd-numbered columns for FE-I3. In contrast, for FE-I4 the mask pattern is moved away from the pads

1 Rows and columns in FE-I3 are counted starting from 0, see figure 1.

2 Pixel register writing and shifting is done via a chain connection of columns connecting them at row 0 or 159, resp., see figure 1.

in odd-numbered columns (left-most column, its 2nd neighbour to the right etc.) and towards the pads in even-numbered columns. When looking at the mask pattern in terms of row numbers, the behaviour is the other way round (e.g. moving towards low row-indices in the left-most column). The initial mask patterns and the pattern after having been shifted by one is illustrated in figure X.

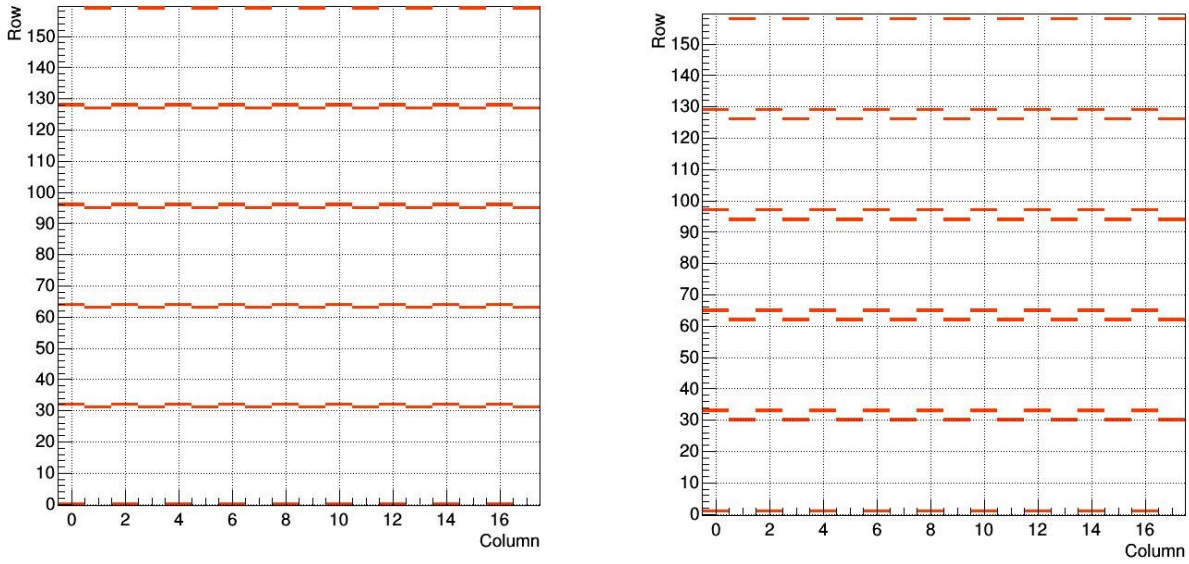

Figure 2: Pattern of a 32-step-mask on FE-I3 with the initial settings, i.e. mask step 0 (left) and after the first shift, i.e. mask step 1 (right). The orientation of the map corresponds to the pixel matrix of the chip when looking at that from the bump-bond side with the wire bond pads at the bottom.

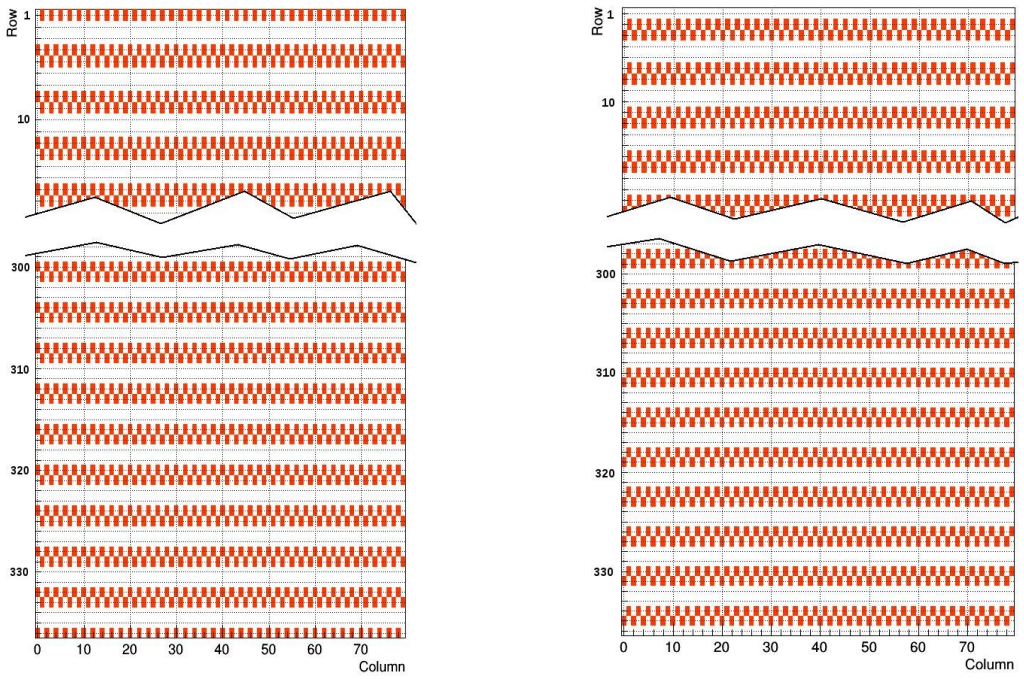

Figure 3: Pattern of a 4-step-mask on FE-I4 with the initial settings, i.e. mask step 0 (left) and after the first shift, i.e. mask step 1 (right). Note the flipped y-axis which displays the row index such that the map corresponds to the pixel matrix of the chip when looking at that from the bump-bond side with the wire bond pads at the bottom. NB: plots from CalibrationConsole will look flipped, i.e. with row 1 at the bottom of the plot!

References

[1] J. Biesiada et al., *The Implementation and Performance of ROD DSP Software in the ATLAS Pixel Detector*, ATL-INDET-INT-2009-006.

[2] J. Grosse-Knetter, A. Kugel et al., *Calibration of the ATLAS IBL detector using the new VME readout architecture*, internal note available on share point.

[3] K. Einsweiler, *ATLAS Pixel FE-I3 Chip: Design Description*, available on share point.