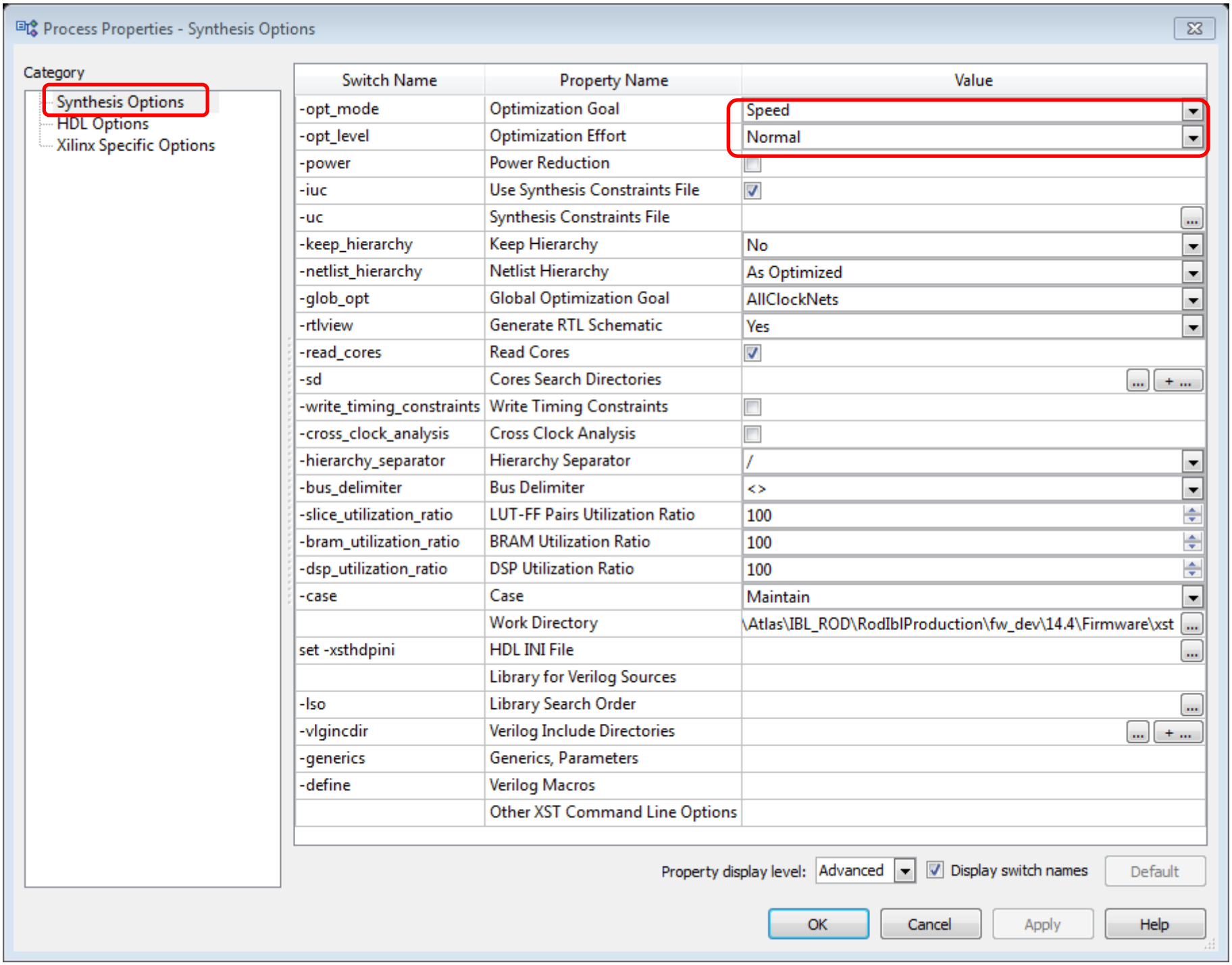
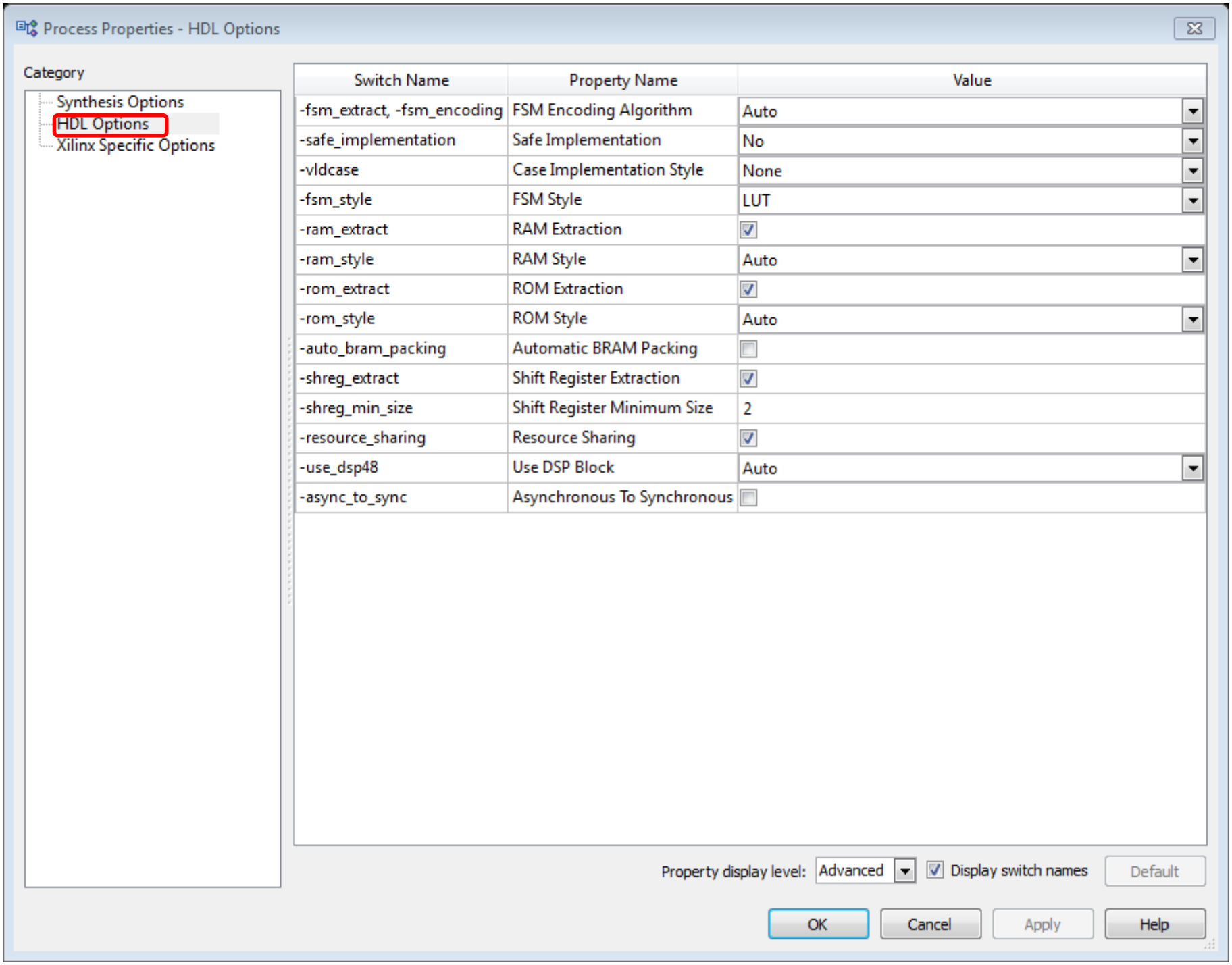
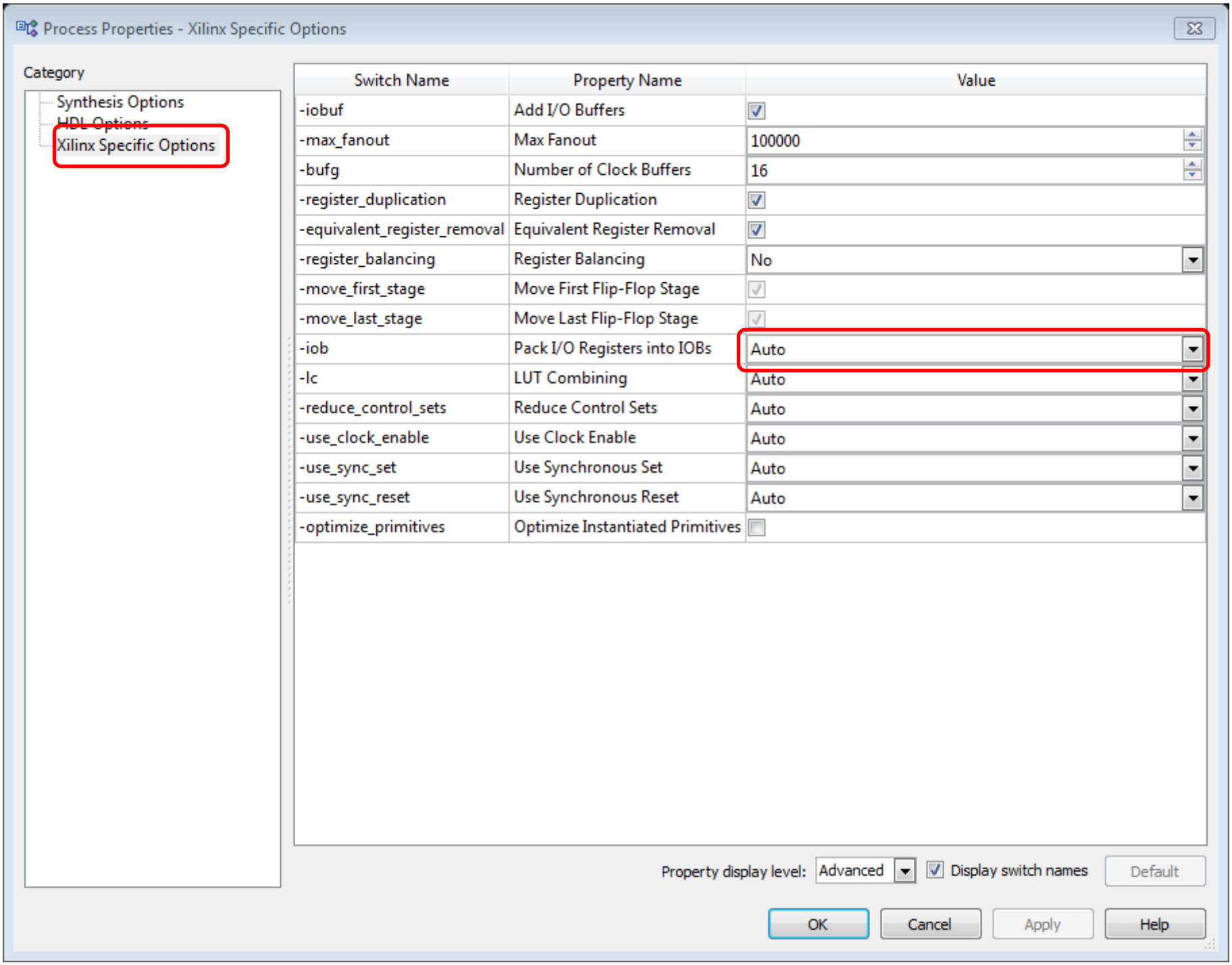

Process Properties - Synthesis Options
Category
Synthesis Options
HDL Options
Xilinx Specific Options
Switch Name
Property Name
Value
-opt_mode
Optimization Goal
Speed
-opt_level
Optimization Effort
Normal
-power
Power Reduction
-iuc
Use Synthesis Constraints File
-uc
Synthesis Constraints File
-keep_hierarchy
Keep Hierarchy
No
-netlist_hierarchy
Netlist Hierarchy
As Optimized
-glob_opt
Global Optimization Goal
AllClockNets
-rtlview
Generate RTL Schematic
Yes
-read_cores
Read Cores
-sd
Cores Search Directories
-write_timing_constraints
Write Timing Constraints
-cross_clock_analysis
Cross Clock Analysis
-hierarchy_separator
Hierarchy Separator
/
-bus_delimiter
Bus Delimiter
<>
-slice_utilization_ratio
LUT-FF Pairs Utilization Ratio
100
-bram_utilization_ratio
BRAM Utilization Ratio
100
-dsp_utilization_ratio
DSP Utilization Ratio
100
-case
Case
Maintain
Work Directory
\Atlas\IBL_ROD\RodIblProduction\fw_dev\14.4\Firmware\xst
set -xsthdpini
HDL INI File
Library for Verilog Sources
-lso
Library Search Order
-vlgincdir
Verilog Include Directories
-generics
Generics, Parameters
-define
Verilog Macros
Other XST Command Line Options
Property display level:
Advanced
Display switch names
Default
OK
Cancel
Apply
Help


Process Properties - HDL Options
Category
Synthesis Options
HDL Options
Xilinx Specific Options
Switch Name
Property Name
Value
-fsm_extract, -fsm_encoding
FSM Encoding Algorithm
Auto
-safe_implementation
Safe Implementation
No
-vldcase
Case Implementation Style
None
-fsm_style
FSM Style
LUT
-ram_extract
RAM Extraction
-ram_style
RAM Style
Auto
-rom_extract
ROM Extraction
-rom_style
ROM Style
Auto
-auto_bram_packing
Automatic BRAM Packing
-shreg_extract
Shift Register Extraction
-shreg_min_size
Shift Register Minimum Size
2
-resource_sharing
Resource Sharing
-use_dsp48
Use DSP Block
Auto
-async_to_sync
Asynchronous To Synchronous
Property display level:
Advanced
Display switch names
Default
OK
Cancel
Apply
Help


Process Properties - Xilinx Specific Options
Category
Synthesis Options
HDL Options
Xilinx Specific Options
Switch Name
Property Name
Value
-iobuf
Add I/O Buffers
-max_fanout
Max Fanout
100000
-bufg
Number of Clock Buffers
16
-register_duplication
Register Duplication
-equivalent_register_removal
Equivalent Register Removal
-register_balancing
Register Balancing
No
-move_first_stage
Move First Flip-Flop Stage
-move_last_stage
Move Last Flip-Flop Stage
-iob
Pack I/O Registers into IOBs
Auto
-lc
LUT Combining
Auto
-reduce_control_sets
Reduce Control Sets
Auto
-use_clock_enable
Use Clock Enable
Auto
-use_sync_set
Use Synchronous Set
Auto
-use_sync_reset
Use Synchronous Reset
Auto
-optimize_primitives
Optimize Instantiated Primitives
Property display level:
Advanced
Display switch names
Default
OK
Cancel
Apply
Help

Process Properties - Map Properties

Category

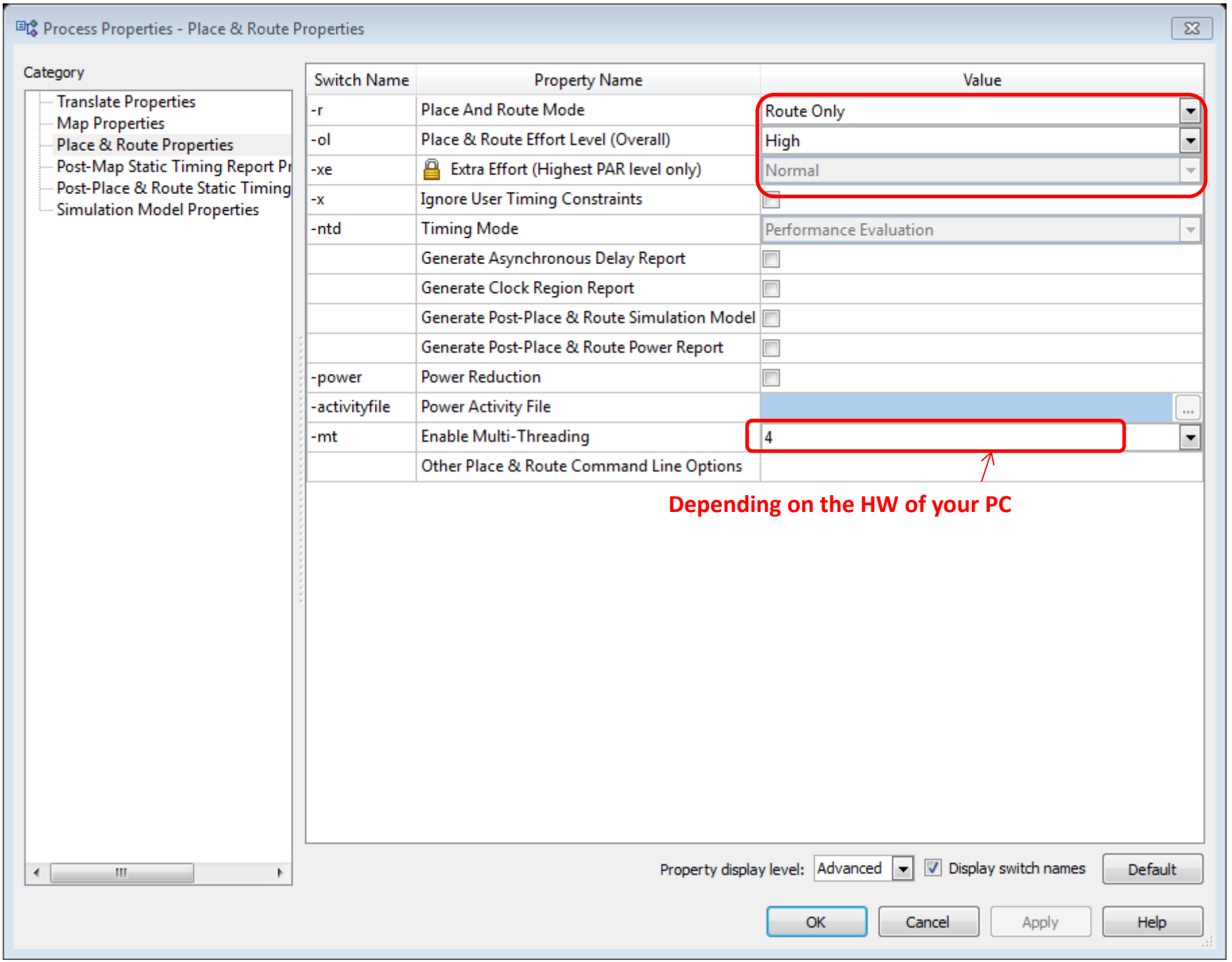
- Translate Properties
- Map Properties
- Place & Route Properties
- Post-Map Static Timing Report Pr
- Post-Place & Route Static Timing
- Simulation Model Properties

Switch Name	Property Name	Value
-ol	Placer Effort Level	High
-xe	Placer Extra Effort	Normal
-t	Starting Placer Cost Table (1-100)	1
-xt	Extra Cost Tables	0
-logic_opt	Combinatorial Logic Optimization	
-register_duplication	Register Duplication	Off
-r	Register Ordering	4
-global_opt	Global Optimization	Off
-equivalent_register_removal	Equivalent Register Removal	
-x	Ignore User Timing Constraints	
-ntd	Timing Mode	Performance Evaluation
-u	Trim Unconnected Signals	
-ignore_keep_hierarchy	Allow Logic Optimization Across Hierarchy	
-detail	Generate Detailed MAP Report	
-ir	Use RLOC Constraints	Yes
-pr	Pack I/O Registers/Latches into IOBs	Off
-c	Maximum Compression	
-lc	LUT Combining	Off
-bp	Map Slice Logic into Unused Block RAMs	
-power	Power Reduction	Off
-activityfile	Power Activity File	
-mt	Enable Multi-Threading	2
	Other Map Command Line Options	

Depending on the HW of your PC

Property display level: Advanced | Display switch names | Default

OK | Cancel | Apply | Help


Process Properties - Place & Route Properties
Category
Translate Properties
Map Properties
Place & Route Properties
Post-Map Static Timing Report Pr
Post-Place & Route Static Timing
Simulation Model Properties
Switch Name
Property Name
Value
-r
Place And Route Mode
Route Only
-ol
Place & Route Effort Level (Overall)
High
-xe
Extra Effort (Highest PAR level only)
Normal
-x
Ignore User Timing Constraints
-ntd
Timing Mode
Performance Evaluation
Generate Asynchronous Delay Report
Generate Clock Region Report
Generate Post-Place & Route Simulation Model
Generate Post-Place & Route Power Report
-power
Power Reduction
-activityfile
Power Activity File
-mt
Enable Multi-Threading
4
Other Place & Route Command Line Options
Depending on the HW of your PC
Property display level:
Advanced
Display switch names
Default
OK
Cancel
Apply
Help