ROD Firmware status

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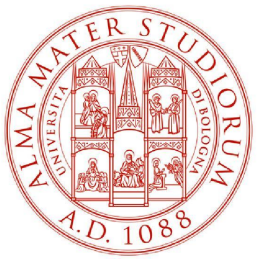

ROD Firmware Status

New implementations

- New **Header Trailer Limit** and **Data Overflow limit** for Pixel and IBL
  1. ready and tested
  2. need proper register settings
  3. HTL counters developed but not tested yet
- New **Timeout Logic**;
  1. ready but not tested
- New **Desynchronization Correction** Algorithm
  1. ready
  2. built on top of HTL to prevent BUSY
  3. not tested
- New **Desynchronization prevention** algorithm
  1. firmware to monitor mcc buffer occupancy has been developed
  2. mechanism to stop forwarding triggers to single modules under investigation

Current

- Master **propagates xc** signal to Slave (1 line)
- Slave immediately **splits xc** over 16 lines $\longrightarrow$ 1 clock cycle delay

New mechanism

- Master **propagates xc** signal to Slave (1 line)
- Slave must **identify trigger** from other xc commands (5 clock cycles required minimum)
- Slave **propagates trigger** only to module **not full** (1 clock cycle required)

Register Settings

Register Settings for Busy, HTL and DOVR

Default values

- **FMT_ROD_BUSY_LIMIT** (Register 0x1C) = 0x3C0 (**not restored** by reset)
- **FMT_HEADER_TRAILER_LIMIT** (Register 0x18) = 0x800 (**restored** by reset)
- **FMT_DATA_OVERFLOW_LIMIT** (Register 0x14) = 0x800 (**restored** by reset)

DATA-TAKING

- **FMT_ROD_BUSY_LIMIT** (Register 0x1C) = 0x776 (15/16 fifo size)
- **FMT_HEADER_TRAILER_LIMIT** (Register 0x18) = 0x700 (7/8 fifo size)
- **FMT_DATA_OVERFLOW_LIMIT** (Register 0x14) $\approx$ 0x320 (800 hits)

CALIBRATION

- **FMT_ROD_BUSY_LIMIT** (Register 0x1C) = 0x776 (ignored during calibration)
- **FMT_HEADER_TRAILER_LIMIT** (Register 0x18) = 0x800 (no effect)
- **FMT_DATA_OVERFLOW_LIMIT** (Register 0x14) $\approx$ 0x800 (no effect)

HTL counters

- same logic of Timeout and Desynch Counters
- register addresses will be provided soon
- still under testing