L1/L2 ROD Firmware Status

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L1/L2 ROD Firmware Status

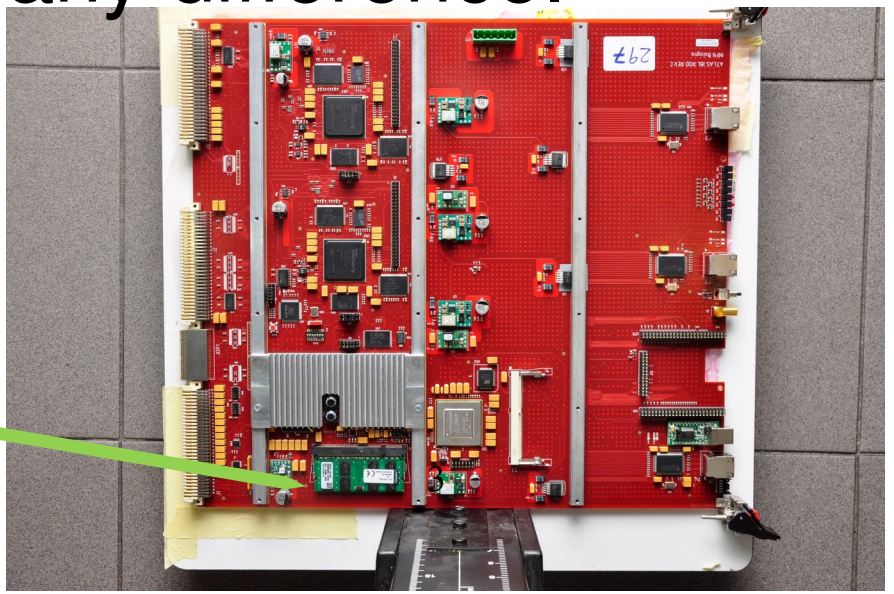
Completed tasks

- Changed the memory controller for DDR2.
- The Histogrammer is working and tested (see next slides).
- Datapath has been tested with FEI3 emulator on BOC with all three modes.
- Merged two S-Link data streams into one per ROD FPGA; we have two S-Links per ROD/BOC pair.

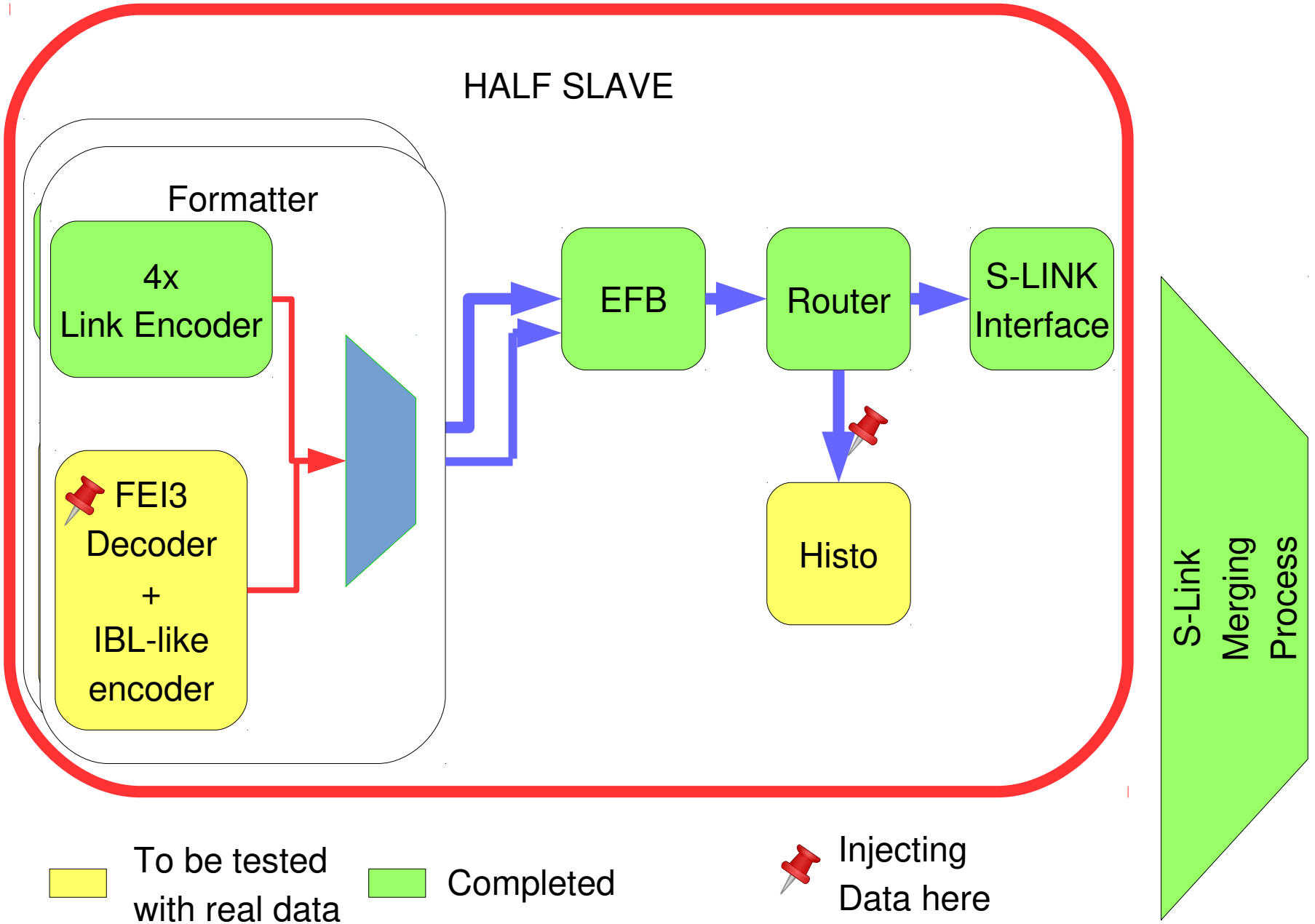
Changed PPC Memory controller

- The new DDR2 SODIMM banks were not compatible with the old memory controller.
- The address space increased from 256MB to 1GB.
- Other peripherals are still in the same location.
- Software does not notice any difference.

Kingston SODIMM
KVR667D2S5/2G (old)
KFJFPC218/2G



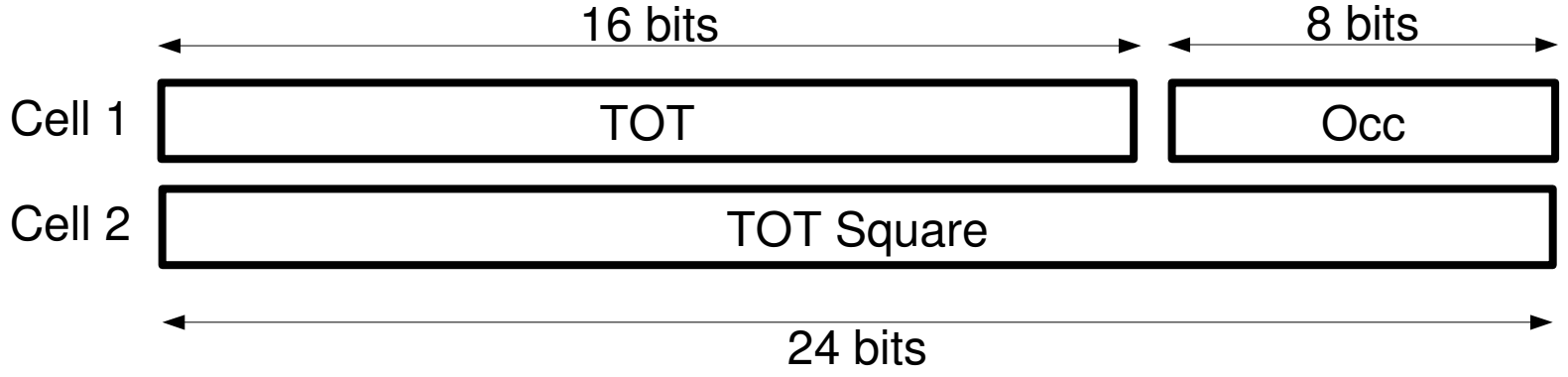
Block diagram: ROD Half SLAVE



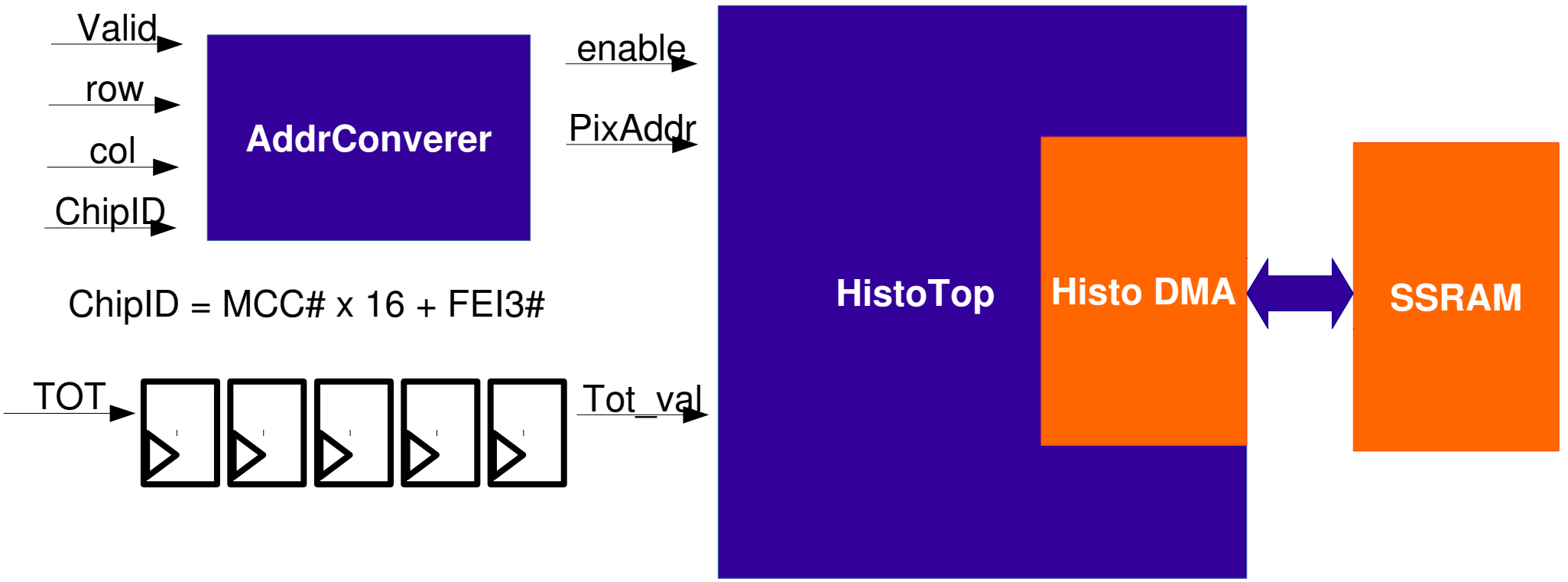
Histogrammer

- Histogrammer fully simulated and working.
- Short TOT mode is not supported anymore since it's not necessary.
- Has no more addressing problems.

We use two 36 bits ssram cells for each pixel:



Histogrammer block diagram



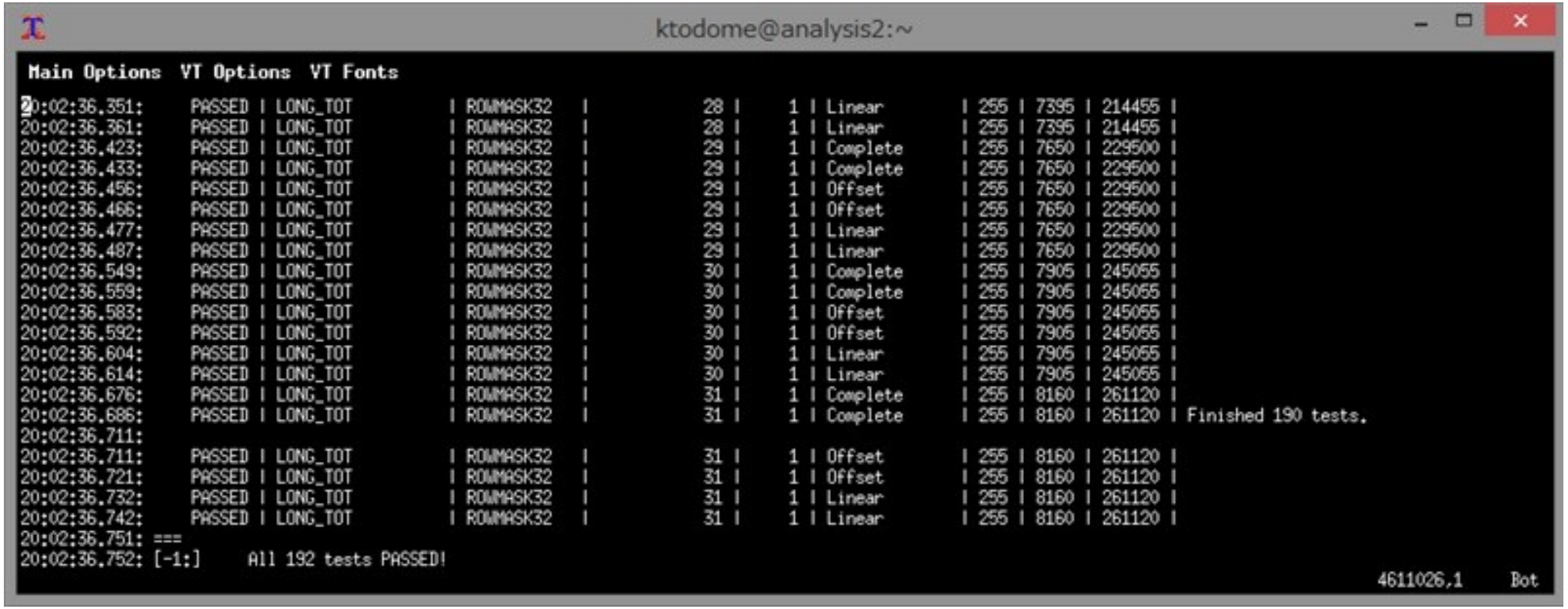
As a consequence of using two ssram cells it takes four clock cycles to write each Hit inside the ssram.

2 kHz trigger rate still achievable.

Histogrammer

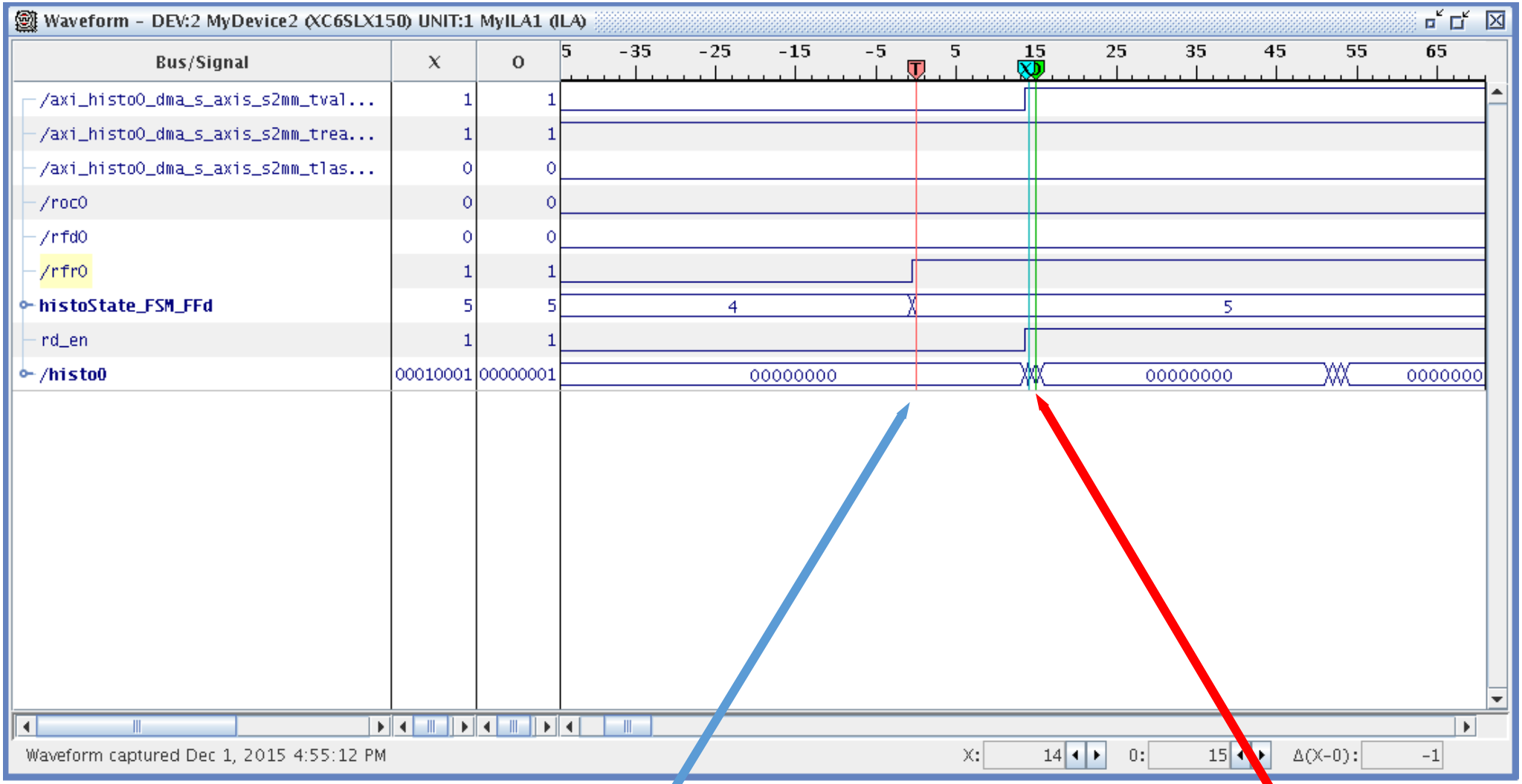
All tests that are implemented in Nick's Software are passed.
(Data injected directly into histogrammer.)

- It has only one Mask Step
- It needs to transfer 128 chips when reading more than one



Histogrammer

Histogrammer



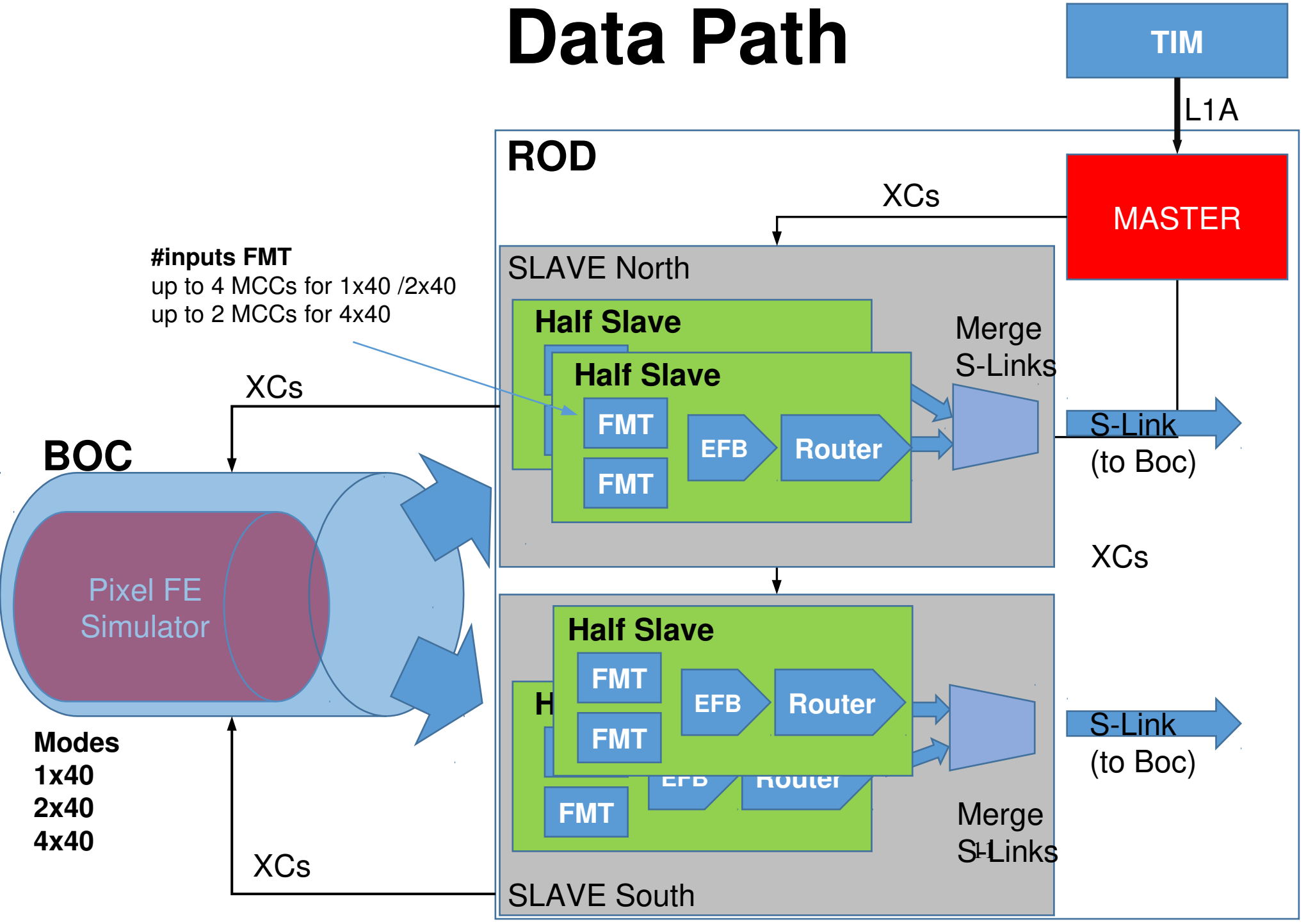
Histogrammer Ready For Readout

First bin transfer, TOT and TOT²

Data Path

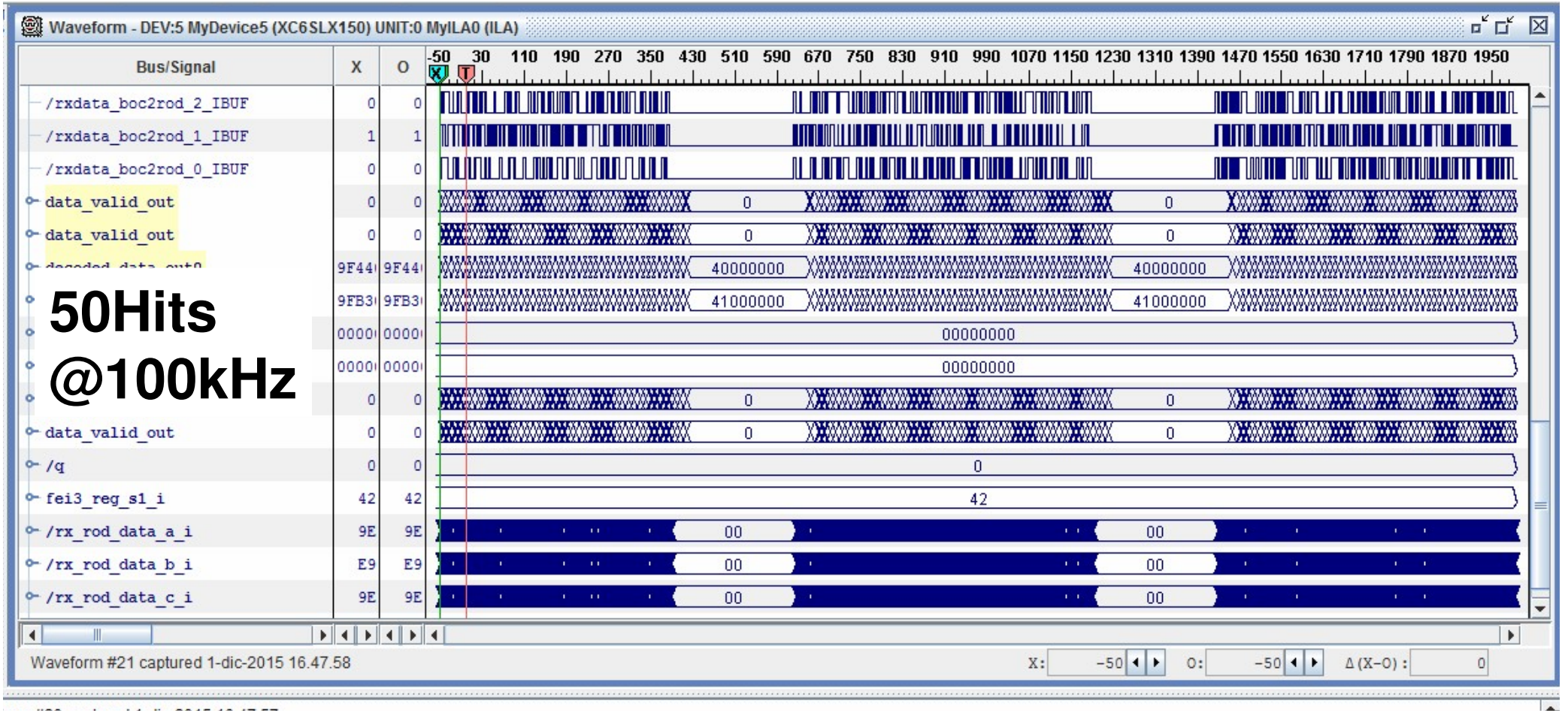
- Pixel FESim moved into the BOC (Marius).
- Adapted John's link encoders into the Formatters and tuned for the local clock.
- With FESim we tested the entire system from BOC to the S-Link output.
  - **4x40**: Fully working at 50 Hits, 100 kHz.
  - **2x40**: Fully working at 10 Hits, 100 kHz.
  - **1x40**: Some issue found in S-Link merge, under study.

Data Path


TIM
L1A
ROD
MASTER
XCs
#inputs FMT
up to 4 MCCs for 1x40 /2x40
up to 2 MCCs for 4x40
SLAVE North
Half Slave
Half Slave
FMT
FMT
EFB
Router
Merge
S-Links
S-Link
(to Boc)
XCs
BOC
Pixel FE
Simulator
Modes
1x40
2x40
4x40
Half Slave
FMT
FMT
EFB
Router
FMT
Merge
S-Links
S-Link
(to Boc)
XCs
SLAVE South

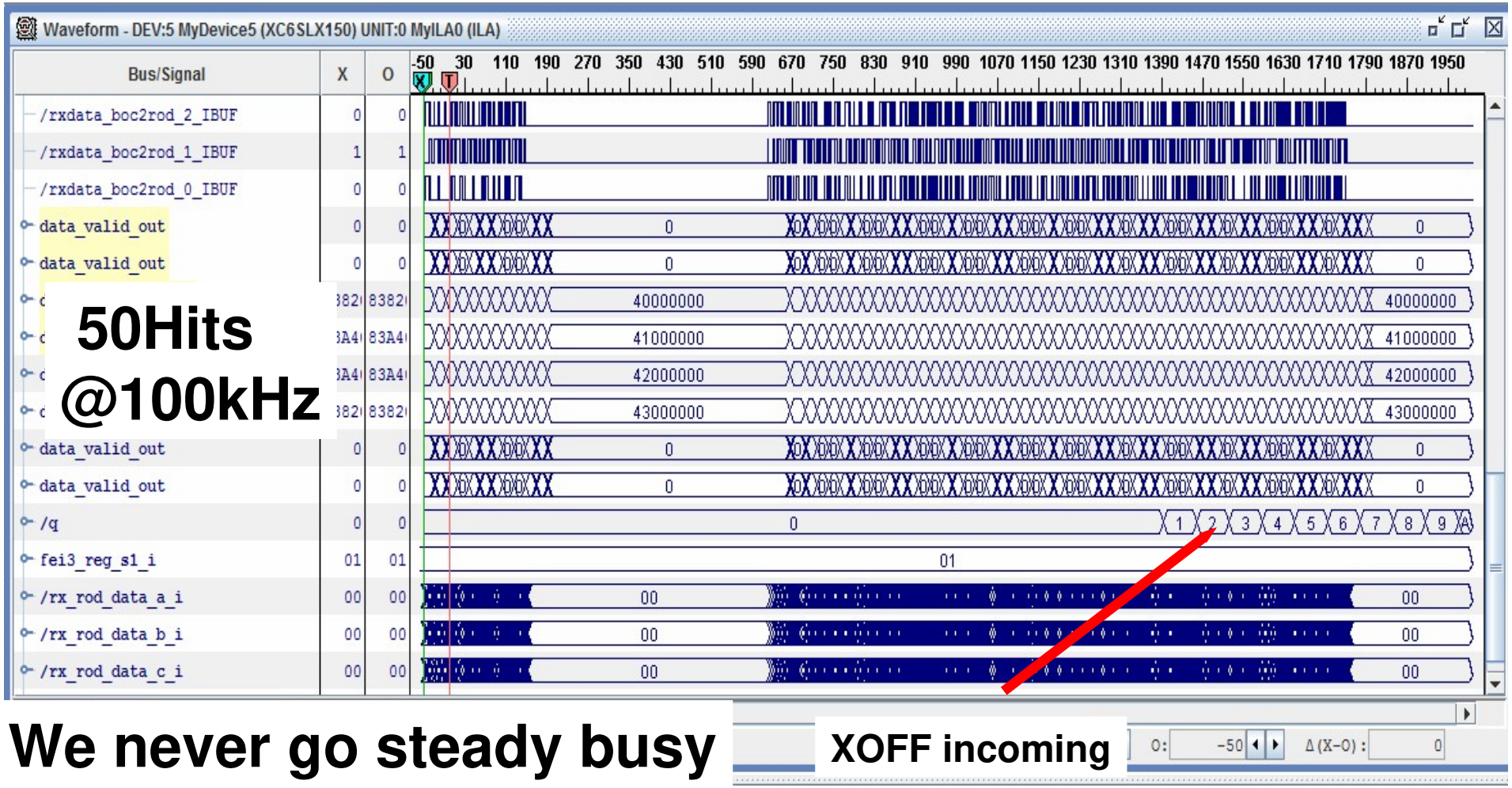
Data Path

Formatters inputs and decoded outputs with 4x40 Mode



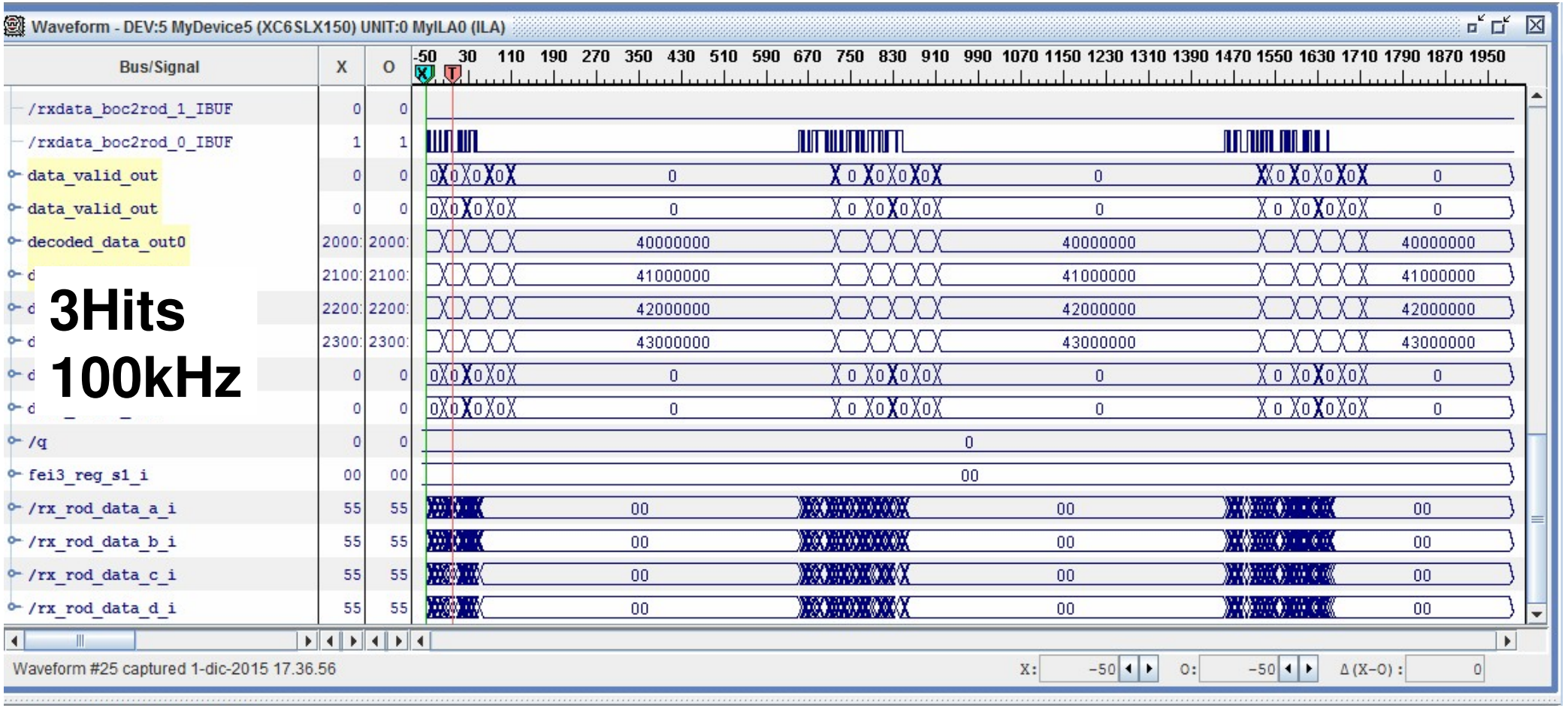
Data Path

Formatters inputs and decoded outputs with 2x40 Mode

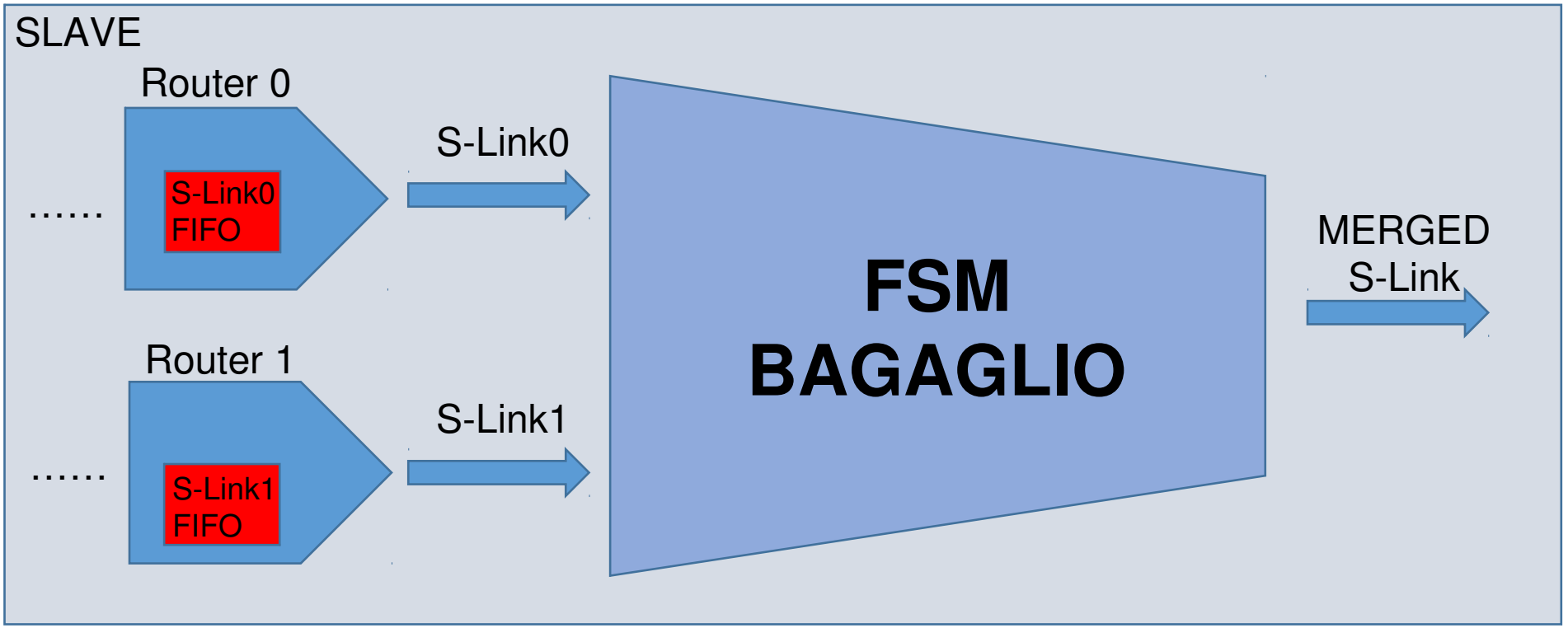


Data Path

Formatters inputs and decoded outputs with 1x40 Mode



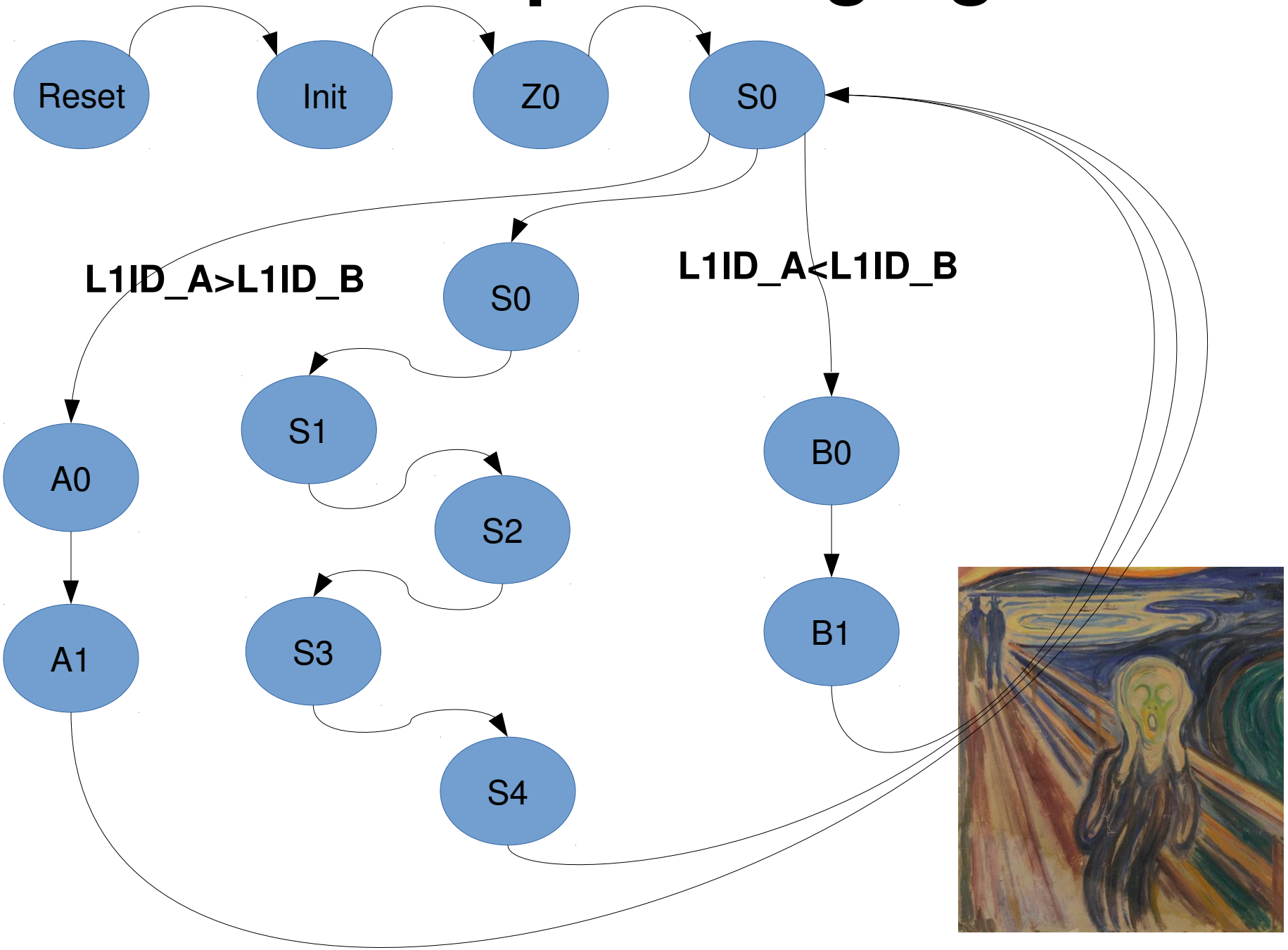
Slink Output Merging



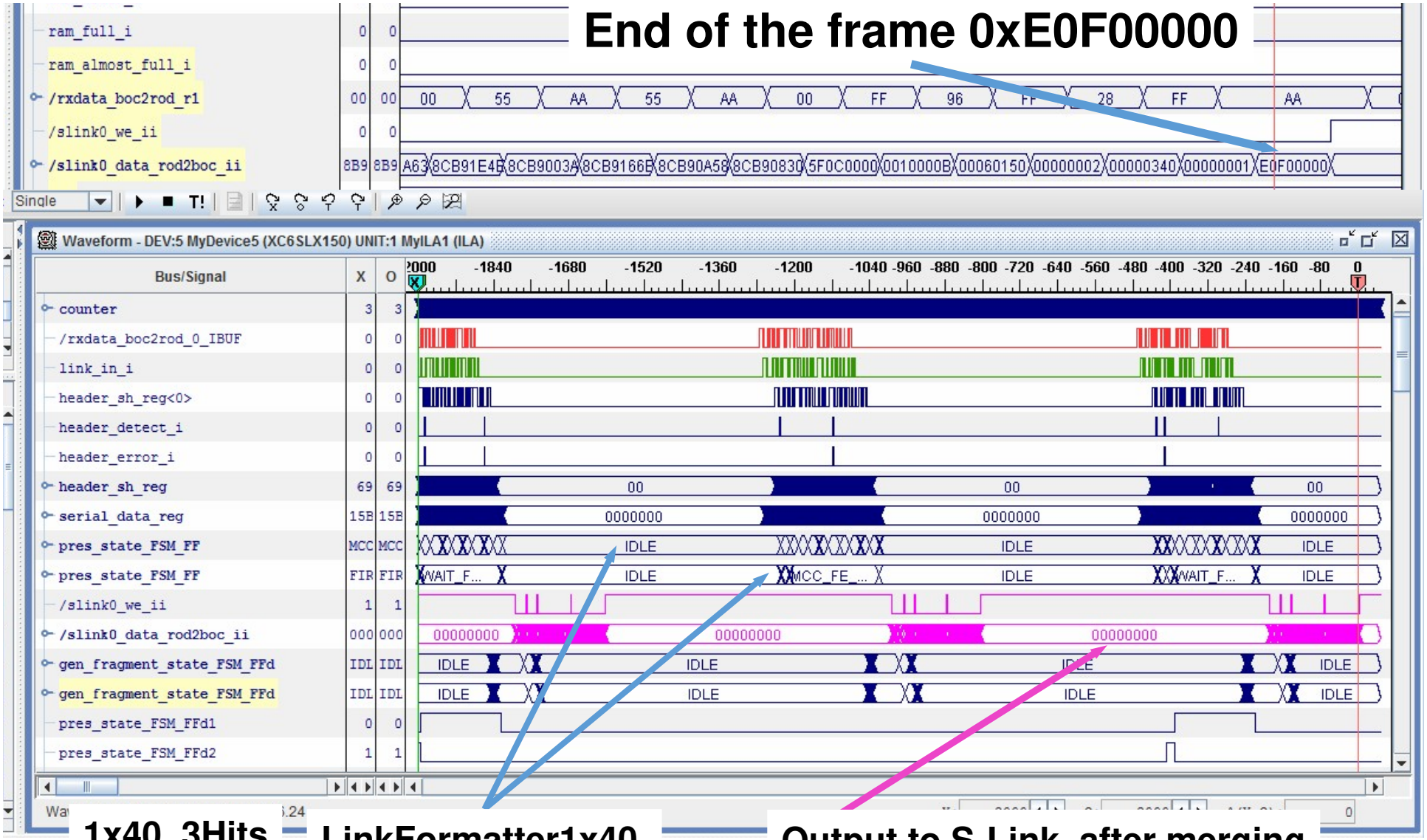
Main Sequence of the FSM:

1. (Z0) EXTRACT HEADERs from S-LINK0 and S-LINK1
2. (S0) COMPARE L1IDs
3. (S1) DROP the HEADER from S-LINK1 and SEND S-LINK0 HEADER
4. (S2) EXTRACT all data from S-LINK0
5. (S3) EXTRACT data from S-LINK1
6. (S4) MERGE Trailer S-LINK0 and S-LINK1 and CLOSE the fragment

Slink Output Merging



Slink Output Merging



TODO

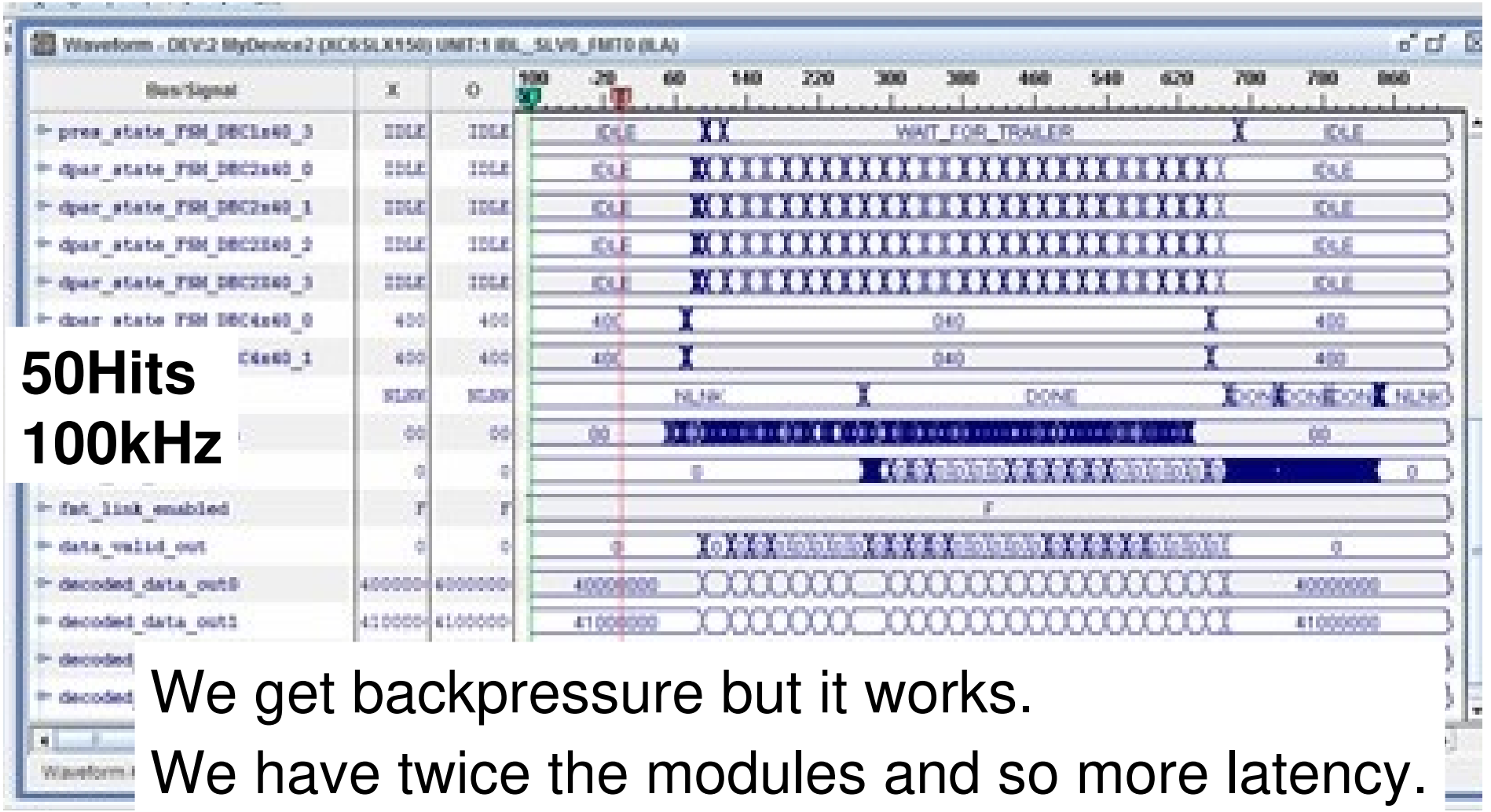
- Check FIFO sizes with real data.
- Check S-Link data quality:
  - Issues within the merging process.
  - Copy the address from hits to Header as per FEI3 format.
- Check the link mapping.

Thanks to all people who worked hard to achieve these results!

Gabriele Balbi
Davide Falchieri
Kazuki Todome
Riccardo Travaglini

Data Path

Formatters inputs and decoded outputs with 2x40 Mode

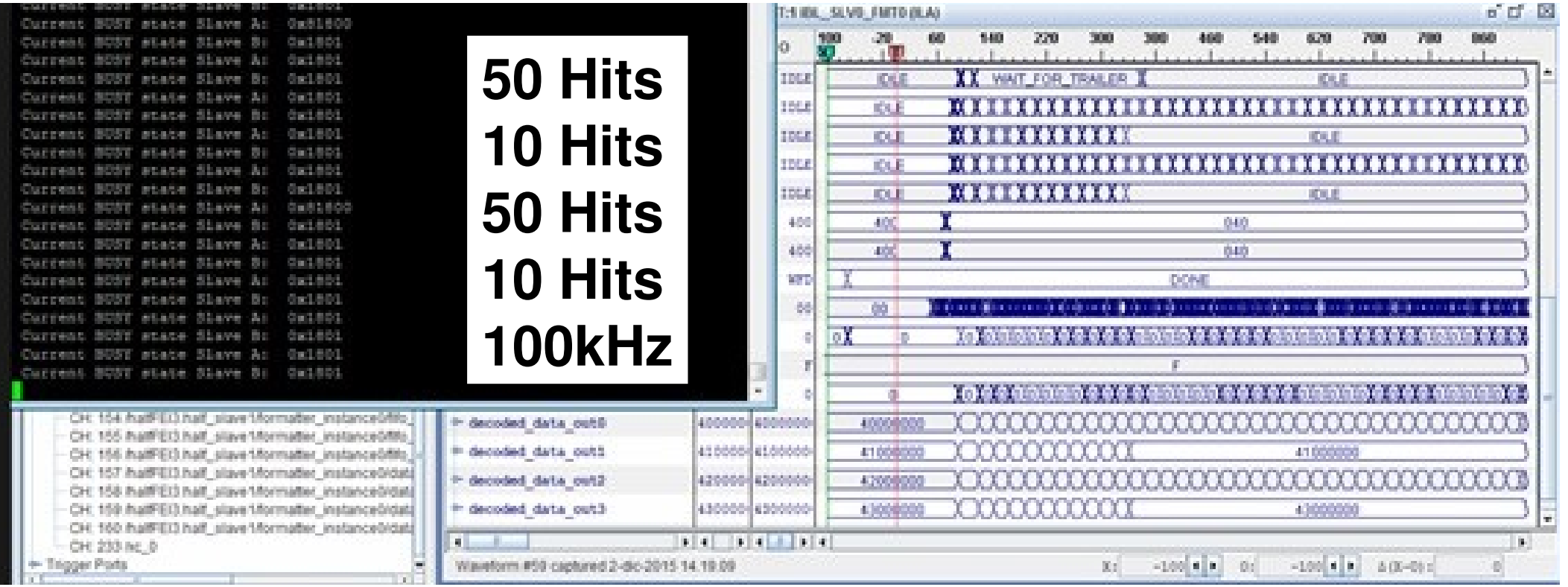


We get backpressure but it works.

We have twice the modules and so more latency.

Data Path

Formatters inputs and decoded outputs with 2x40 Mode



We do not go busy with unequal # of hit in different links.