**Tutorial 4**

**Compiling Pixel ROD Slave Firmware and generating bitfiles with ISE locally**

*March 2022*

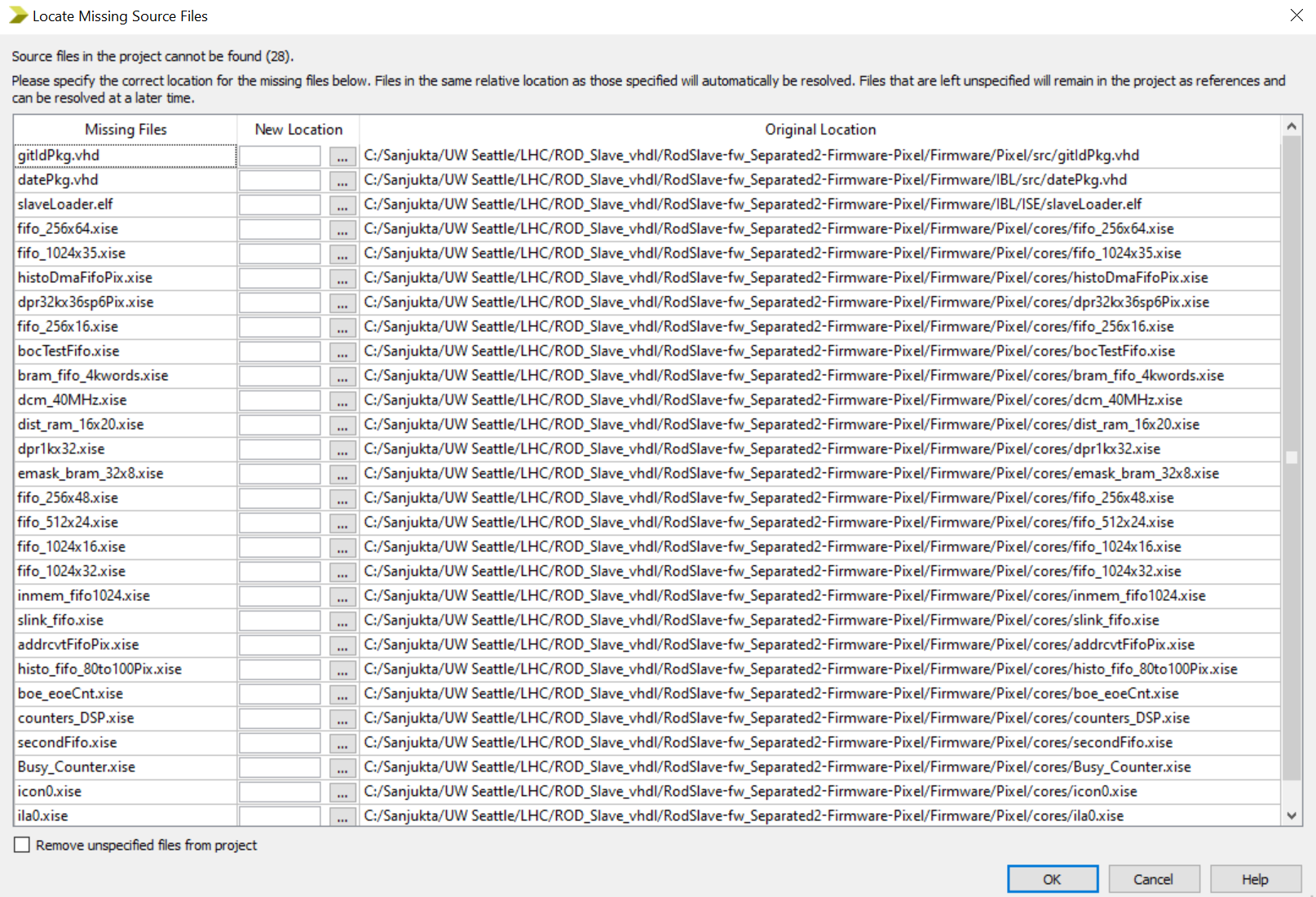
1. **Download the correct branch from git repo (fw\_Separated2 shown here)**

git clone --single-branch -b fw\_Separated2 <https://gitlab.cern.ch/atlas-pixel/daq/pixelrod_firmware/RodSlave>

Open the ISE project - Rodslave/Firmware/Pixel/ISE

The .xise ise projects are located here.

Since Spartan6 FPGAs are used, ISE Design Suite has to be used. In this tutorial we are using the slave firmware for calibration mode called **pixel\_rodSlave\_calibration.xise** . Upon first opening the project you may get a prompt called Locate Missing Source FIles. This will be solved in the next steps.



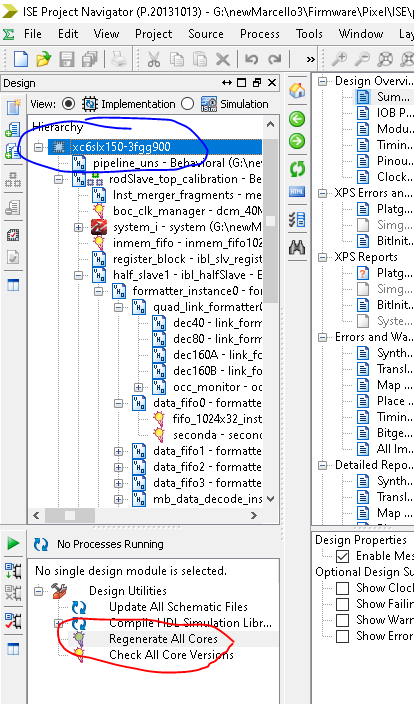
1. **Source git hash**

In order to generate the gitIDPkg.vhd you have to run the command "source hash2id.sh" from the Firmware/ directory (use git bash if on a windows machine)

source hash2id.sh

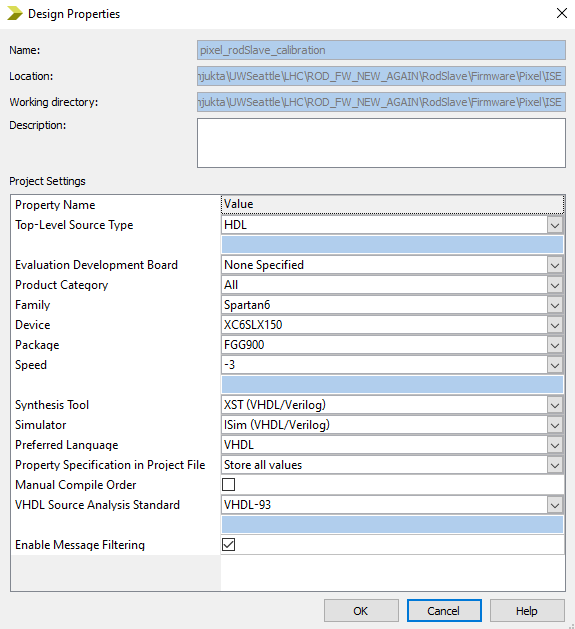
1. **Regenerate cores**

Regenerate all cores in the ISE project. This will get rid of the pop up.



1. **Check design properties**

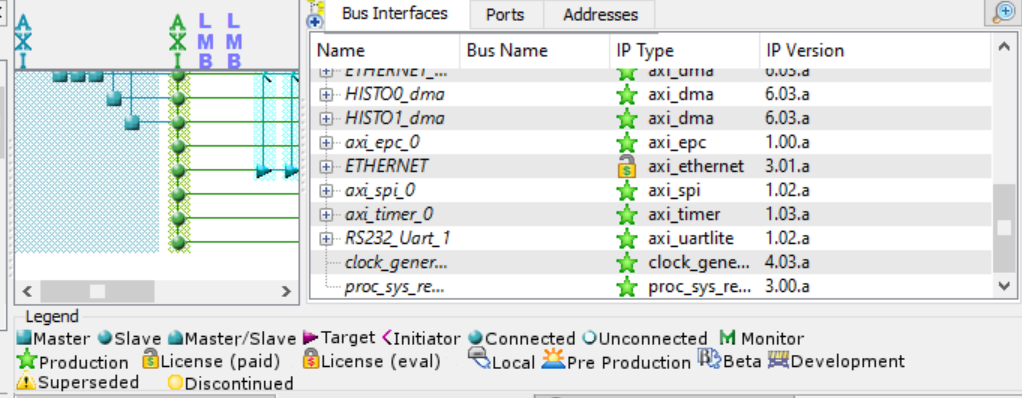
Ensure that it matches as below



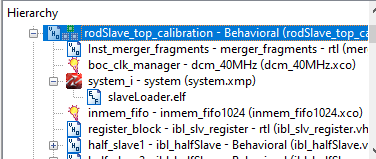
1. **system.xmp**

In order to do this step, the axi\_ethernet license is required. This license does not come with any full ISE or Vivado license options and has to be purchased separately. This is used for the microblaze

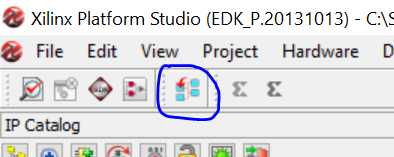
<https://www.xilinx.com/support/documentation/ip_documentation/axi_ethernet/v3_01_a/ds759_axi_ethernet.pdf>



Double click system\_i.xmp



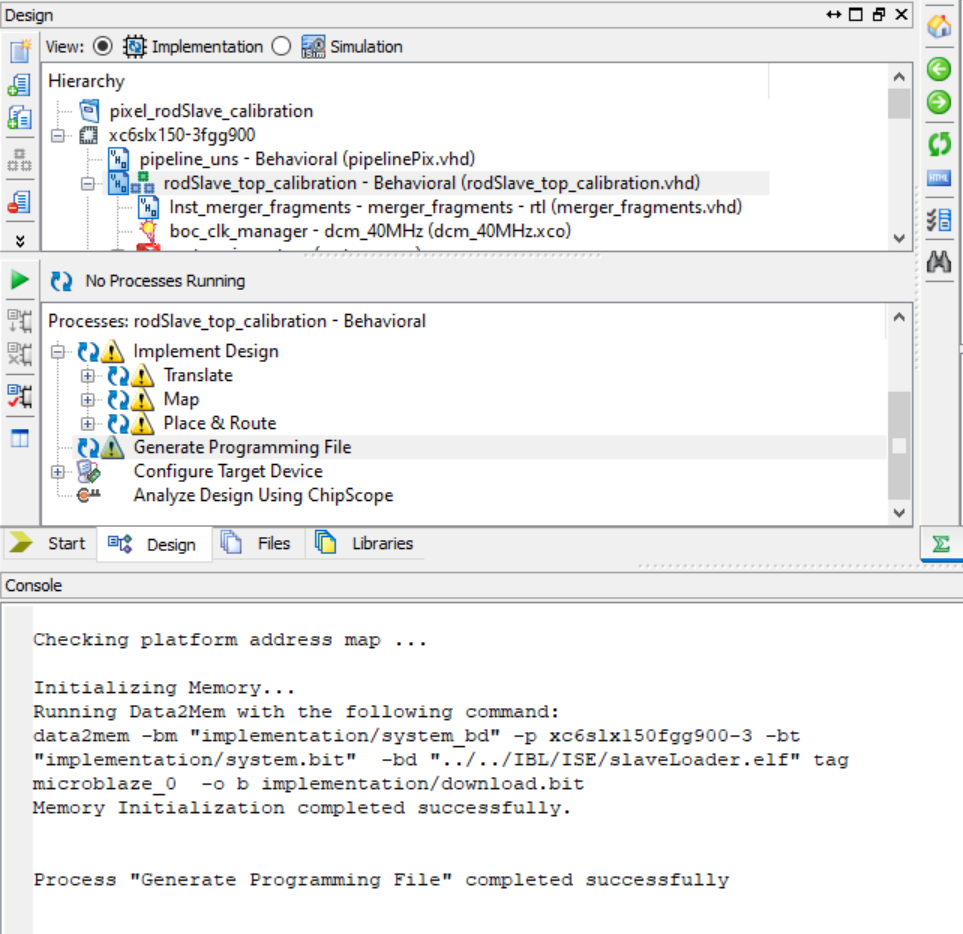
Platform studio will open, click on generate netlist there



Note that the path to the system.xmp has no spaces, if there are spaces there will be an error because XPS will not be able to read the file.

1. **Synthesize, implement, generate bitstream**

Select rodSlave\_top\_calibration and go through the synthesize, implement and generate bitstream steps. The warnings can be ignored.



The generated bitfile will appear in the folder of the. xise project.

In order to load this file in the modules at SR1, it has to be converted to .ace file which will be in another tutorial