

PHYS 234 Lab 2

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Output 1 if and only if at least two out of three inputs are 1

To implement this functionality, we set up the FPGA circuit board to have 3 input switches and 1 output LED. Whenever two switches are flipped to true, the LED would light up.

Verilog Code:

```
`timescale 1ns / 1ps
module eelab2(
    input a,
    input b,
    input c,
    output e
);

assign e = a&((b&~c)|(~b&c))|b&c;

endmodule
```

The results can be demonstrated using the truth table below. The 0s under A, B, and C represent when the switches are flipped to off, and 1s represent when the switches are on. In the output column, a 0 means the LED is off and 1 when the LED is on.

A	B	C	Output	Minterm	Maxterm
0	0	0	0	$\bar{A}\bar{B}\bar{C}$	$A + B + C$
1	0	0	0	$A\bar{B}\bar{C}$	$\bar{A} + B + C$
0	1	0	0	$\bar{A}B\bar{C}$	$A + \bar{B} + C$
0	0	1	0	$\bar{A}\bar{B}C$	$A + B + \bar{C}$
1	1	0	1	$A B \bar{C}$	$\bar{A} + \bar{B} + C$
1	0	1	1	$A\bar{B}C$	$\bar{A} + B + \bar{C}$
0	1	1	1	$\bar{A}B C$	$A + \bar{B} + \bar{C}$
1	1	1	1	$A B C$	$\bar{A} + \bar{B} + \bar{C}$

Using the sum of products (when minterms' output = 1), we can determine our circuit:

$$\begin{aligned}y &= ABC\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}C \\&= ABC\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{A}(BC) \\&= A(\bar{B}\bar{C} + \bar{B}C) + BC\end{aligned}$$

The above statement written in verilog code form will be “`a&((b&~c)|(~b&c))|b&c`”, and we assign this to our output variable e.

Additionally, we could also use the product of sums (when maxterms' output = 0) to determine the circuit, which will look like this:

$$y = (A + B + C)(\bar{A} + B + C)(A + \bar{B} + C)(A + B + \bar{C})$$

Both circuits would generate the same outcomes.

Output 1 if and only if a four-bit input represents a prime number

To implement this functionality, we set up the FPGA circuit board to have 4 input switches where each switch represents a digit in the 4-bit number. The value of the digits is 1 when the switches are flipped on and 0 when flipped off. The LED would light up whenever the 4-bit number is a prime number.

Verilog Code:

```
`timescale 1ns / 1ps
module eelab2(
    input a,
    input b,
    input c,
    input d,
    output e
);

assign e =
    (~a&b&~c&~d) | (a&b&~c&~d) | (a&~b&c&~d) | (a&b&c&~d) | (a&b&~c&d) | (a&~b&c&d)
;

endmodule
```

The results are demonstrated by the truth table below. It shows all combinations of the 4-digit input, its corresponding decimal number, and whether or not it is a prime number. We only record the minterms for the prime numbers as only they are needed to define our circuit.

D	C	B	A	Decimal	Prime?	Minterm
0	0	0	0	0	0	
1	0	0	0	8	0	
0	1	0	0	4	0	
0	0	1	0	2	1	$\bar{A}B\bar{C}\bar{D}$
0	0	0	1	1	0	
1	1	0	0	12	0	
0	1	1	0	6	0	
0	0	1	1	3	1	$A\bar{B}\bar{C}\bar{D}$
1	0	1	0	10	0	
1	0	0	1	9	0	
0	1	0	1	5	1	$A\bar{B}C\bar{D}$
1	1	1	0	14	0	
0	1	1	1	7	1	$A\bar{B}C\bar{D}$
1	0	1	1	11	1	$A\bar{B}\bar{C}D$
1	1	0	1	13	1	$A\bar{B}C\bar{D}$
1	1	1	1	15	0	

Using the sum of products (when minterms' output = 1) again, we can determine our circuit:

$$y = \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + AB\bar{C}\bar{D} + AB\bar{C}D + A\bar{B}CD$$

In verilog code, this will be

`"(~a&b&~c&~d)|(a&b&~c&~d)|(a&~b&c&~d)|(a&b&c&~d)|(a&b&~c&d)|(a&~b&c&d)"`, and we assign this to our output e again.

In this scenario, we would prefer to use the sum of products method rather than the product of sums method, because it is easier to sum 6 products with an output of 1 than to multiply 10 sums with an output of 0.