Ethan Bloom

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Education

The Pennsylvania State University – University Park, Pennsylvania **Expected May 2025**
Bachelor of Science in Computer Engineering Major GPA: 3.93

Experience

Undergraduate Researcher – Semiconductor Research Corporation (SRC) **August 2024 – Present**
Selected by the SRC and sponsored by Texas Instruments to participate in rigorous semiconductor research projects at Penn State

- Neuromorphic Computing Lab – Research and development of Ferroelectric Materials-based Devices and Circuits

Systems Engineering Intern – Multi-Dimensional Integration – Shrewsbury, PA **May 2024 – August 2024**
Developed various software and hardware system projects across the quotation, design, testing, and commissioning phases

- Composed $100,000+ quote documents and project proposals for multiple customers and their various design specifications
- Designed and produced complete hardware and software solutions, comprised of diverse logic programs and controllers

Project Engineering Intern – ProMinent Fluid Controls – Pittsburgh, PA **May 2023 – December 2023**
Integrated with project development teams, responsible for completing tasks for customer deliverables and documentation

- Optimized engineering calculation time by approximately 50% by creating spreadsheet tools with Visual Basic and Java

Projects

Digital ASIC Design and Layout – In-Progress **Cadence Virtuoso, HSPICE**
Individualized capstone project tailored to showcase design layout, implementation, and verification skills for digital design course

- Design layout and implementation realized through CAD tools; produced test specifications and review documentation

MIPS Five-Stage Pipelined Processor **VHDL, Xilinx Vivado**
Pipelined processor implements a 32-bit MIPS instruction set with a five-stage instruction cycle and forwarding/hazard logic

- Datapath integrates process modules and pipelining logic including handlers for branch prediction, forwarding, and hazards
- Memory controller arbitrates read and write data accesses to external memory/cache and supports variable-latency access
- Data and memory structures include 32-bit read-only instruction memory and 32-bit random access data memory modules
- Synthesizable through Xilinx Vivado and Vitis targeting the Zybo XC7Z010 – 1CLG400C development board

Dynamic Superscalar Instruction Scheduling Simulator **Vector Processing, Python, Bash**
Variable machine-width, out-of-order execution CPU simulator fetches arbitrary instructions and outputs 7-stage cycle timings

- Pipeline implements single-cycle register renaming and dependency checking across instructions in decoded buffer cache
- Re-order buffer and dynamic issue queue enable instruction selection and wake-up during issue and execute/writeback stages

Multiple Disk and Device Management Utility **C, Make, Ubuntu**
Software utility for accessing 16-disk linear device, implemented in C targeting 64-bit Linux devices operating on Ubuntu

- Memory access time improvement via application-specific single level cache hierarchy with LRU and write-through policies
- Validation testing suite built with make utility, consisting of unit tests and trace files for comprehensive scenario verification

Knowledge/Skills

- Digital IC/ASIC VLSI design, layout, and testing using Cadence CAD software in computer and hardware lab environments
- FPGA-based RTL design, simulation, and verification in Verilog HDL using Xilinx Vivado and Quartus Prime with MultiSim
- Design, transient analysis, and power performance evaluation of combinational, sequential, memory, and arithmetic circuits
- Digital and analog circuit and PCB design, simulation, and layout planning in NI Multisim and KiCad electronics design suites
- System, firmware, and embedded programming in C, C++, and Assembly languages, Scripting in bash, Python, and JavaScript

Involvement

Eta Kappa Nu, Institute of Electrical and Electronics Engineers (IEEE) Student Honors Society

- Coached undergraduate students in computer science and electrical engineering topics during department tutoring sessions