Ethan Bloom

ethantbloom@gmail.com | (412) 315-9130 | linkedin.com/in/ethan-bloom-PSU-CompEng | ethanbloom.github.io

Education

The Pennsylvania State University – University Park, Pennsylvania **Expected May 2025**
Bachelor of Science in Computer Engineering Major GPA: 3.93

Professional Experience

Project Engineering Intern – ProMinent Fluid Controls – Pittsburgh, PA **May 2023 – December 2023**
Responsible for integrating with project development teams, completing tasks for customer deliverables and documentation

- Improved customer acquisition and retention rates by developing multi-platform online parametric modeling system
- Optimized engineering calculation time by approximately 50% by creating spreadsheet tools with Visual Basic

Projects

Multiple Disk and Device Management Utility **C, Make, Ubuntu**
Software utility for accessing 16-disk linear device, implemented in C targeting Linux devices operating on Ubuntu

- Implemented API functionality that interfaces with single-function device driver for executing firmware operations
- Linear device mounting and un-mounting process allows for 256-byte per block read and write operations
- Memory access time improvement via application-specific single level cache with LRU and write-through policies
- Testing suite built with make utility, consisting of unit tests and trace files for comprehensive scenario verification

MIPS Five-Stage Pipelined Processor **VHDL, Xilinx Vivado**
Pipelined processor implementing the 32-bit MIPS instruction set with a five-stage cycle and forwarding/hazard logic

- Datapath integrates modules and pipelining logic including handlers for branch prediction, forwarding, and hazards
- Memory controller arbitrates read/write memory accesses to external memory and supports variable-latency access
- Data and memory structures include 32-bit read-only instruction memory and 32-bit random access data memory
- Synthesizable through Xilinx Vivado and Vitis targeting the Zybo XC7Z010 – 1CLG400C development board

Dynamic Superscalar Instruction Scheduling Simulator **Python, Bash, Make**
Variable machine-width out-of-order instruction simulator reads arbitrary instructions and outputs 7-stage cycle timings

- Pipeline implements full register renaming and dependency checking among instructions in decoded buffer
- Re-Order Buffer and Issue Queue handle instruction selection and wake-up via Issue stage and Execute/Writeback
- Conservative load-store ordering in load-store queue assumes all possible dependencies must be respected

Knowledge/Skills

- FPGA RTL design, simulation, and verification in Verilog HDL using Xilinx Vivado and Quartus Prime with MultiSim
- Digital and analog circuit design, simulation, and layout planning in NI Multisim and KiCad electronics design suites
- ASIC design including state machines, combinational, and sequential logic in computer and hardware lab environments
- System Programming in C/C++ and Assembly; Programming in Java, JS, and MATLAB; Scripting in bash and Python

Involvement

Eta Kappa Nu, Institute of Electrical and Electronics Engineers (IEEE) Student Honors Society

- Coached undergraduate students in computer science and engineering topics during department tutoring sessions

Nittany Motorsports, Low Voltage Electronics Team

- Designed analog and digital circuits for various controls/sensor systems, then produced PCB layout designs

IEEE Penn State Chapter

- Developed and improved technical skills and project methods through group workshops and team study sessions