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Lab 2

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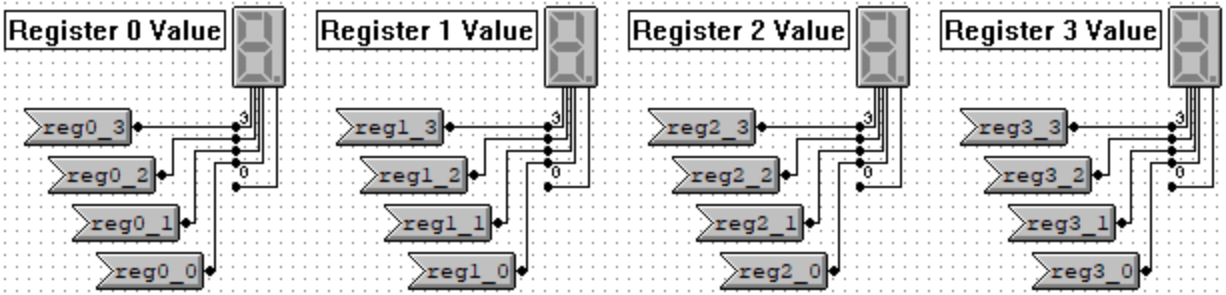
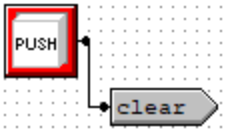
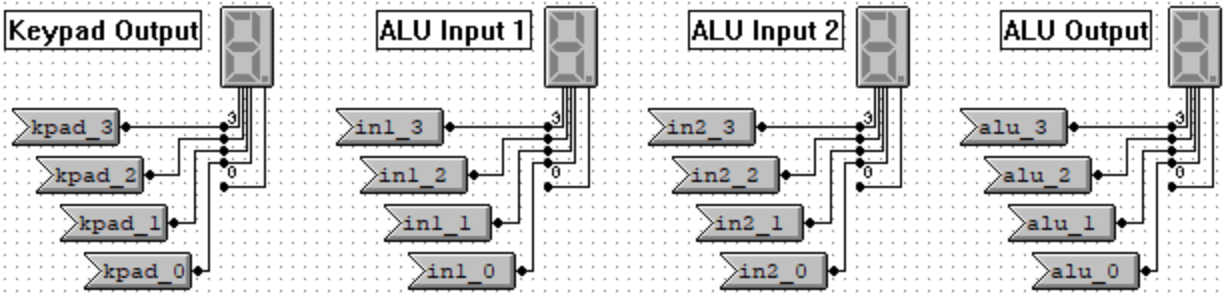
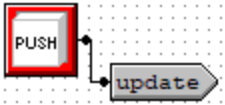


Clear Registers



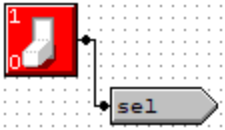


Update Register

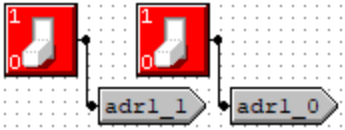


Store Select

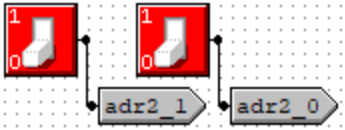
0 = Keypad input, 1 = ALU result



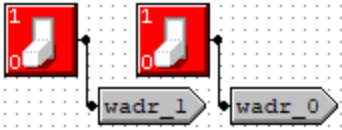
Read Register 1 Address

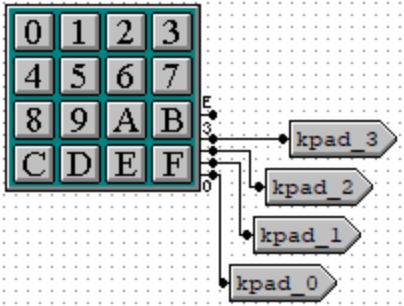


Read Register 2 Address



Write Register Address





Select clear to initialize registers to 0.

Select store select to choose which value to store.

Choose read and write register addresses.

Read addresses = reg sources of ALU inputs, Write address = reg to save to

Press update to save value to register

You are only permitted to modify the header comment on this page.

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Register Page 1

Lab 2 Flip/Flops that take the keypad output and selected register if triggered then takes bit to Register Display Page

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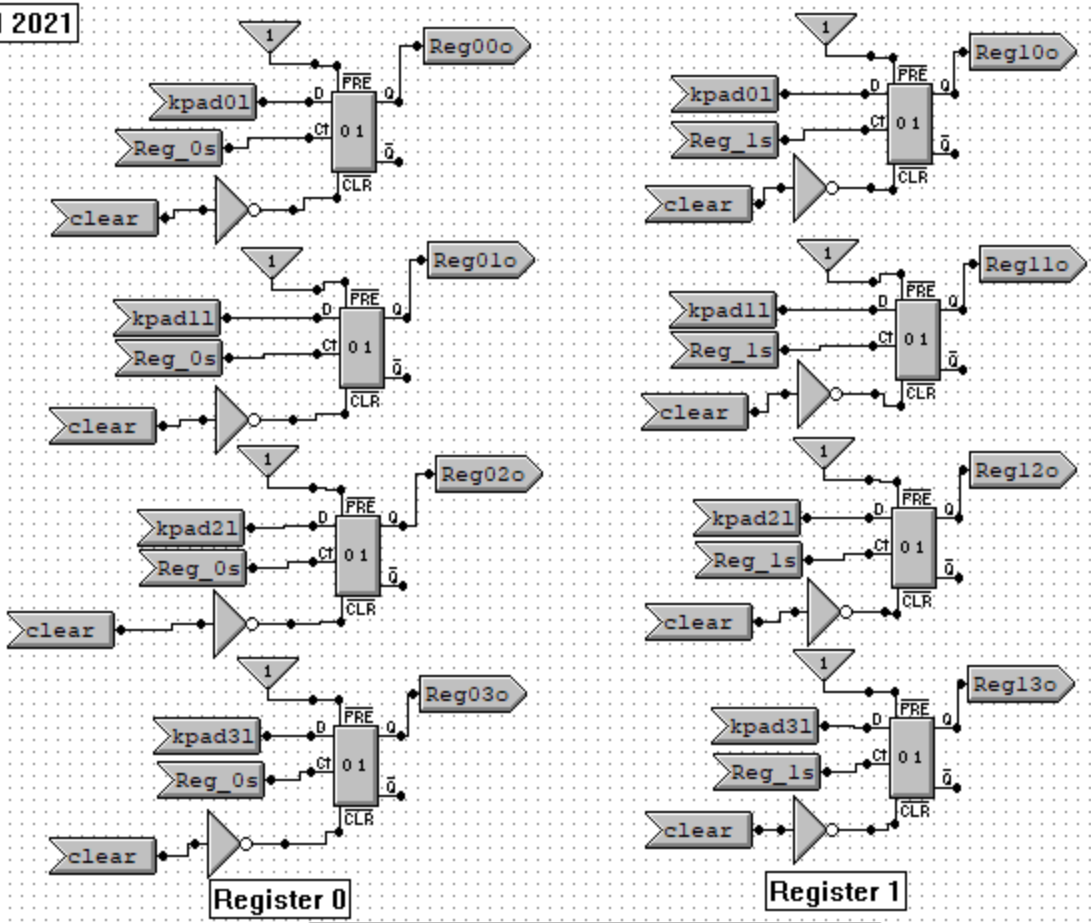

Also include clear functions and default to 0

Page for Registers 0 and 1

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Register Page 2

Lab 2 Flip/Flops that take the keypad output and selected register if triggered then takes bit to Register Display Page

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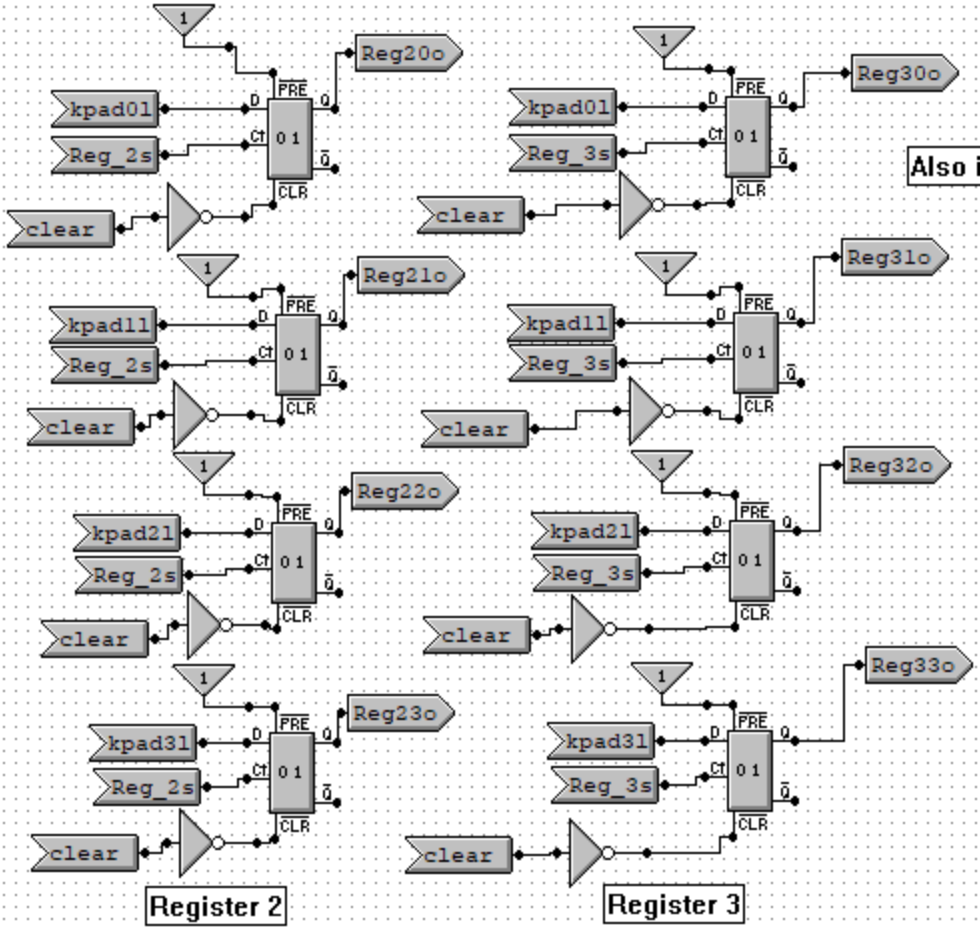

Also include clear functions and default to 0

Page for Registers 2 and 3

Register 2

Register 3

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Lab 2

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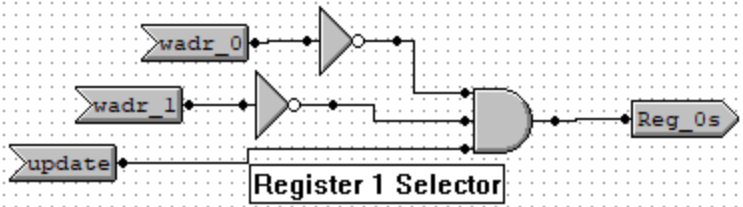
Register Selector Logic

Uses AND to gates decide selected register

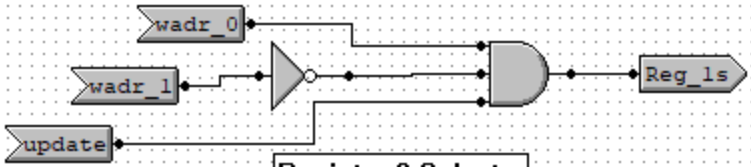
Depending on selected write address and if update was pressed to decide

Which register was chosen to write on

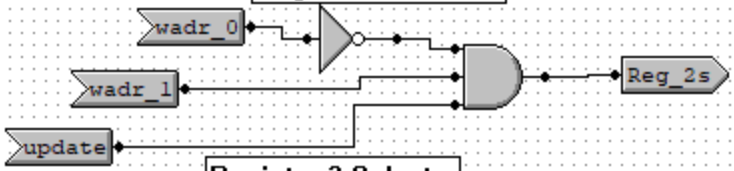
Register 0 Selector



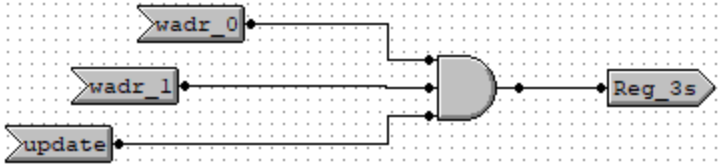
Register 1 Selector



Register 2 Selector



Register 3 Selector



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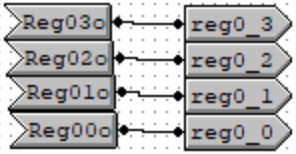
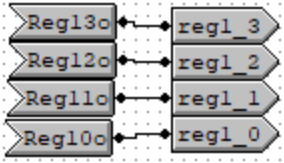
Register Display Page Logic

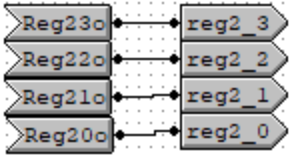
Carries Logic from registers 0-4 and assigns each bit a sender for the respective display bit



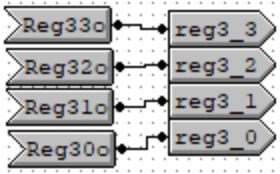
Register 0 Display Logic



Register 1 Display Logic



Register 2 Display Logic



Register 3 Display Logic

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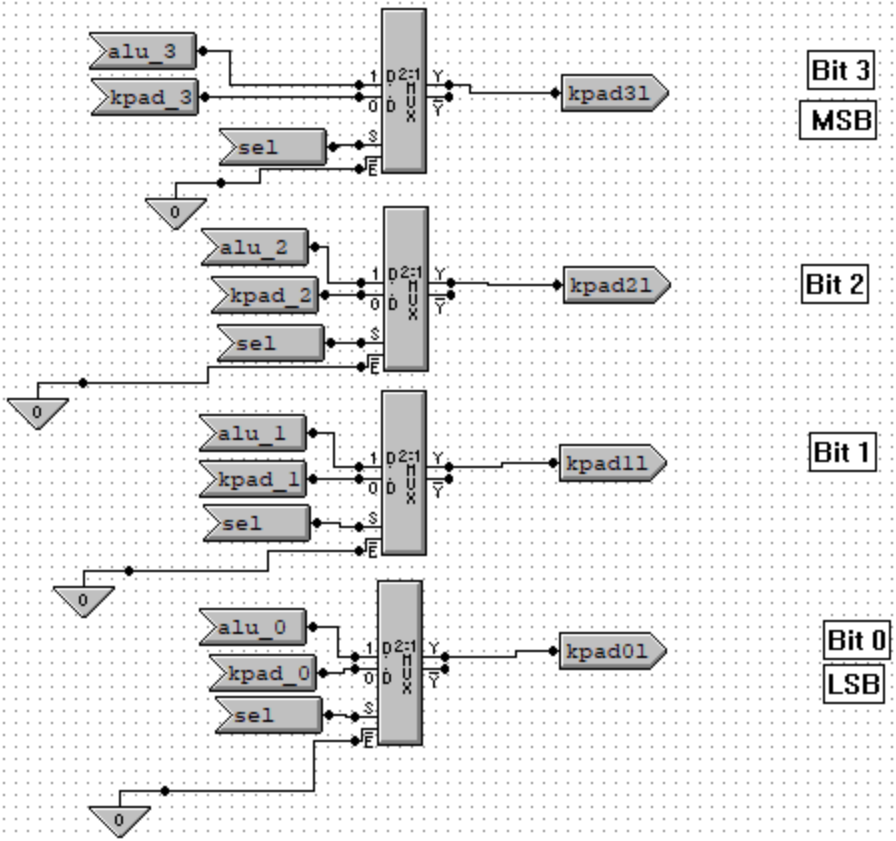
Keypad Select Page Logic



Muxes that use saved ALU Output and Keypad output with select latch as trigger

Bases at output 0 and will use bit output for Register input to display and store

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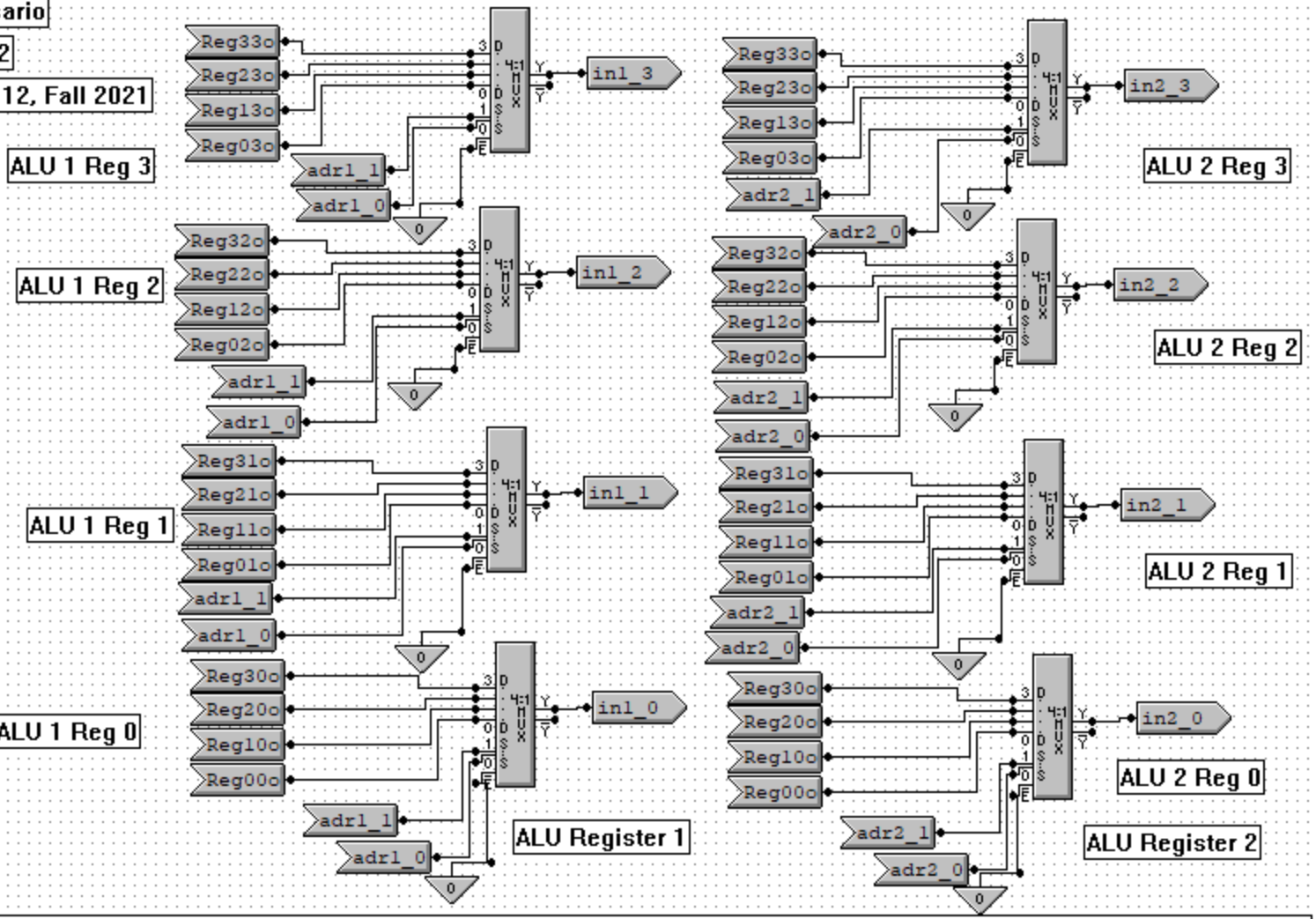
ALU Selector Page with Read Addresses



Takes outputs from all registers, then uses MUXs and Read Adresses 1 and 2 to decide which Registers values will be ALU Input 1 or 2. Output is ALU 1 and 2 bits 0-4

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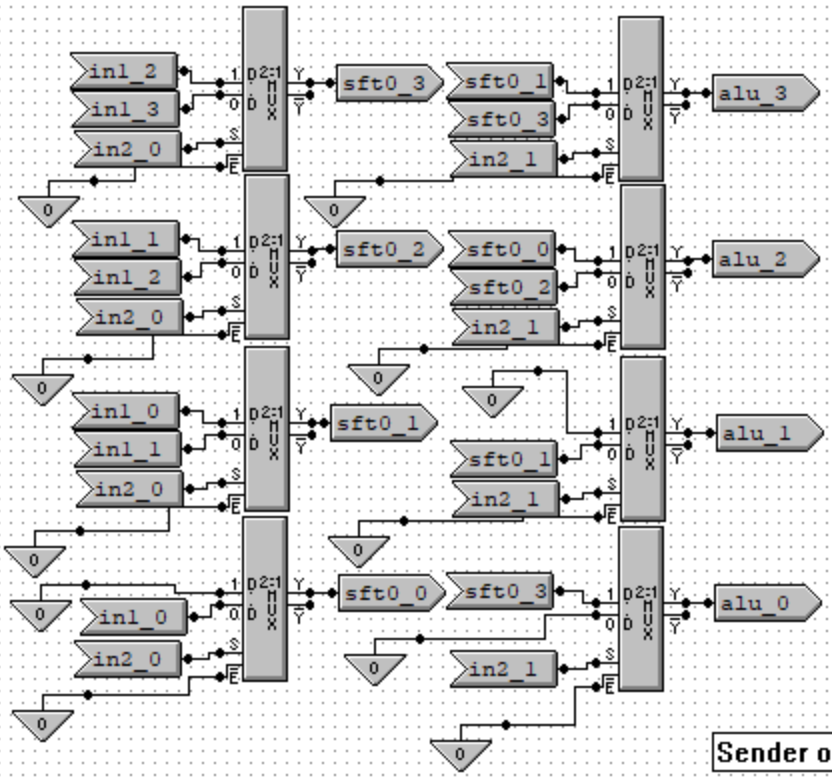
ALU Circular Left Shift Logic



Each bit has 2 MUX, first will rotate one

Second will rotate two

Sender outputs in second column is used for ALU output Display

First Rotation

Second Rotation

Takes Inputs from ALU 1 then uses muxes to shift each bit if ALU 2 bit is 1

Output from first rotation will then be used for possible rotation 2