1.

Lab 1 - Department of Electrical Engineering and Computer Science

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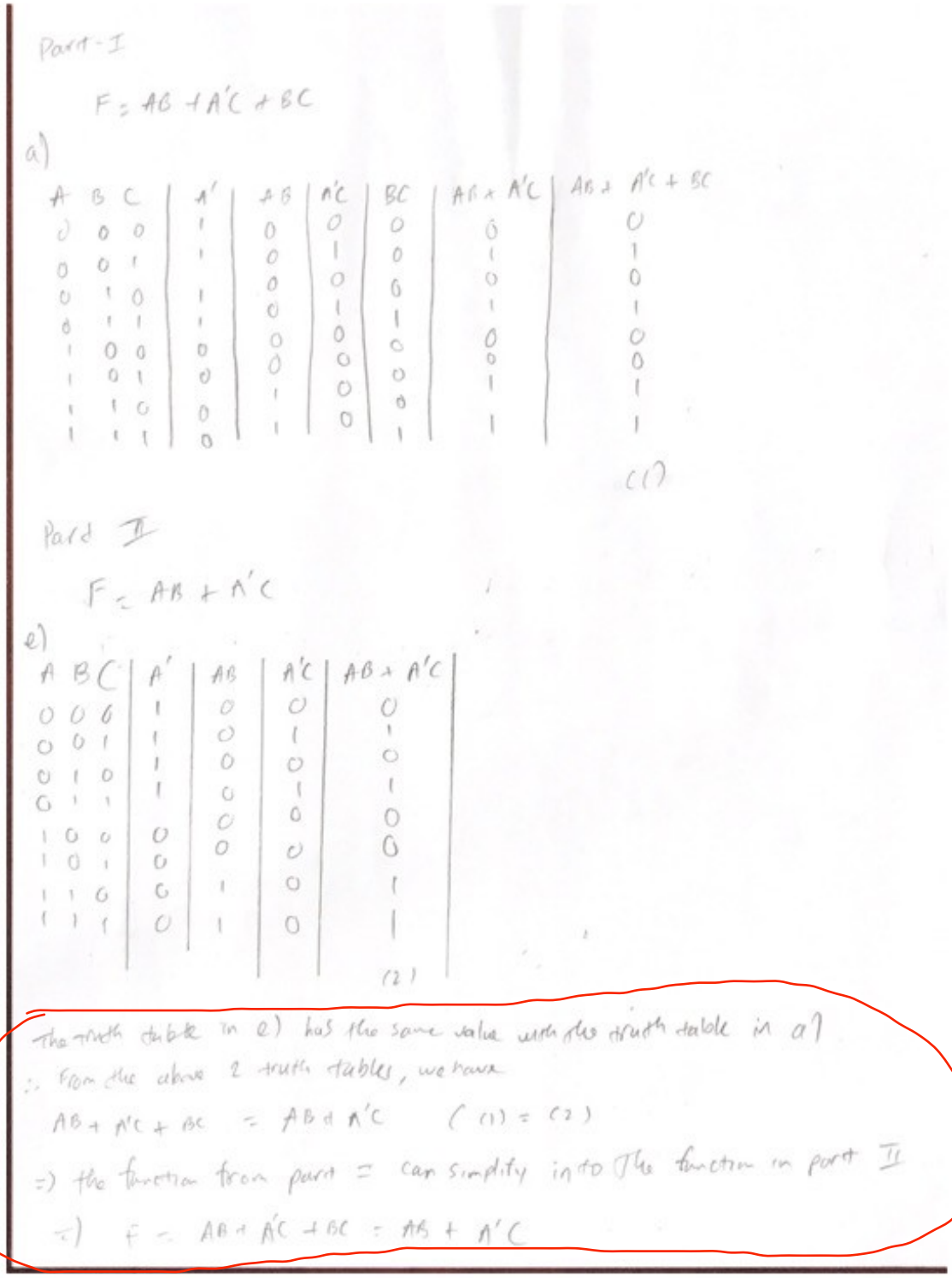
Switch. Cir. & Log Desgn Lab

29 January 2022

2.

Purpose of Experiment: Get use to Quartus and truth table of the Boolean function.

Design and Implementation Procedure: First, we have to derive the truth table for the Boolean function. Then use the truth table to draw the circuit for part I. Then from the circuit we do the schematics on Quartus by adding components such as AND2, OR3, INPUT, ETC. After do the schematics, we run the program to see if there are any errors. If not, then we do the waveform. We figure out and set up the end time, grid size, and clock to get the result similar waveform as lab 1. Then we put the pin planner for input A,B,C and output F and plug in the DE2-115 board and demonstrate it to Professor.



Part - I

$F = AB + A'C + BC$

a)

A	B	C	A'	AB	A'C	BC	AB + A'C	AB + A'C + BC
0	0	0	1	0	0	0	0	0
0	0	1	1	0	1	0	1	1
0	1	0	1	0	0	0	0	0
0	1	1	1	0	1	1	1	1
1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	1	0	0	1	0	0	1	1
1	1	1	0	1	0	1	1	1

(1)

Part II

$F = AB + A'C$

e)

A	B	C	A'	AB	A'C	AB + A'C
0	0	0	1	0	0	0
0	0	1	1	0	1	1
0	1	0	1	0	0	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	0	1	0	1

(2)

The truth table in e) has the same value with the truth table in a)

∴ From the above 2 truth tables, we have

$AB + A'C + BC = AB + A'C$ ((1) = (2))

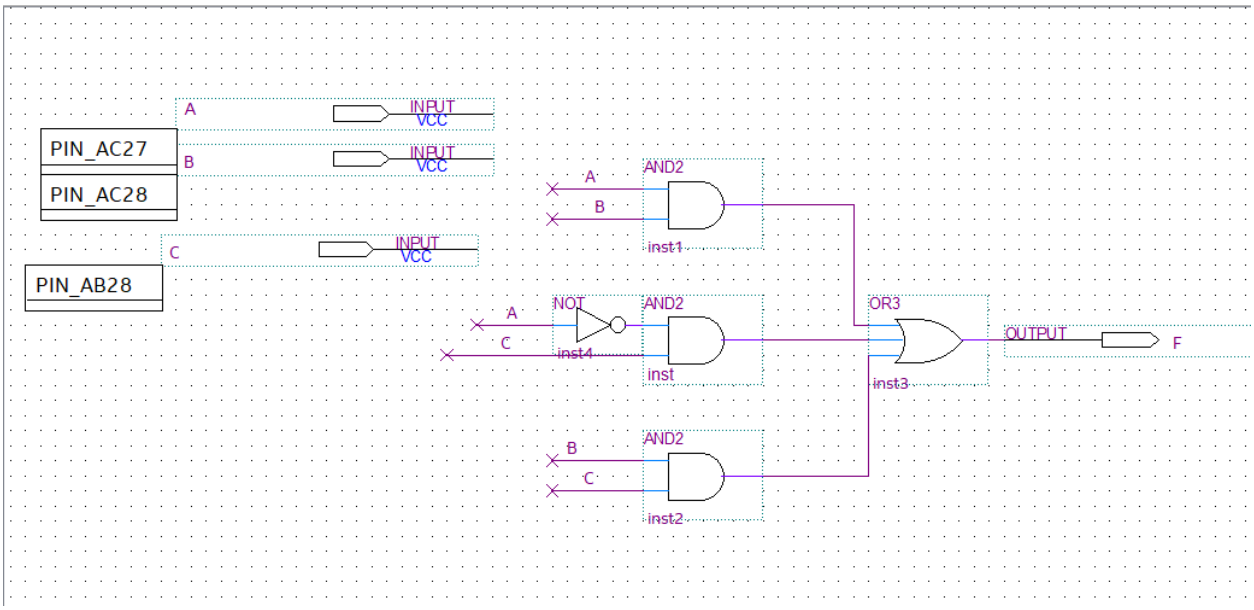
⇒ the function from part I can simplify into the function in part II

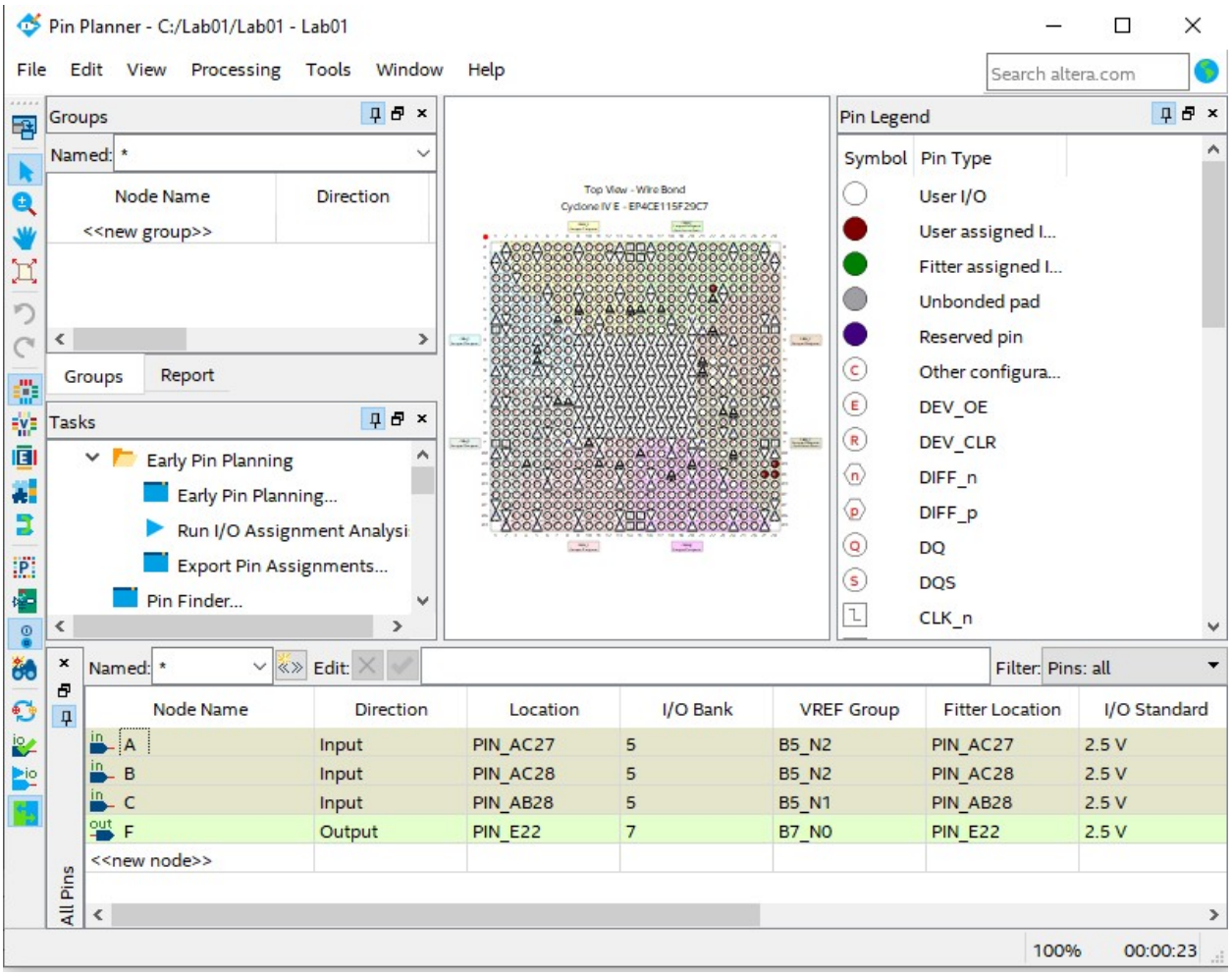
⇒ $F = AB + A'C + BC = AB + A'C$

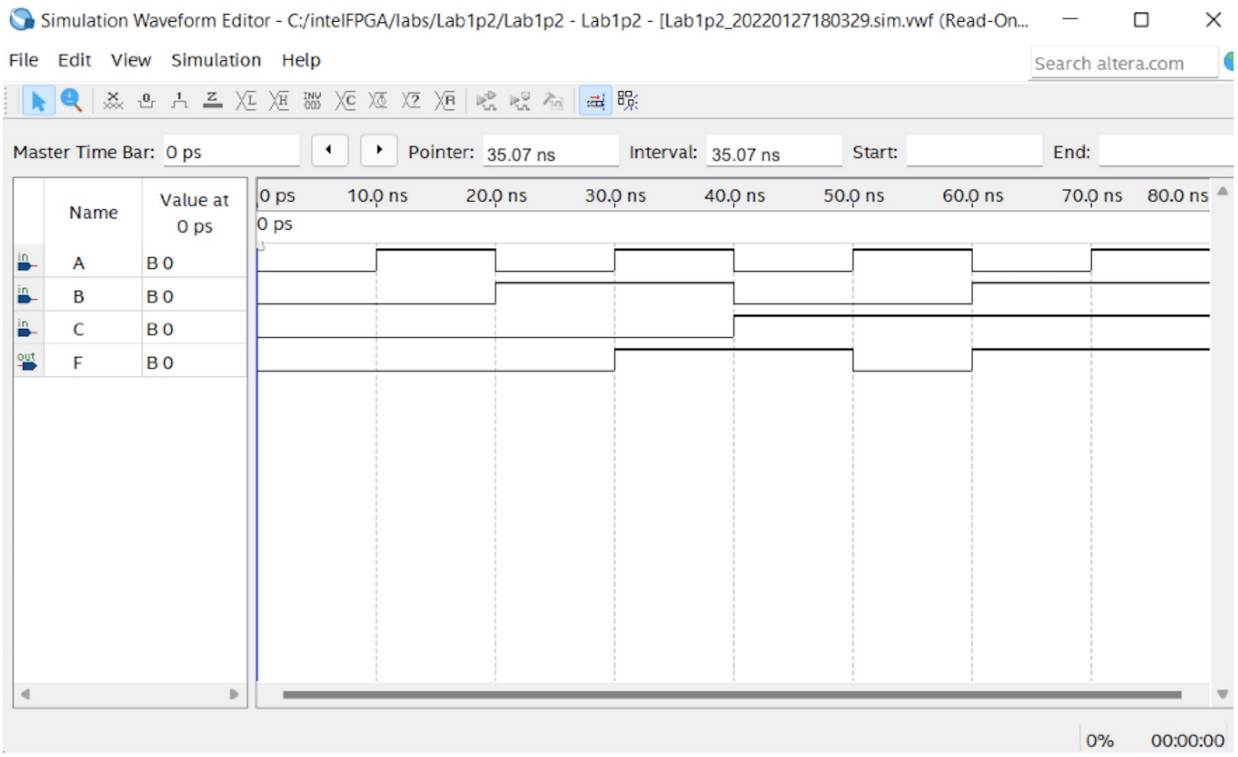
lab requirement is using Boolean theorems to simplify the function.

3.

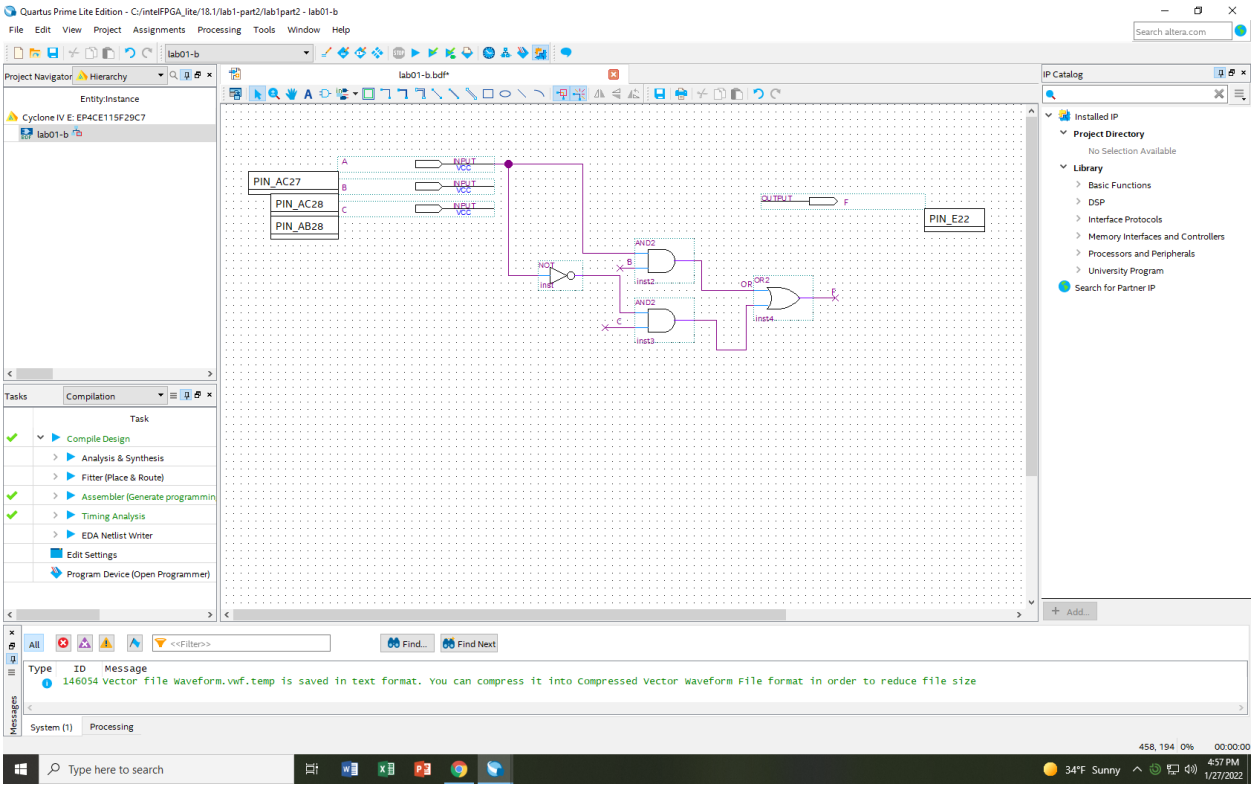
Part I – Schematics, Pin planner, waveform

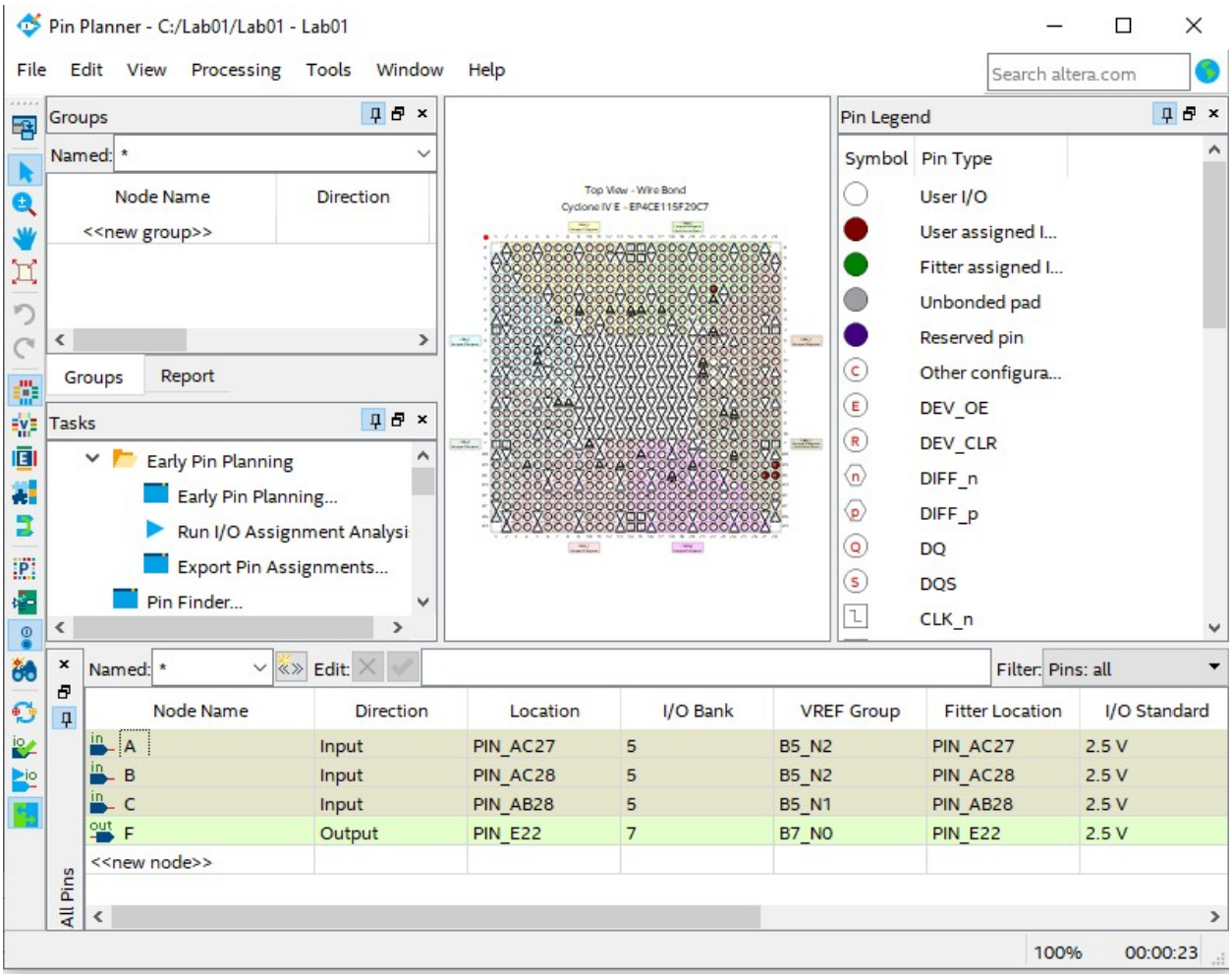


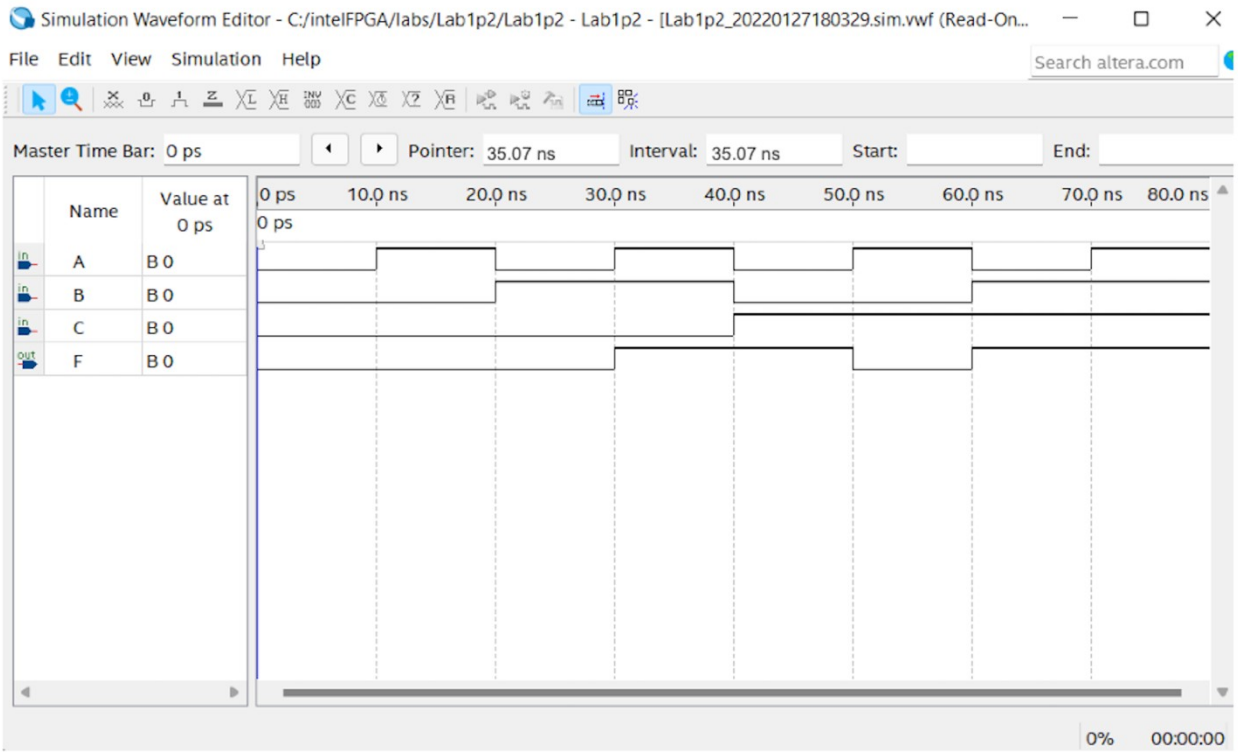

Pin Planner - C:/Lab01/Lab01 - Lab01
File Edit View Processing Tools Window Help
Search altera.com
Groups
Named: *
Node Name Direction
<<new group>>
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Run I/O Assignment Analysi
Export Pin Assignments...
Pin Finder...
Top View - Wire Bond
Cyclone IV E - EP4CE115F29C7
Pin Legend
Symbol Pin Type
User I/O
User assigned I...
Fitter assigned I...
Unbonded pad
Reserved pin
Other configura...
DEV_OE
DEV_CLR
DIFF_n
DIFF_p
DQ
DQS
CLK_n
Named: * Edit: Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard
A Input PIN_AC27 5 B5_N2 PIN_AC27 2.5 V
B Input PIN_AC28 5 B5_N2 PIN_AC28 2.5 V
C Input PIN_AB28 5 B5_N1 PIN_AB28 2.5 V
F Output PIN_E22 7 B7_N0 PIN_E22 2.5 V
<<new node>>
All Pins
100% 00:00:23



Part II – Schematics, pin planner, waveform


Quartus Prime Lite Edition - C:/intelFPGA_lite/18.1/lab1-part2/lab1part2 - lab01-b
File Edit View Project Assignments Processing Tools Window Help
lab01-b.bdf*
PIN_AC27
PIN_AC28
PIN_AB28
PIN_E22
INPUT
OUTPUT
AND2
NOT
OR2
Cyclone IV E: EP4CE115F29C7
lab01-b
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programmin
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
146054 Vector file Waveform.vwf.temp is saved in text format. You can compress it into Compressed Vector Waveform File format in order to reduce file size
Type here to search
34°F Sunny
4:57 PM
1/27/2022


Pin Planner - C:/Lab01/Lab01 - Lab01
File Edit View Processing Tools Window Help
Search altera.com
Groups
Named: *
Node Name Direction
<<new group>>
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Run I/O Assignment Analysi
Export Pin Assignments...
Pin Finder...
Top View - Wire Bond
Cyclone IV E - EP4CE115F29C7
Pin Legend
Symbol Pin Type
User I/O
User assigned I...
Fitter assigned I...
Unbonded pad
Reserved pin
Other configura...
DEV_OE
DEV_CLR
DIFF_n
DIFF_p
DQ
DQS
CLK_n
Named: * Edit: Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard
A Input PIN_AC27 5 B5_N2 PIN_AC27 2.5 V
B Input PIN_AC28 5 B5_N2 PIN_AC28 2.5 V
C Input PIN_AB28 5 B5_N1 PIN_AB28 2.5 V
F Output PIN_E22 7 B7_N0 PIN_E22 2.5 V
<<new node>>
All Pins
100% 00:00:23



4.

Lessons Learned: Learning how to do schematics, waveform, pin on Quartus and truth table of the Boolean function. Learning how to simplify the Boolean function from the truth table