CSC 327 – Lab 4

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Course Name: CSC 327

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Experiment Description

In this Lab you are to design a BCD to Seven-segment display driver circuit that will take BCD number as input and display the corresponding decimal value of BCD input on a Seven-segment display, as shown in Figure 1. For undesired inputs (i.e. inputs from 1010 to 1111) the circuit will display **U** on the Seven-segment display.

Each of the seven segments is labeled **a** through **g**. The numbers 0 through 9 light up the segments shown in Figure 2. For example, the number 0 lights up all but the middle segment, segment **g**. There are two types of 7-segment display available in the market. One is common anode and the other is common cathode. In DE2-115 board, the manufacturer used the **common anode** type display. To turn on a common anode display segment, you have to provide a low signal (0). For example, to turn on segment **a**, you have to provide a low signal (0) to the corresponding pin of segment **a**.

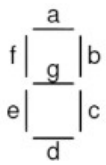


Figure 1. Seven-segment display

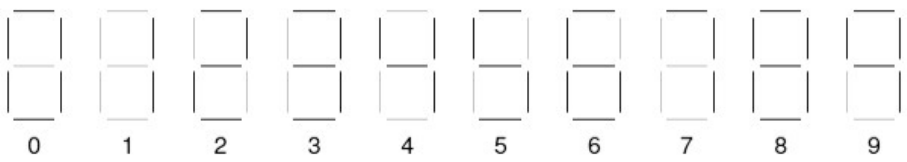


Figure 2. Seven-segment display Function

To design your seven-segment display decoder, you will first write the truth table specifying the output values for each input combination. For example, when the input is ABCD = 0000, the outputs are **abcdefg**= 0000001 and when the input is ABCD=1010 (undesired input), the outputs are **abcdefg** = 1000001 (display **U**).

Deliverable:

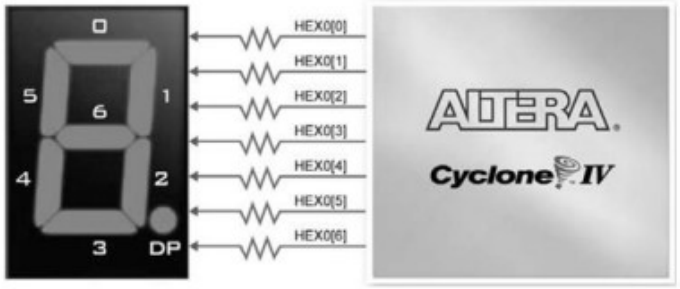
a) Write the **truth table** and **derive the expression** for **a,b,c,d,e,f,** and **g** using four variable K-map.

b) Design a digital circuit in Quartus II that will satisfy the truth table you derived in (a).

c) Simulate your design and justify that your design functions properly.

d) Once you are satisfied with your design, download your design in the DE2-115 board and verify that your circuit functions properly according to the design objective.
For inputs use ***SW3, SW2, SW1,*** and ***SW0*** as **A, B, C,** and **D** respectively. For outputs, use **HEX0** Seven-segment display of your DE2-115 board**.**
(** use DE2-115 user manual to do the necessary pin assignment for this design)

Figure 3 shows the internal connection between the HEX0 and Cyclone IV E. In your design HEX0[0] is represented as **a,** and HEX0[1] as **b,** and so on.



Signal Name	*FPGA Pin No.*
HEX0[0]	PIN_G18
HEX0[1]	PIN_F22
HEX0[2]	PIN_E17
HEX0[3]	PIN_L26
HEX0[4]	PIN_L25
HEX0[5]	PIN_J22
HEX0[6]	PIN_H22

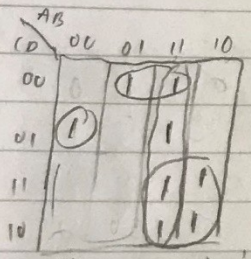
Figure 3 Connections between the 7-segment display HEX0 and Cyclone IV E FPGA

Experimental Results

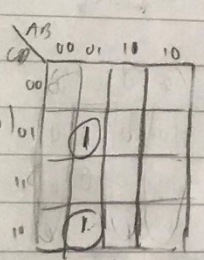
Truth table and derive the expression for a,b,c,d,e,f, and g using four variable K-map

	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0
10	1	0	1	0	1	0	0	0	0	0	1
11	1	0	1	1	1	0	0	0	0	0	1
12	1	1	0	0	1	0	0	0	0	0	1
13	1	1	0	1	1	0	0	0	0	0	1
14	1	1	1	0	1	0	0	0	0	0	1
15	1	1	1	1	1	0	0	0	0	0	1

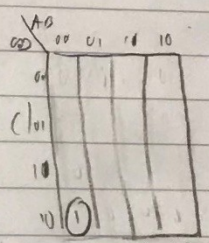
a)



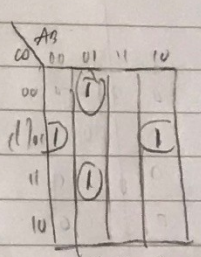
a= AB+AC + BC'D'+AB'C'D



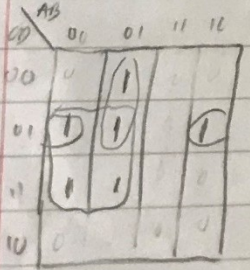
b=a'bc'd + a'bcd'



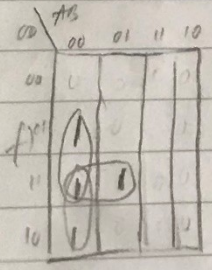
c= a'b'cd'



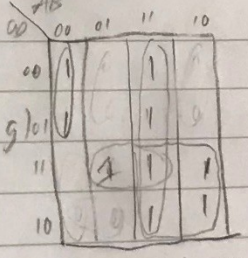
d=b'c'd+a'bc'd'+ a'bcd



e= A'D+ A'bc'+ B'C'D

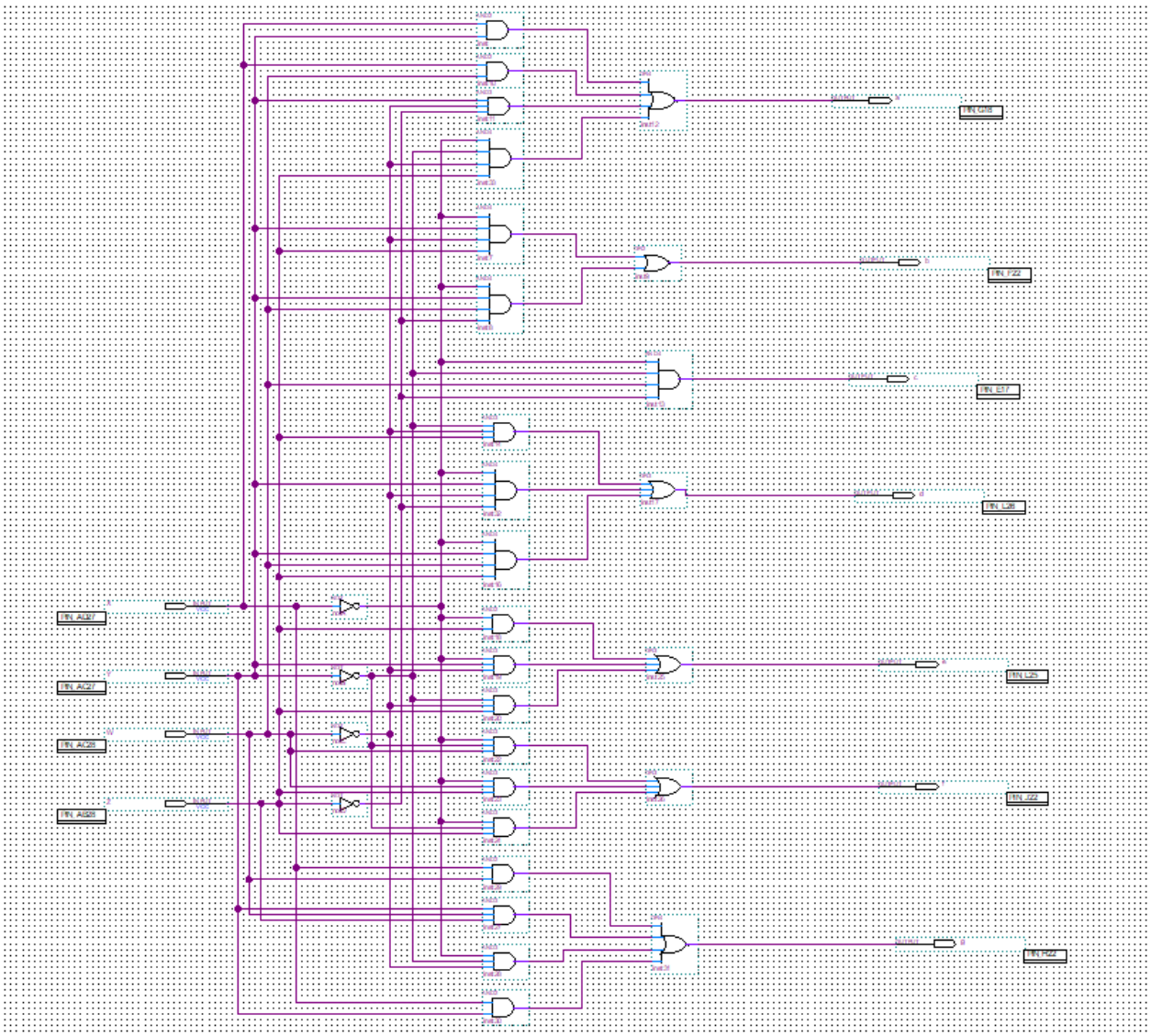


f= A'BC+A'CD +A'B'D

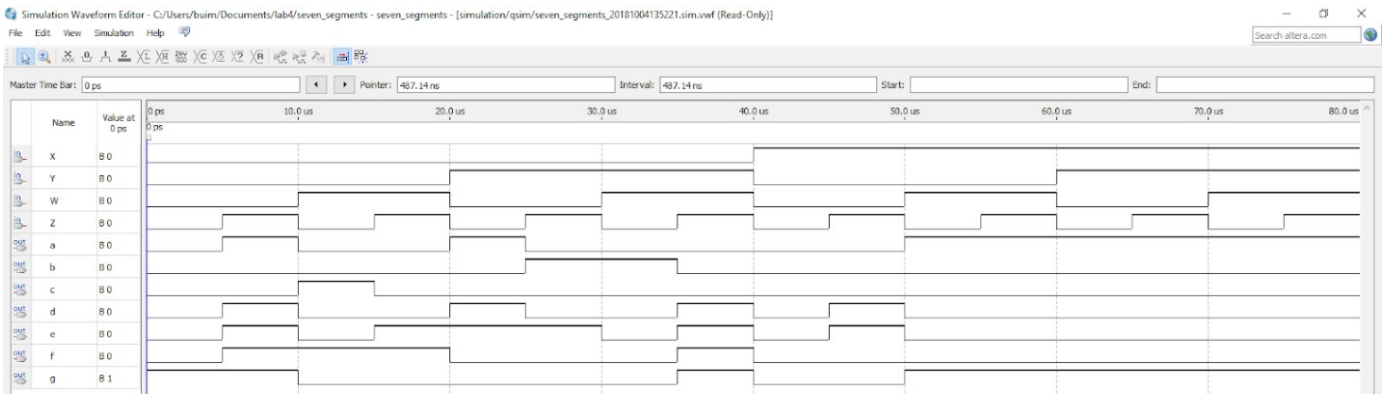


g= BCD+ AC+ AB+ A'B'C'

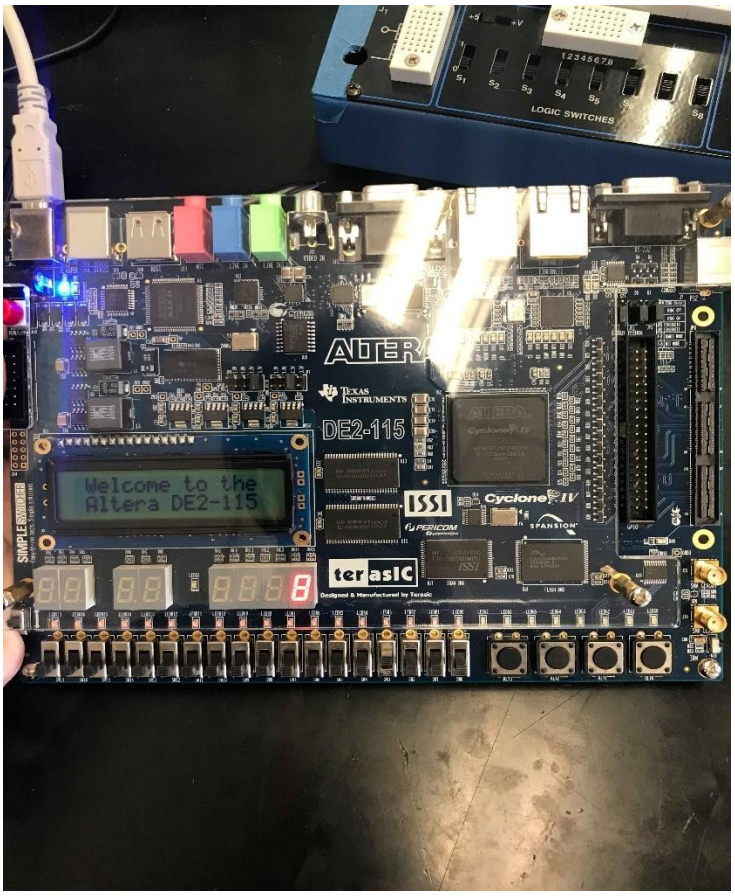
Circuit of Seven-segments



Simulation result



Pin Planner


LOGIC SWITCHES
Welcome to the
Altera DE2-115
DE2-115
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Cyclone IV