EE/CSC 327, Laboratory Assignment 2

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Course name: CSC 327

Due date: February 12, 2022

Experiment Description

Given the following truth table,

a	b	c	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

a) Find the **Minterm** expansion of the truth table and design the corresponding circuit in Quartus II. Simulate your design and verify that it functions properly according to the truth table.

b) Once you are satisfied with your design, download your design in the DE2-115 board and verify that your circuit functions according to the truth table.
For inputs use ***SW2, SW1*** and ***SW0*** as ***a, b,*** and ***c*** respectively. For output ***F***, use **LEDG1**
(** use DE2-115 user manual to do the necessary pin assignment for this design)

c) Find the **Maxterm** expansion of the truth table and design the corresponding circuit in Quartus II. Simulate your design and verify that it functions properly according to the truth table.

d) Once you are satisfied with your design, download your design in the DE2-115 board and verify that your circuit functions according to the truth table.
For inputs use ***SW5, SW4*** and ***SW3*** as ***a, b,*** and ***c*** respectively. For output ***F***, use **LEDG2**
(** use DE2-115 user manual to do the necessary pin assignment for this design)

e) Show that the circuit designed in part (a) can be simplified to a circuit consisting of three NOT gates, two 2-input AND gate and one 2-input OR gate. Draw and simulate your circuit in Quartus II and show that it functions properly according to the truth table.

f) Once you are satisfied your design, download the circuit on the DE2-115 board and verify that your circuit works properly. For inputs use ***SW2, SW1*** and ***SW0*** as ***a, b,*** and ***c*** respectively. For output ***F***, use **LEDG1**

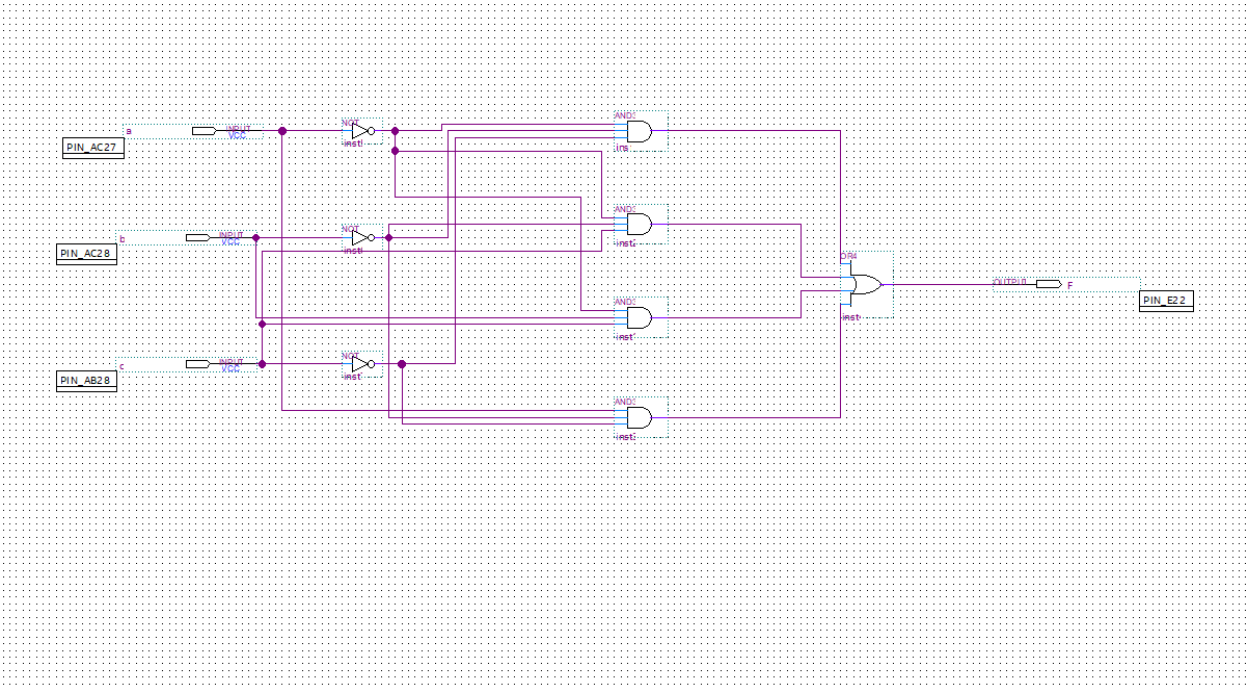
Experimental Results

Table:

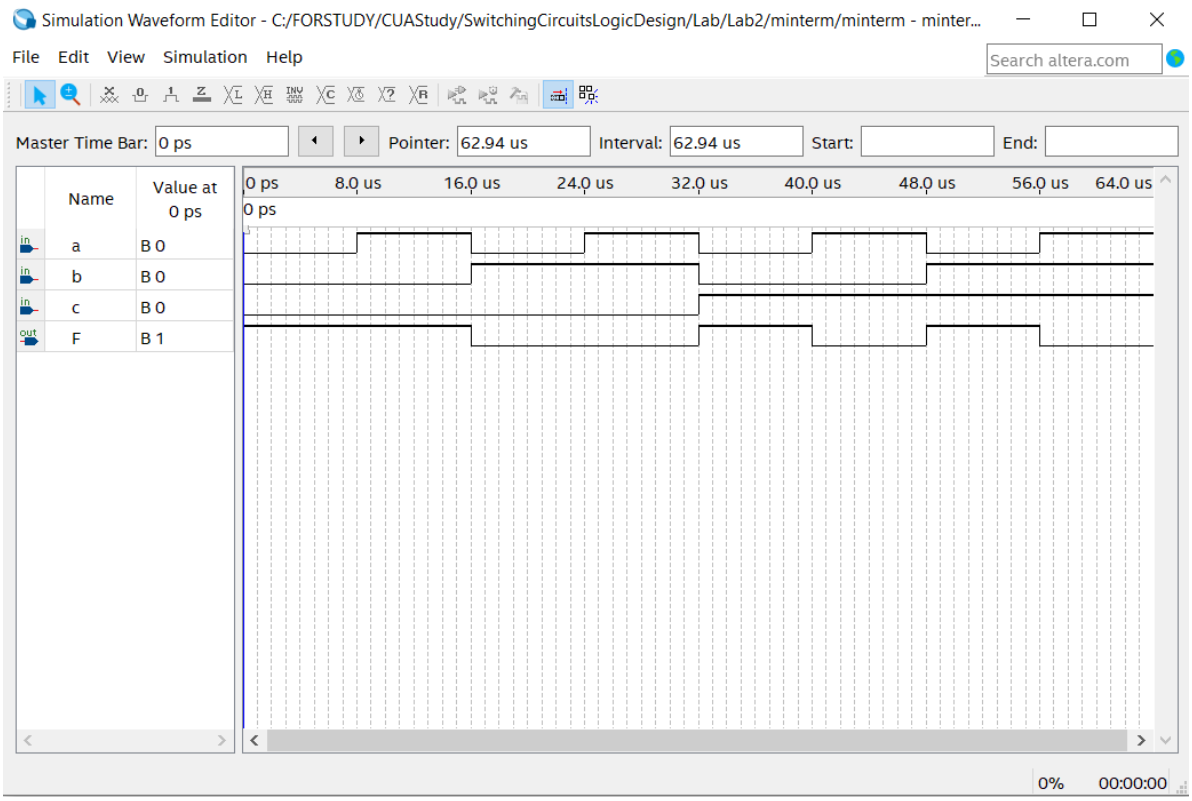
a	b	c	Minterm	Maxterm	F
0	0	0	a’b’c’	a+b+c	1
0	0	1	a’b’c	a+b+c’	1
0	1	0	a’bc’	a+b’+c	0
0	1	1	a’bc	a+b’+c’	1
1	0	0	ab’c’	a’+b+c	1
1	0	1	ab’c	a’+b+c’	0
1	1	0	abc’	a’+b’+c	0
1	1	1	abc	a’+b’+c’	0

a) Minterm expansion: a’b’c’ + a’b’c + a’bc + ab’c’

Circuit Design



Simulation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c B 0
F B 1
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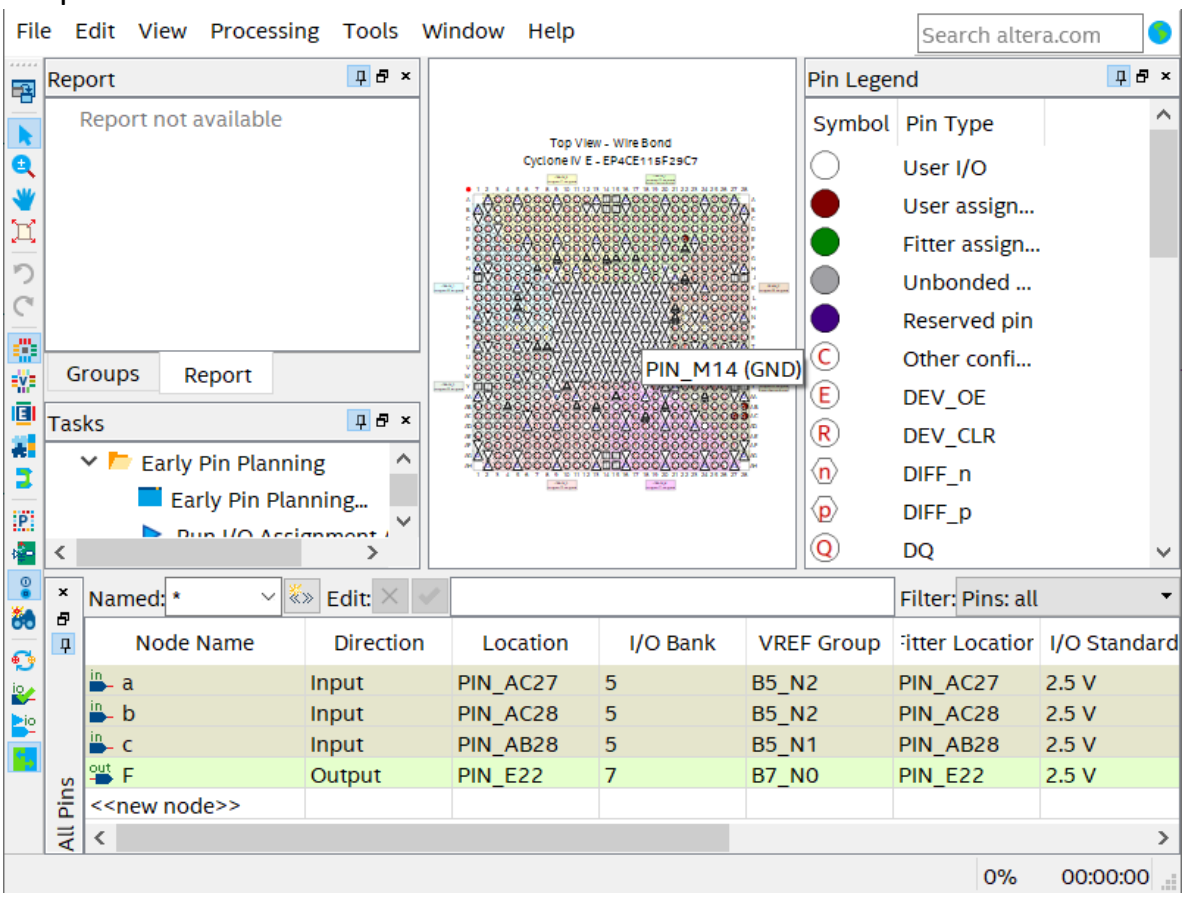
Pin planner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Tasks
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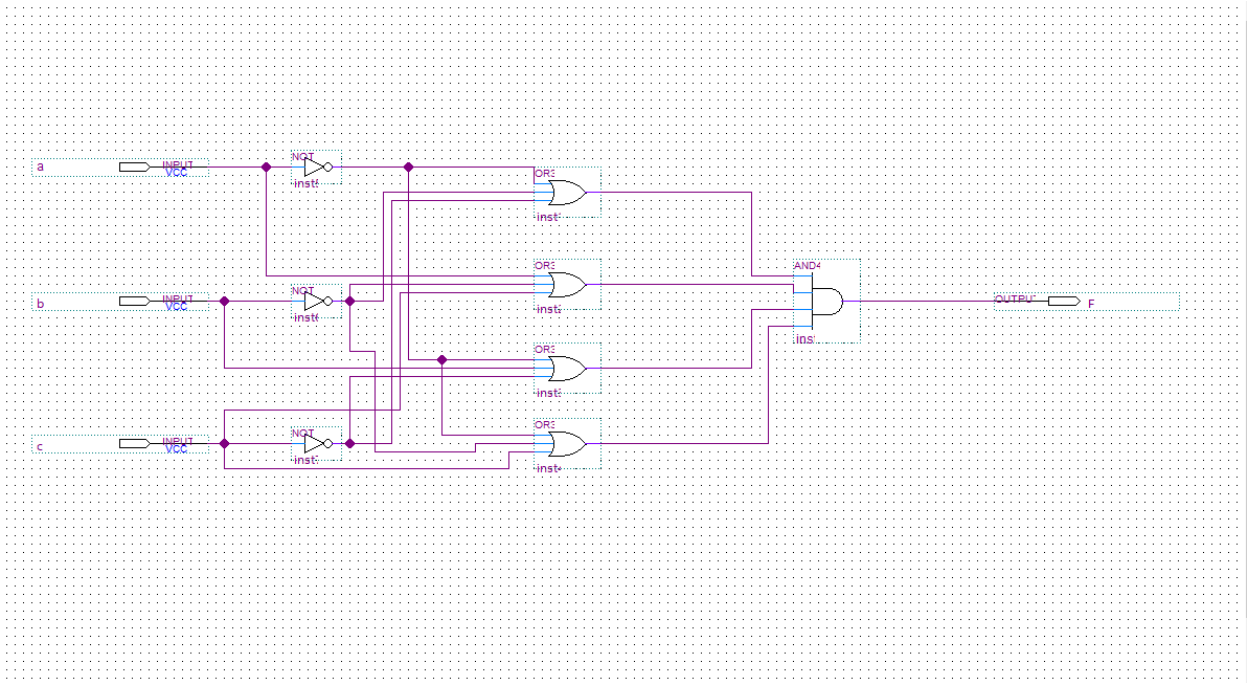
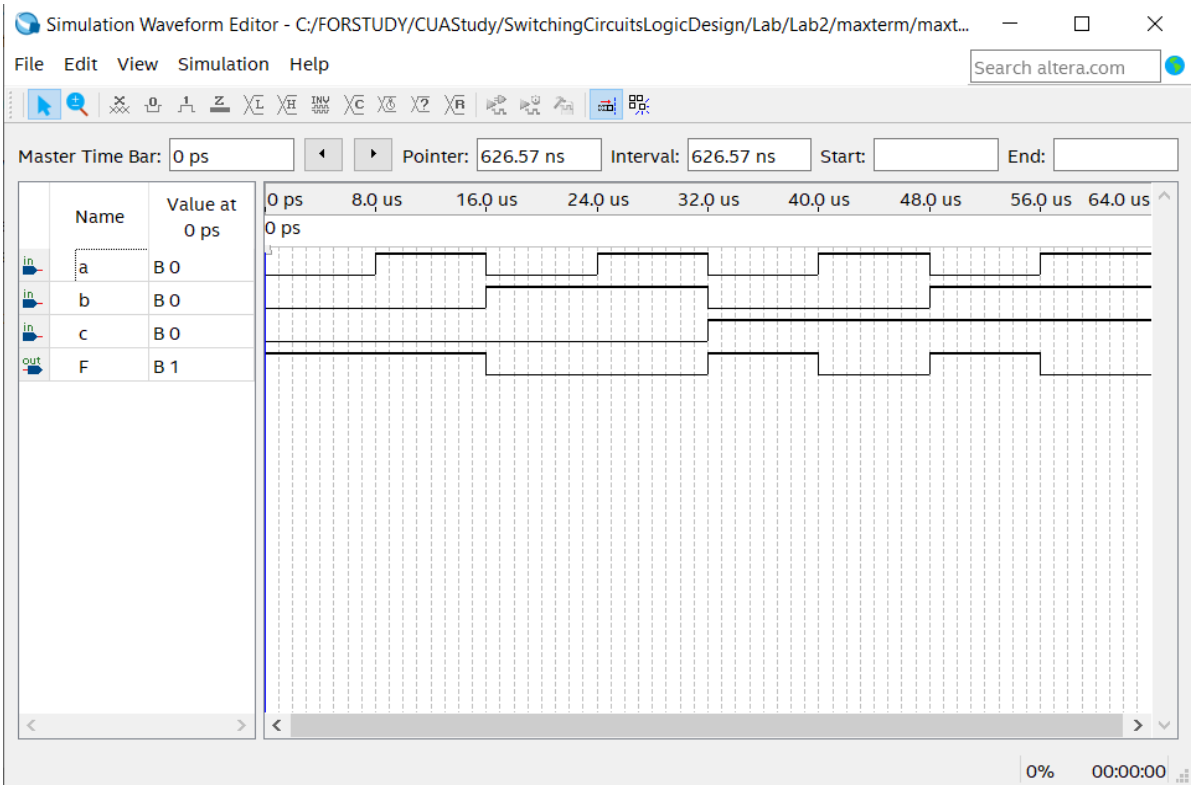
Top View - Wire Bond
Cyclone IV E - EP4CE115F29C7
PIN_M14 (GND)
Pin Legend
Symbol
Pin Type
User I/O
User assign...
Fitter assign...
Unbonded ...
Reserved pin
Other confi...
DEV_OE
DEV_CLR
DIFF_n
DIFF_p
DQ
Named: *
Edit:
Filter: Pins: all
Node Name
Direction
Location
I/O Bank
VREF Group
Fitter Location
I/O Standard
a Input PIN_AC27 5 B5_N2 PIN_AC27 2.5 V
b Input PIN_AC28 5 B5_N2 PIN_AC28 2.5 V
c Input PIN_AB28 5 B5_N1 PIN_AB28 2.5 V
F Output PIN_E22 7 B7_N0 PIN_E22 2.5 V
<<new node>>
All Pins
0%
00:00:00

c) Maxterm expansion: (a+b’+c)(a’+b+c’)(a’+b’+c)(a’+b’+c’)

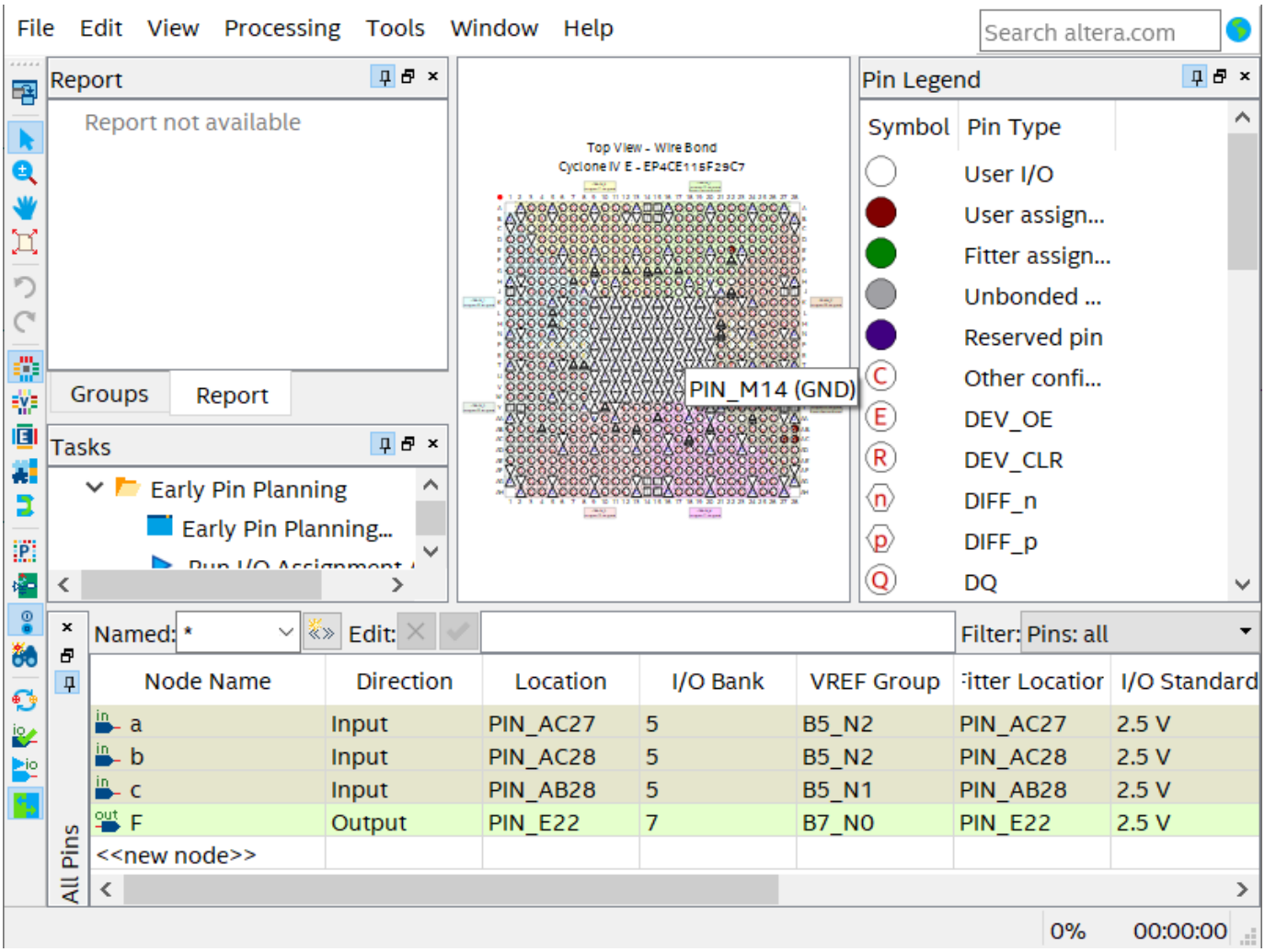
Circuit Design



Simulation



Pin planner

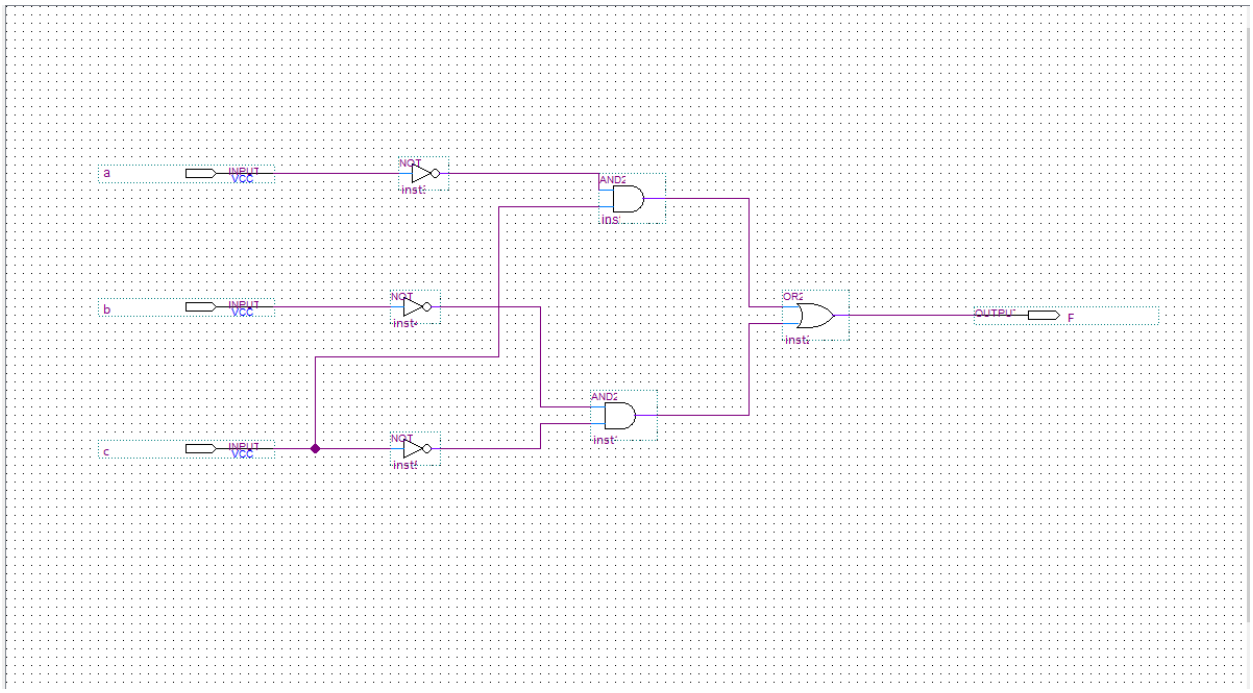


e) We have a’b’c’ + a’b’c + a’bc + ab’c’

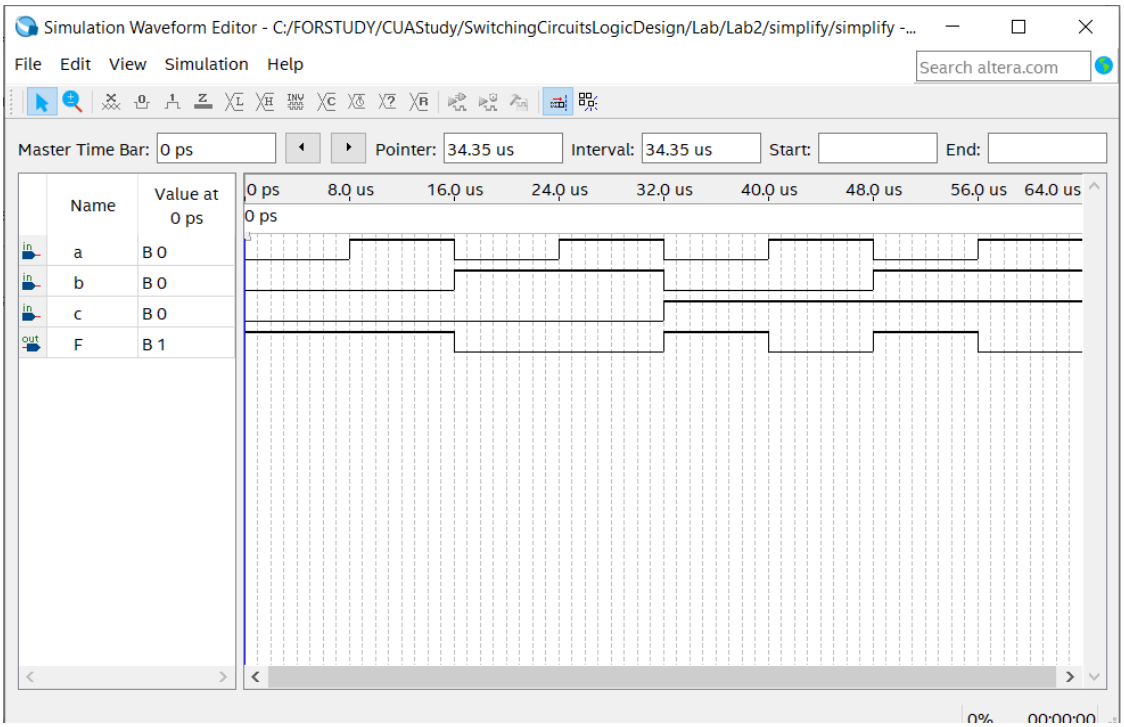
⇔ b’c’(a+a’) + a’c(b’+b)

⇔ **a’c + b’c’**

Circuit Design


a
INPUT
VCC
NOT
inst
AND2
inst
b
INPUT
VCC
NOT
inst
OR2
inst
OUTPUT
F
AND2
inst
c
INPUT
VCC
NOT
inst

Simulation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c B 0
F B 1
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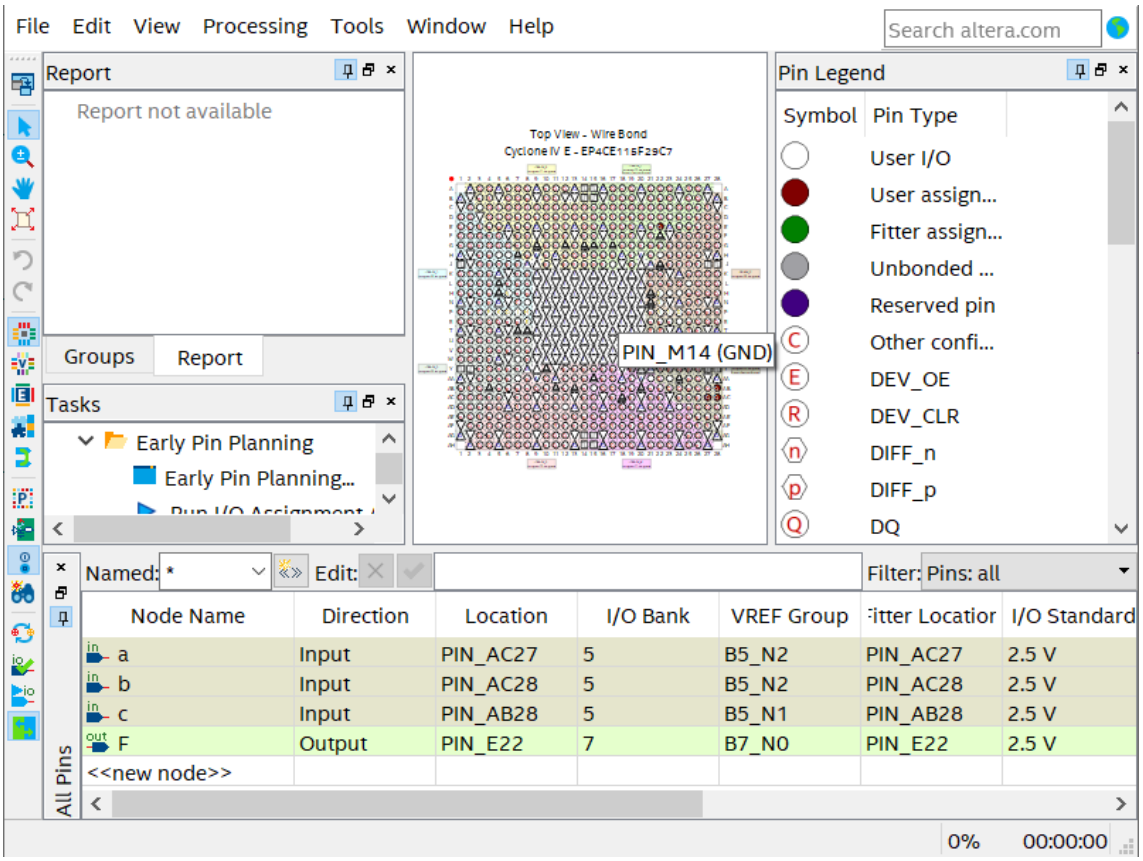

Conclusion

I learned how to find minterm and maxterm based on truth table. In addition, I learned how to simplify minterm and draw circuits base on minterm and maxterm of truth table.