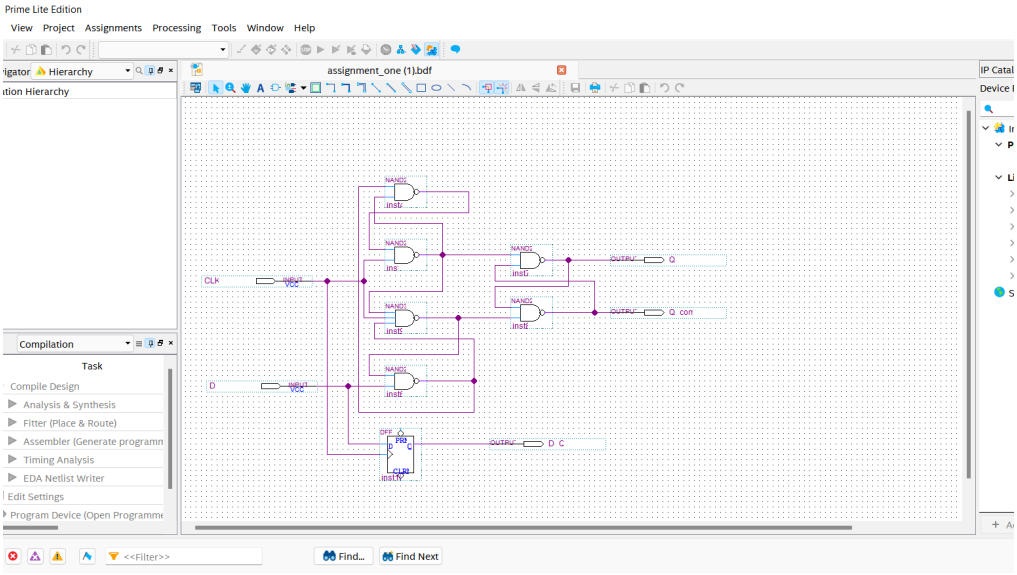
Lab 07

Shyang Kao

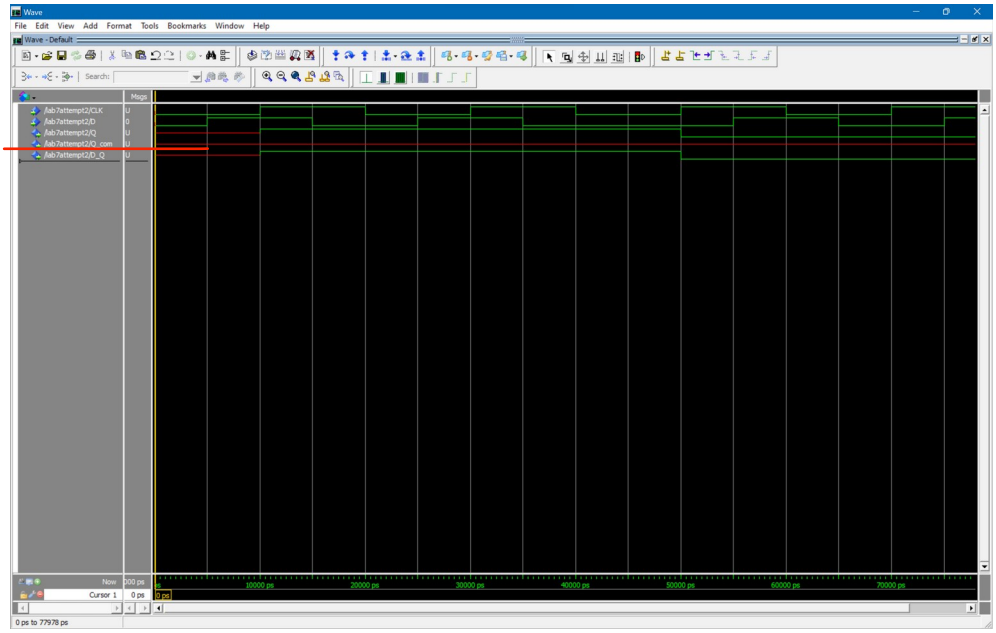
Purpose

This lab builds on the previous one by introducing the VDHL programming language and how to use it to model circuits. This demonstrates a different method of designing a circuit and a different way of utilizing ModelSim software. The student was given the responsibility of designing a circuit, translating it into VDHL code, and modeling it in ModelSim.

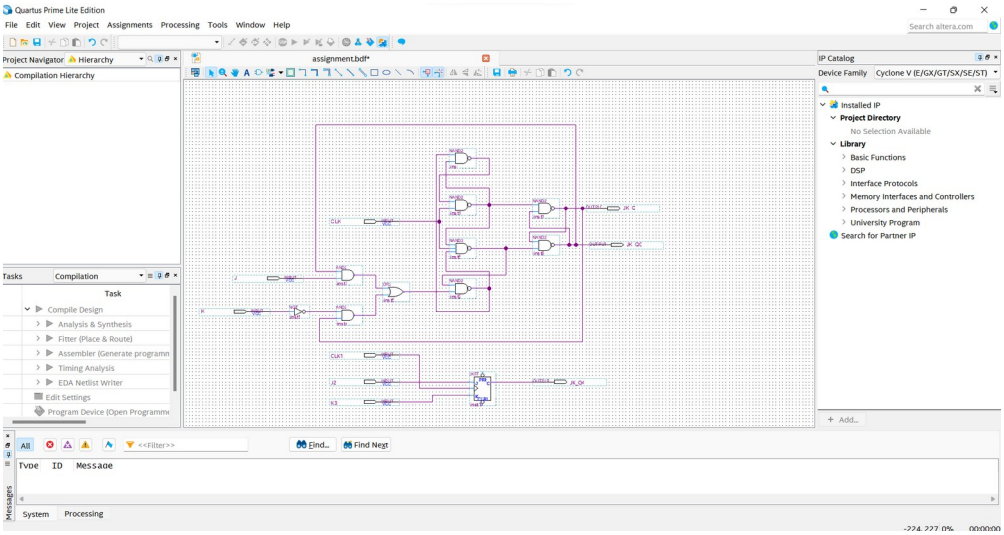
Part 1 Circuit



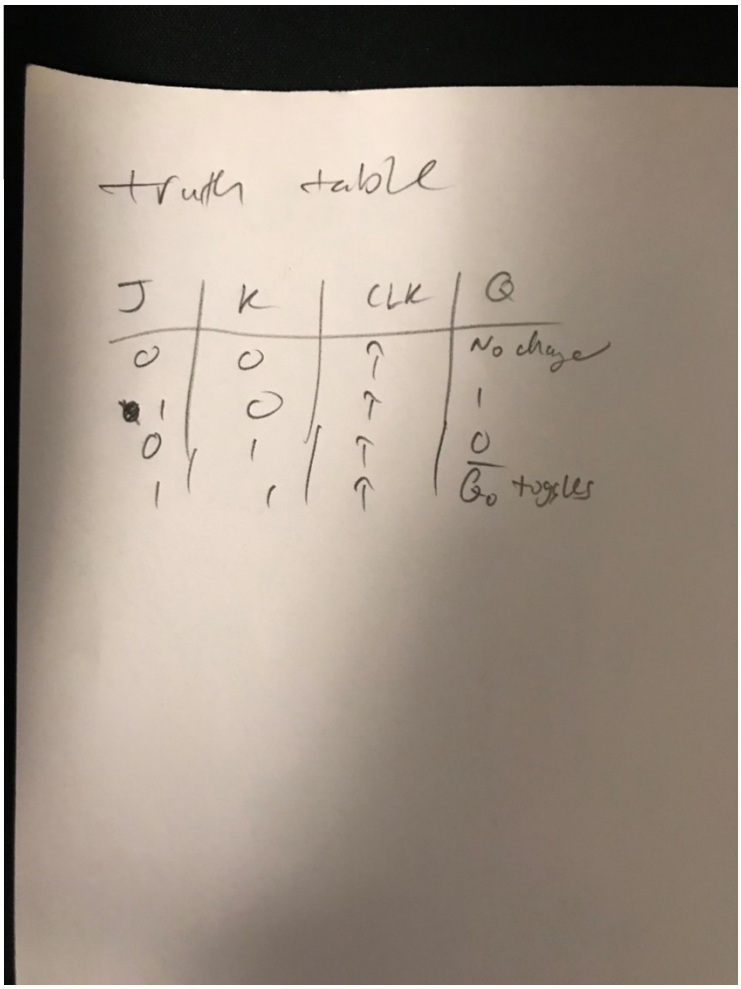
Part 1 Simulation



Part 2 Circuit:



Part 2 Truth Table:



Part 2 Simulation: