Lab 1 Submission

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1 Introduction

The goal of this lab was to design and program a logic circuit that only outputs a 1 for a given few inputs. This lab was a success and I was able to complete all of the tasks.

2 Video of Working Project

Linked here is a video of the working project: Project Video

3 Simulation

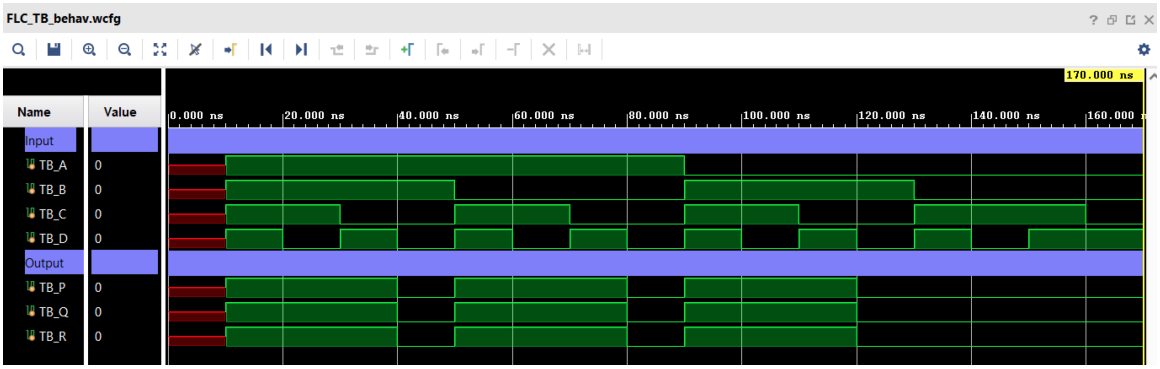

Figure 1: Vivado Simulation

4 Elaborated Design

Presented below is the elaborated design of the project generated by Vivado.

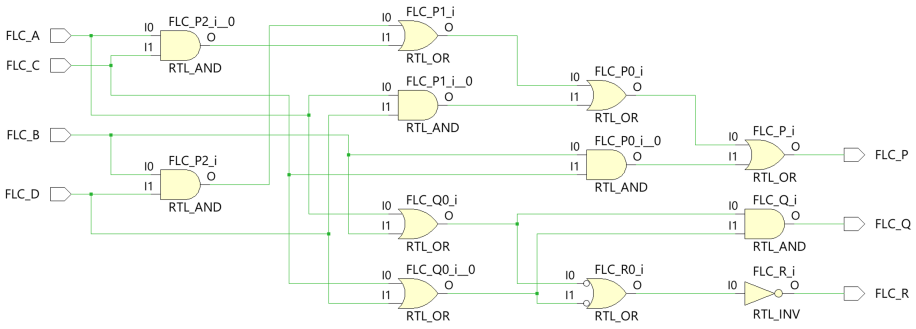

Figure 2: Elaborated Design

5 Error Log

There were no errors or significant warnings in the Vivado log as shown below.

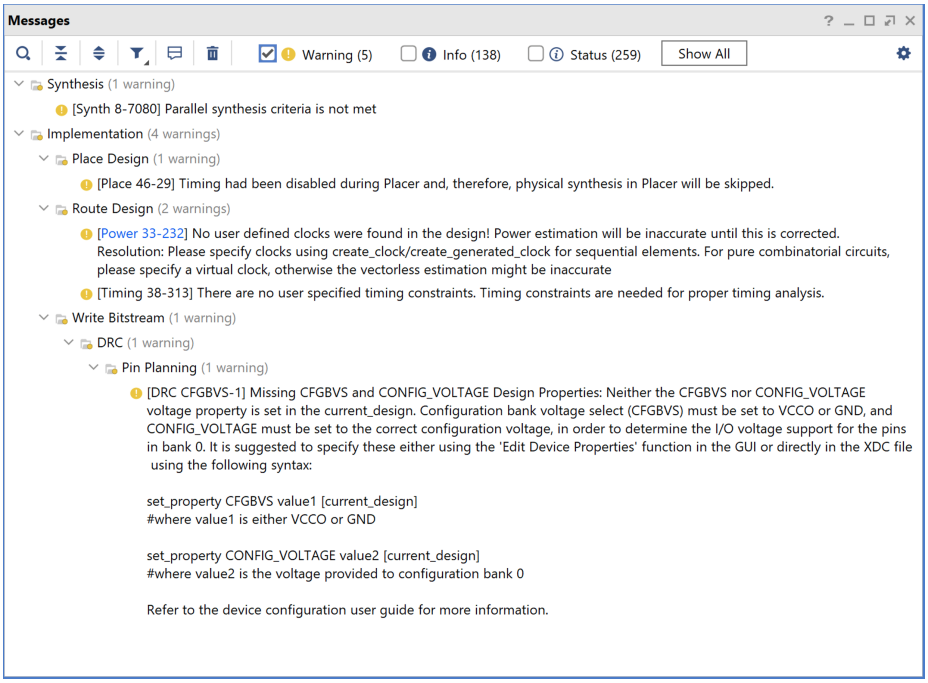

Figure 3: Error and Warning Log