

# Lab 1 Submission

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CPE 133  
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# **1 Introduction**

The goal of this lab was to design and program a logic circuit that only outputs a 1 for a given few inputs. This lab was a success and I was able to complete all of the tasks.

# **2 Video of Working Project**

Linked here is a video of the working project: [Project Video](#)

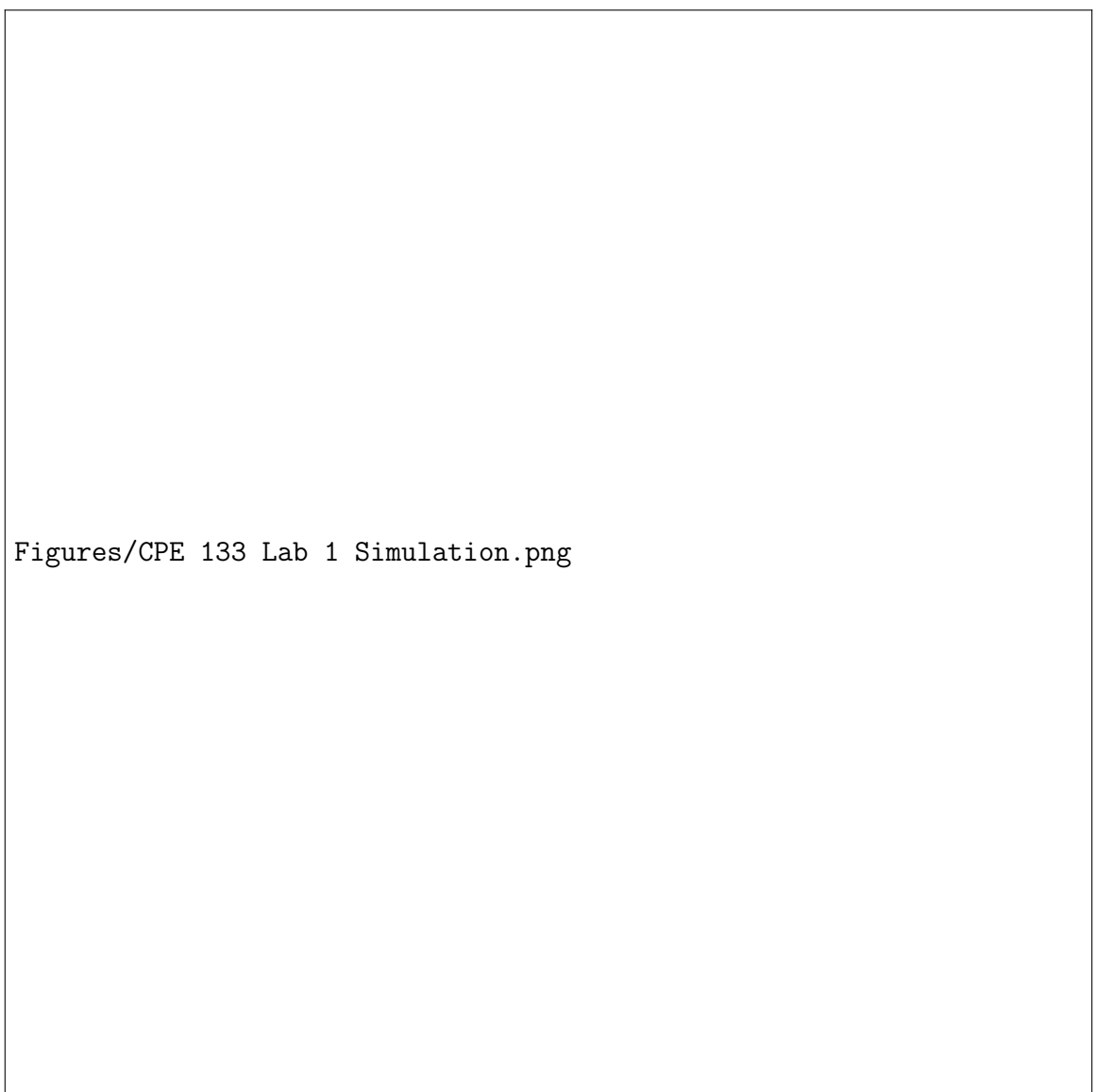
# **3 Simulation**

# **4 Elaborated Design**

Presented below is the elaborated design of the project generated by Vivado.

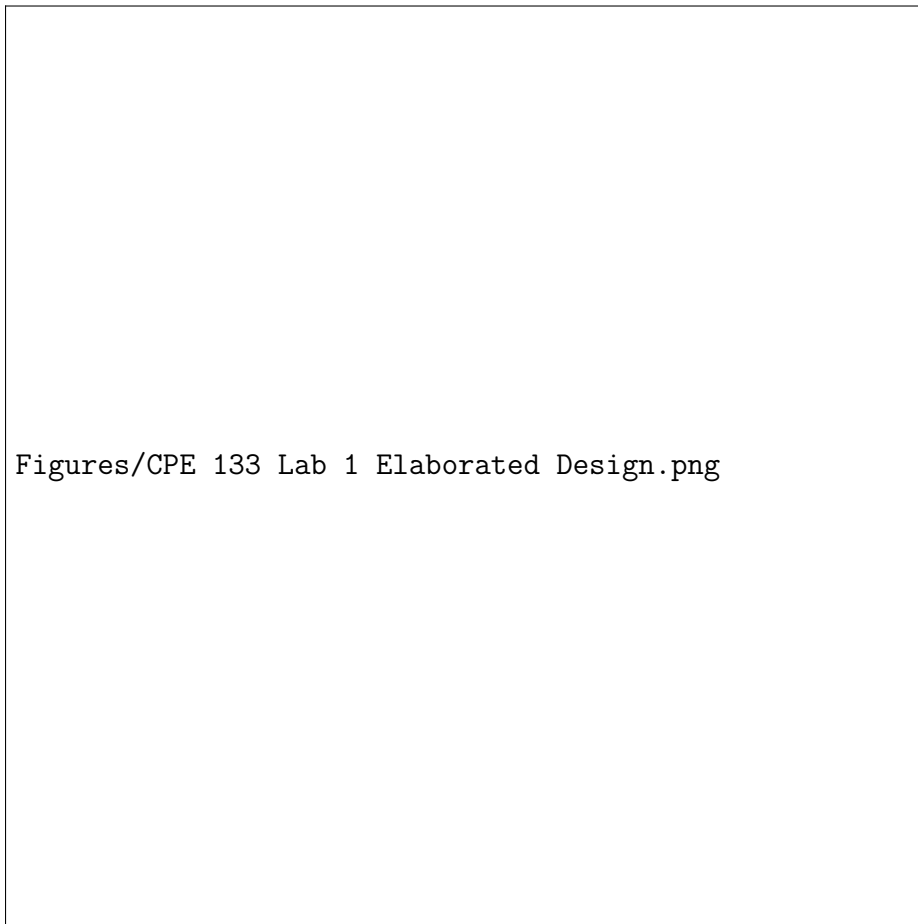
## 5 Error Log

There were no errors or significant warnings in the Vivado log as shown below.

A large rectangular area representing a Vivado simulation. It is mostly empty, with the text 'Figures/CPE 133 Lab 1 Simulation.png' located on the left side.

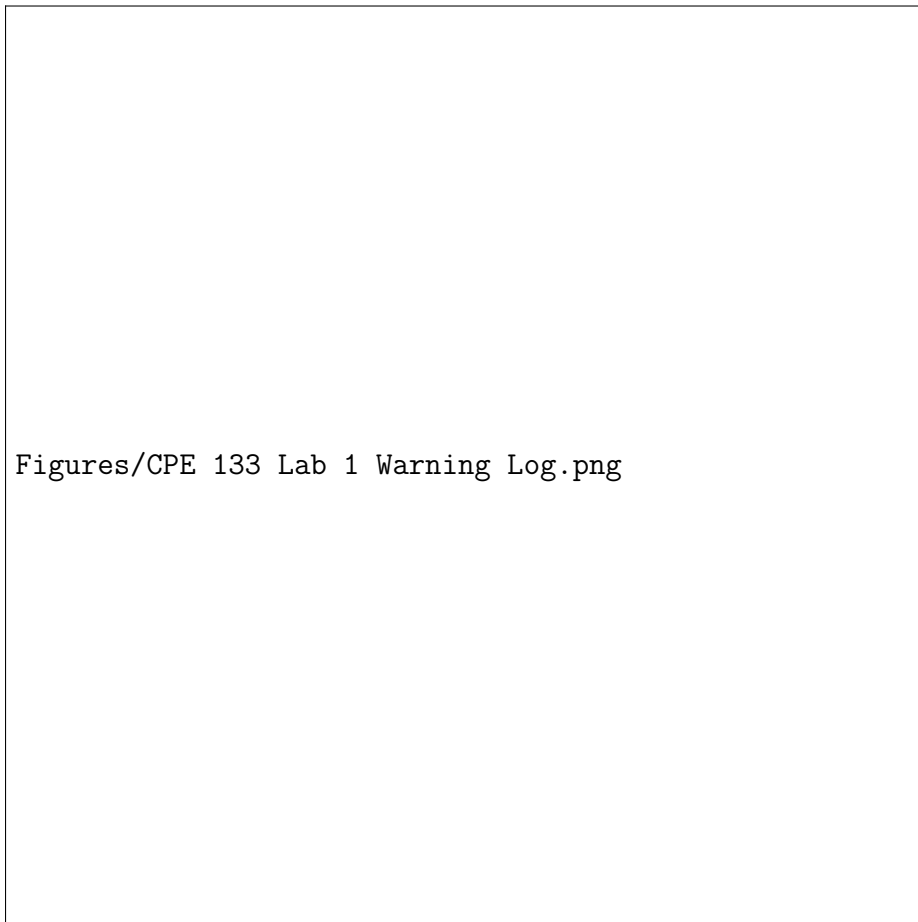
Figures/CPE 133 Lab 1 Simulation.png

Figure 1: Vivado Simulation



Figures/CPE 133 Lab 1 Elaborated Design.png

Figure 2: Elaborated Design



Figures/CPE 133 Lab 1 Warning Log.png

Figure 3: Error and Warning Log