



CAL POLY

CPE 233 Software Assignment 3

Decision Trees in Assembly

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1 Flow Charts

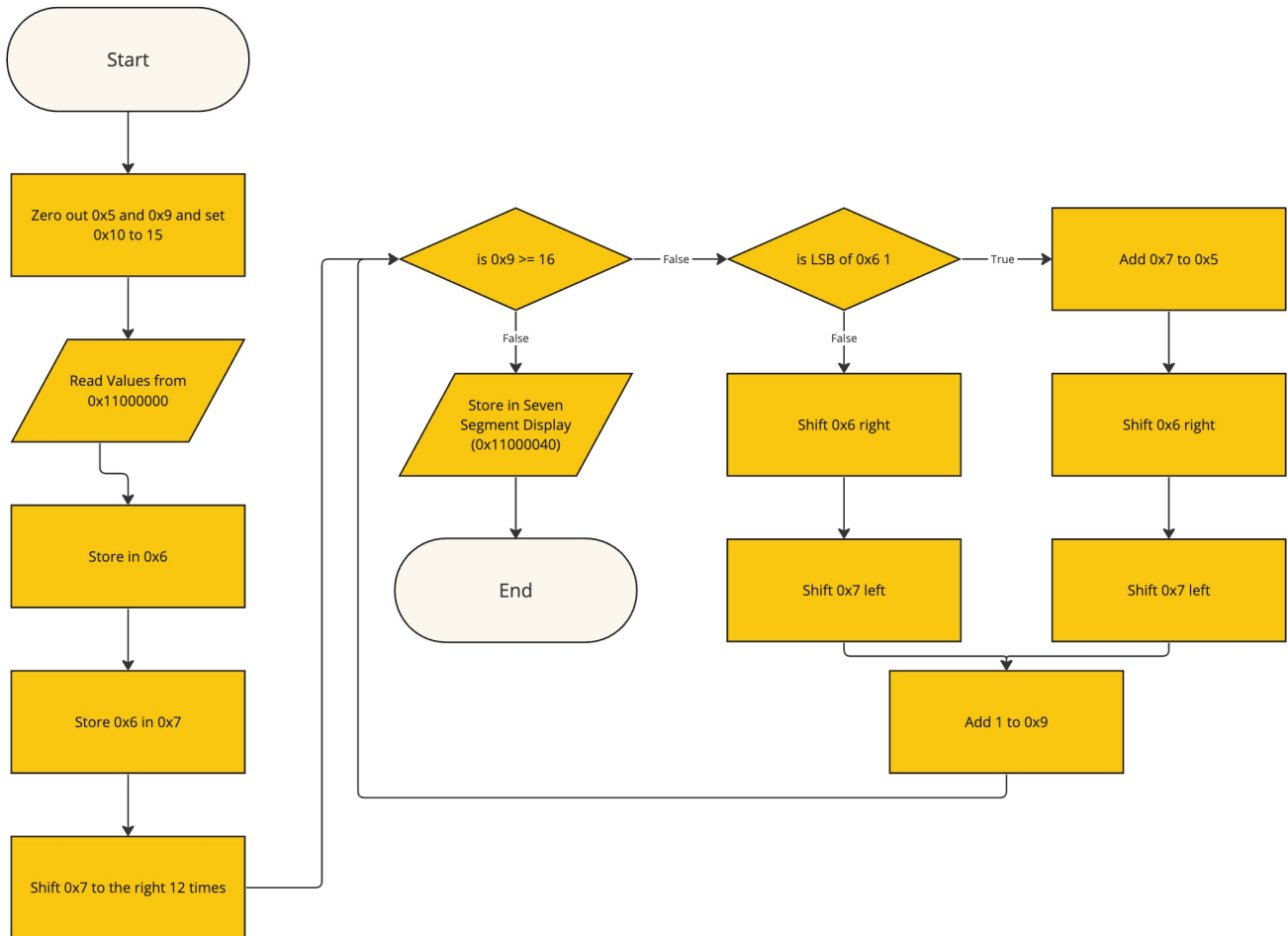


Figure 1: Multiplication Flowchart

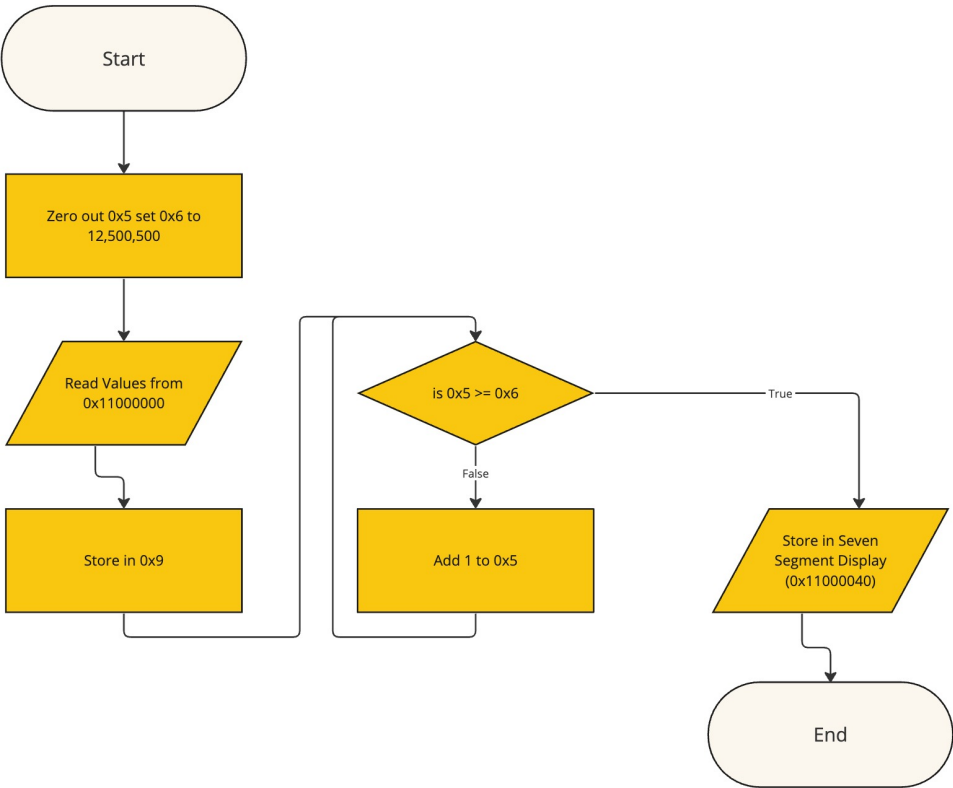


Figure 2: Instruction Delay Flowchart

2 Assembly Instructions

Below is the assembly instructions for each flow chart.

```
1      # Setup registers
2      lui    x5, 0x000000      # Output value from multiplication
3      lui    x11, 0x11000      # Define Address for switch input
4      lui    x9, 0x000000      # Current place counter
5      addi    x10, x0, 0x00000010 # Number of places to multiply
6
7      # Recive user input and format
8      lw     x6, 0(x11)        # Load switch values to x6
9      add    x7, x0, x6        # Load switch values to x7
10     srli   x7, x7, 16        # Isolate second number
11
12 multiplyStep:
13     # Begin multiplication
14     bge     x9, x10, end      # If x9 >= x10 then end
15     andi    x13, x6, 1       # Check is LSB is 1
16     beqz    x13, isZero      # Branch if LSB is 0
17
18     # Add shifted value to running total and then shift
19     # registers and increment index
20     add     x5, x5, x7
21     srli    x6, x6, 1
22     slli    x7, x7, 1
23     addi    x9, x9, 1
24     j       multiplyStep
25
26 isZero:
27     # Shift registers and increment index
28     srli    x6, x6, 1
29     slli    x7, x7, 1
30     addi    x9, x9, 1
31     j       multiplyStep
32
33
34 end:
35     sw      x5, 0x40(x11)     # Store final value
```

Listing 1: Assembly Code for Multiplication in Figure 1

```
1  # Setup registers
2  lui    x11, 0x11000    # Define Address for switch input
3  lui    x5, 0x00000     # Output value from multiplication
4
5  li     x6, 5000        # Define delay time by cycle count
6  # Calculation of the cycle count:
7  # Each instruction takes 40ns noting that there are 4
8  # instructions in the count loop this means that one loop
9  # takes 160ns. Divideing 0.5 seconds by the 160ns results
10 # in 3,125,000 cycles.
11
12 # Recive user input and format
13 lw     x9, 0(x11)      # Load switch values to x9
14
15 countLoop:
16 # Count up untill the desired time is met and the move
17 # forward in the program
18 bge    x5, x6, end
19 addi   x5, x5, 1       # Increment loop counter
20 nop
21 j      countLoop
22
23 end:
24 sw     x9, 0x40(x11)   # Store final value
```

Listing 2: Assembly Code for Delay in Figure 2

3 RARS Verification

Table 1: Flow Chart 1 Test Cases

Test Case	Input (0x5)	Expected Output	Actual Output
Zero Check	0x0000_0000	0x0000_0000	0x0000_0000
Alternating Check	0xaaaa_aaaa	0x71c6_38e4	0x71c6_38e4
Other Alternating Check	0x5555_5555	0x1c71_8e39	0x1c71_8e39
Max Check	0xffff_ffff	0xfffe0001	0xfffe0001

The test cases above demonstrate the code performs the desired outputs.

Test case 1 shows the zero case.

Test case 2 shows a value with alternating 1 and 0 .

Test case 3 shows a value with alternating 1 and 0 opposite of case 3.

Test case 5 shows an input at the maximum of the register.

Table 2: Flow Chart 2 Test Cases

Test Case	Input	Expected Output	Actual Output
Zero Check	0x0000_0000	0x0000_0000	0x0000_0000
Alternating Check	0xaaaa_aaaa	0xaaaa_aaaa	0xaaaa_aaaa
Other Alternating Check	0x5555_5555	0x5555_5555	0x5555_5555
Overflow Check	0xffff_ffff	0xffff_ffff	0xffff_ffff

The test cases above demonstrate the code performs the desired outputs.

Test case 1 shows the zero case.

Test case 2 shows a value with alternating 1 and 0 .

Test case 3 shows a value with alternating 1 and 0 opposite of case 3.

Test case 5 shows an input at the maximum of the register.