

Declarations

Ports:

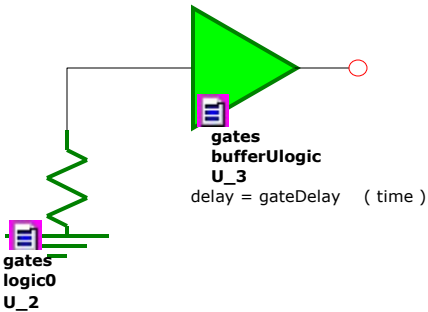
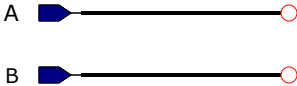
A : std_ulogic_vector(17 DOWNT0 0)
B : std_ulogic_vector(17 downto 0)
resultat : std_ulogic

Diagram Signals:

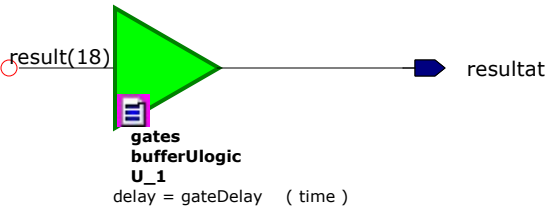
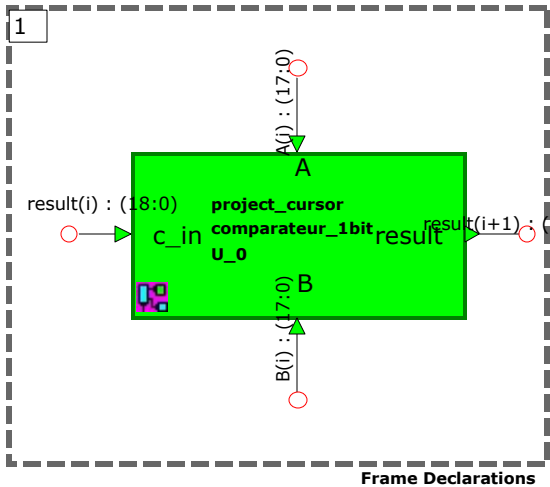
SIGNAL logic_0 : std_uLogic
SIGNAL result : std_ulogic_vector(18 DOWNT0 0)

Package List

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;
LIBRARY gates;
USE gates.gates.all;



g0: FOR i IN 0 TO 17 GENERATE



<company name>		Project:	hds
Title:		<enter comments here>	
Path:			
Edited:			