#### project\_cursor/soustracteur\_18bits/struct

### Declarations

### Ports:

A : std\_ulogic\_vector(17 DOWNTO 0)
B : std\_ulogic\_vector(17 DOWNTO 0)
resultat : std\_ulogic\_vector(17 DOWNTO 0)

# **Diagram Signals:**

SIGNAL carry : std\_ulogic\_vector(18 downto 0)

- resultat



USE gates.gates.all;

LIBRARY gates;

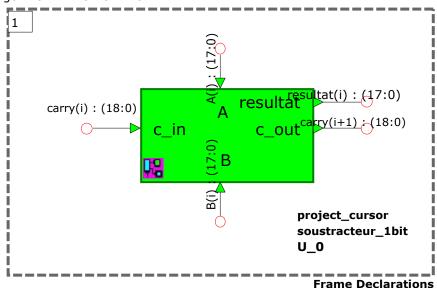
Package List

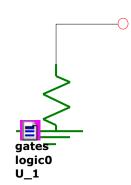
LIBRARY ieee;

USE ieee.std\_logic\_1164.all; USE ieee.numeric\_std.all;



# q0: FOR i IN 0 TO 17 GENERATE





<company name=""></company>		Project:	hds
		<enter comments="" here=""></enter>	
Title:	<enter diagram="" here="" title=""></enter>		
Path:	project_cursor/soustracteur_18bits/struct		
Edited:	by Etienne on 02 déc. 2023		