Package List
LIBRARY ieee;
  USE ieee.std_logic_1164.all;
  USE ieee.numeric_std.all;
LIBRARY gates;
USE gates.gates.ALL;

Declarations
Ports:
    A   : std_ulogic_vector(7 DOWNTO 0)
    B   : std_ulogic_vector(7 downto 0)
    resultat : std_ulogic
Diagram Signals:
    SIGNAL Egal   : std_uLogic
    SIGNAL Zero   : std_uLogic
    SIGNAL logic_0 : std_uLogic
    SIGNAL out4   : std_uLogic
    SIGNAL result   : std_ulogic_vector(8 DOWNTO 0)

A

B

result(i+1)

result(8)

gates
or2
U_1
delay = gateDelay   (time)

gates
and2inv1
U_17
delay = gateDelay   (time)

resultat

g1: FOR i IN 0 TO 7 GENERATE

2

A(i) : (7:0)

result(i) : (8:0)

c_in

project_cursor
comparateur_1bit
U_0

A

result

B

B(i) :(7:0)

gates
bufferUlogic
U_3
delay = gateDelay   (time)

gates
logic0
U_2

Frame Declarations