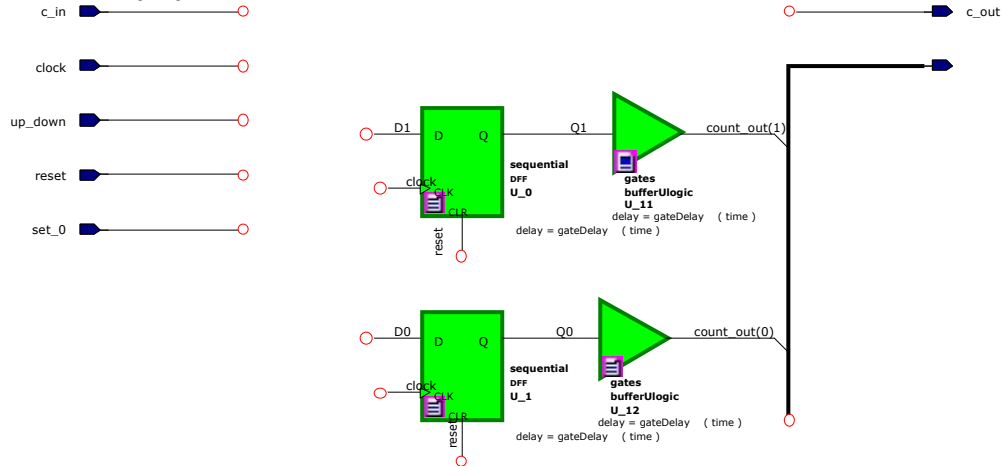


```
Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;
LIBRARY gates;
USE gates.gates.all;
```



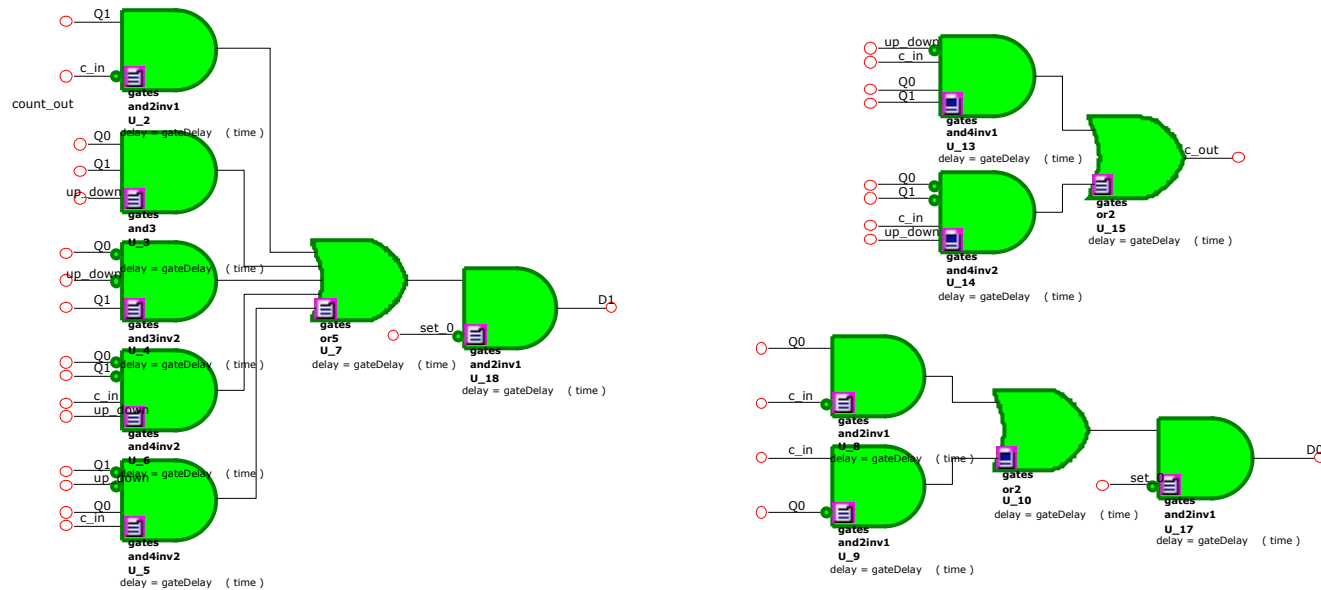
Declarations

Ports:

```
c_in      : std_logic
clock     : std_logic
reset     : std_logic
set_0     : std_logic
up_down   : std_logic
c_out     : std_logic
count_out : std_logic_vector(1 DOWNTO 0)
```

Diagram Signals:

```
SIGNAL D0      : std_logic
SIGNAL D1      : std_logic
SIGNAL Q0      : std_logic
SIGNAL Q1      : std_logic
SIGNAL in17    : std_logic
SIGNAL in18    : std_logic
SIGNAL in19    : std_logic
SIGNAL in20    : std_logic
SIGNAL in21    : std_logic
SIGNAL out1    : std_logic
SIGNAL out2    : std_logic
SIGNAL out3    : std_logic
SIGNAL out4    : std_logic
SIGNAL out5    : std_logic
SIGNAL out6    : std_logic
```



<company name>		Project:	hds
		<enter comments here>	
Title:	<enter diagram title here>		
Path:	<-- more -->		
Edited:	by Etienne on 21 janv. 2024		