Package List

```
LIBRARY ieee;
 USE ieee.std_logic_1164.all;
 USE ieee.numeric_std.all;
LIBRARY gates;
USE gates.gates.all;
```

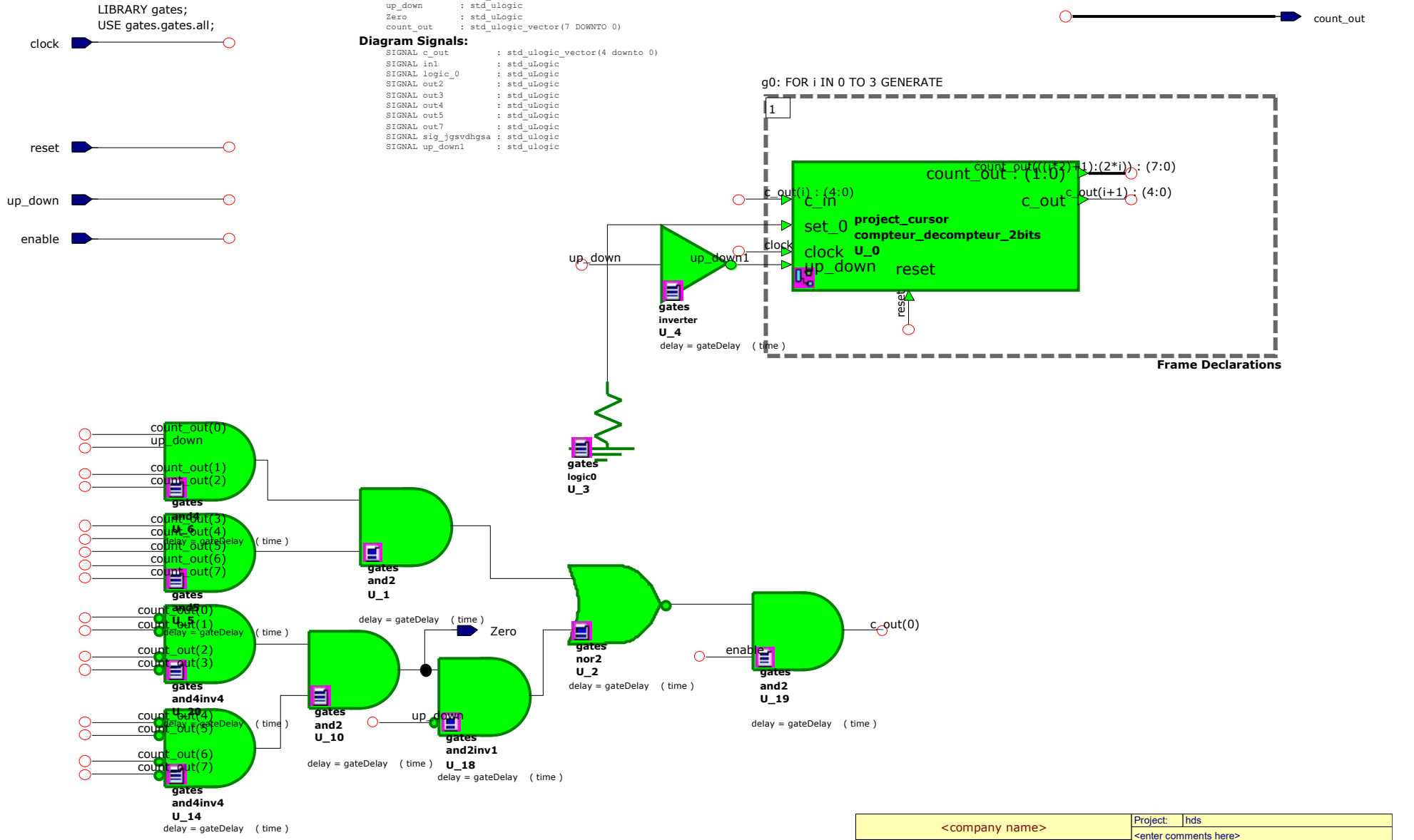
Declarations

Ports:

```
clock         : std_ulogic
enable        : std_ulogic
reset         : std_ulogic
up_down       : std_ulogic
Zero          : std_uLogic
count_out     : std_ulogic_vector(7 DOWNTO 0)
```

Diagram Signals:

```
SIGNAL c_out          : std_ulogic_vector(4 downto 0)
SIGNAL in1            : std_uLogic
SIGNAL logic_0        : std_uLogic
SIGNAL out2           : std_uLogic
SIGNAL out3           : std_uLogic
SIGNAL out4           : std_uLogic
SIGNAL out5           : std_uLogic
SIGNAL out7           : std_uLogic
SIGNAL sig_jgsvdhgsa  : std_ulogic
SIGNAL up_down1       : std_ulogic
```



<company name>		Project:	hds
Title:	<enter diagram title here>	<enter comments here>	
Path:	<<-- more -->>		
Edited:	by etienne.haingart on 08 janv. 2024		