GSI008 – Sistemas Digitais

Projeto de Circuitos Combinacionais Aritméticos

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Créditos dos slides para o Prof. Dr. Daniel D. Abdala

Na Aula Anterior ...

- DLPs – Ideia Geral
- Benefícios da Utilização de DLPs;
- Funcionamento geral de DLPs;
- Visão geral FPGAs;
- Introdução ao VHDL.

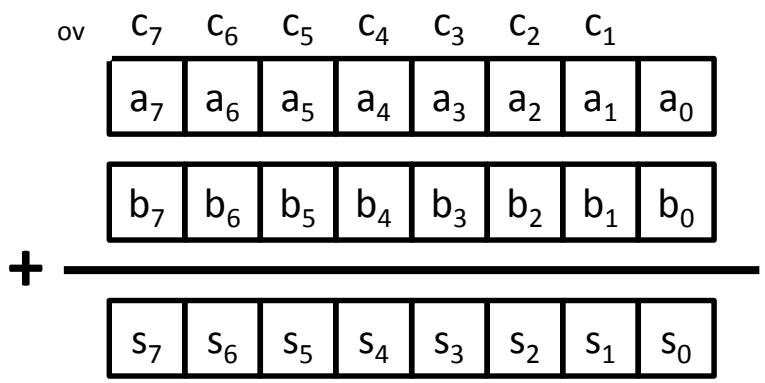
DLP	Dispositivo Lógico Programável
FPGA	Field Programmable Gate Array
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuits

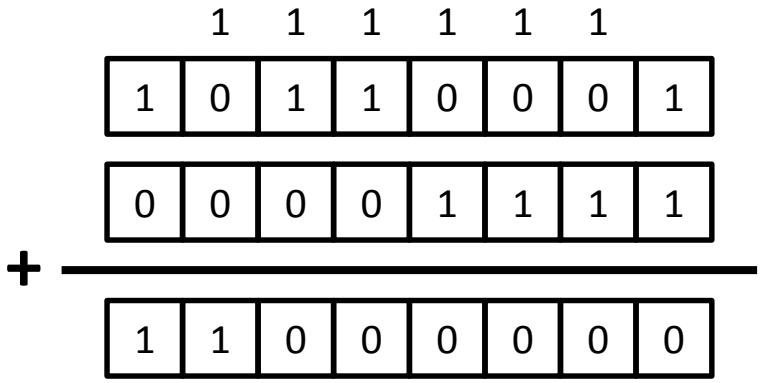
Nesta Aula

- Circuito para o Meio Somador;
- Circuito para o Somador Completo de 1 bit;
- Circuito para o Somador Completo de 8 bits;
- Circuito para o Meio Subtrator;
- Circuito para o Subtrator Completo de 1 bit;
- Circuito para o Subtrator Completo de 8 bits.

Problema

- Construir um circuito digital capaz de somar dois números de 8 bits.



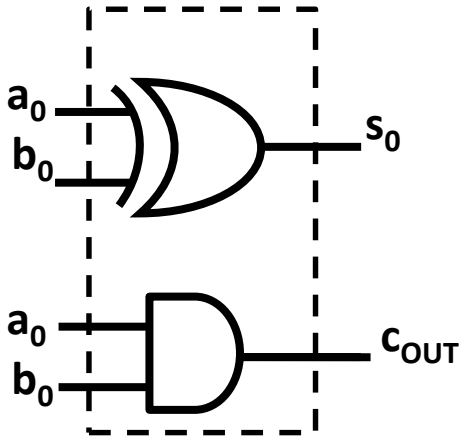


Meio Somador

a_0	b_0	s_0	c_{OUT}
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$s_0 = a_0 \oplus b_0$$

$$c_{OUT} = a_0 \cdot b_0$$



Somador Completo

- Somador para os demais bits

a_n	b_n	c_n	s_n	c_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$s_n = (\bar{a}_n \cdot \bar{b}_n \cdot c_n) + (\bar{a}_n \cdot b_n \cdot \bar{c}_n) + (a_n \cdot \bar{b}_n \cdot \bar{c}_n) + (a_n \cdot b_n \cdot c_n)$$

$$s_n = \bar{a}_n \cdot [(\bar{b}_n \cdot c_n) + (b_n \cdot \bar{c}_n)] + a_n \cdot (\bar{b}_n \cdot \bar{c}_n) + (b_n \cdot c_n)$$

$$s_n = \bar{a}_n \cdot (b_n \oplus c_n) + a_n \cdot (b_n \otimes c_n)$$

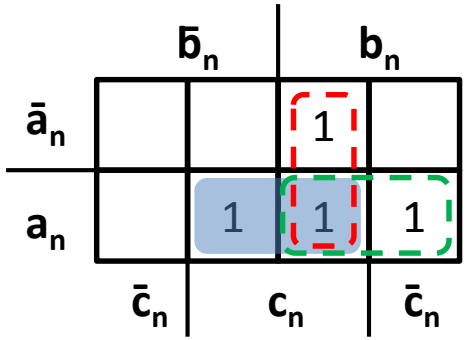
$$s_n = \bar{a}_n \cdot (b_n \oplus c_n) + a_n \cdot \overline{(b_n \oplus c_n)}$$

$$s_n = a_n \oplus b_n \oplus c_n$$

Somador Completo

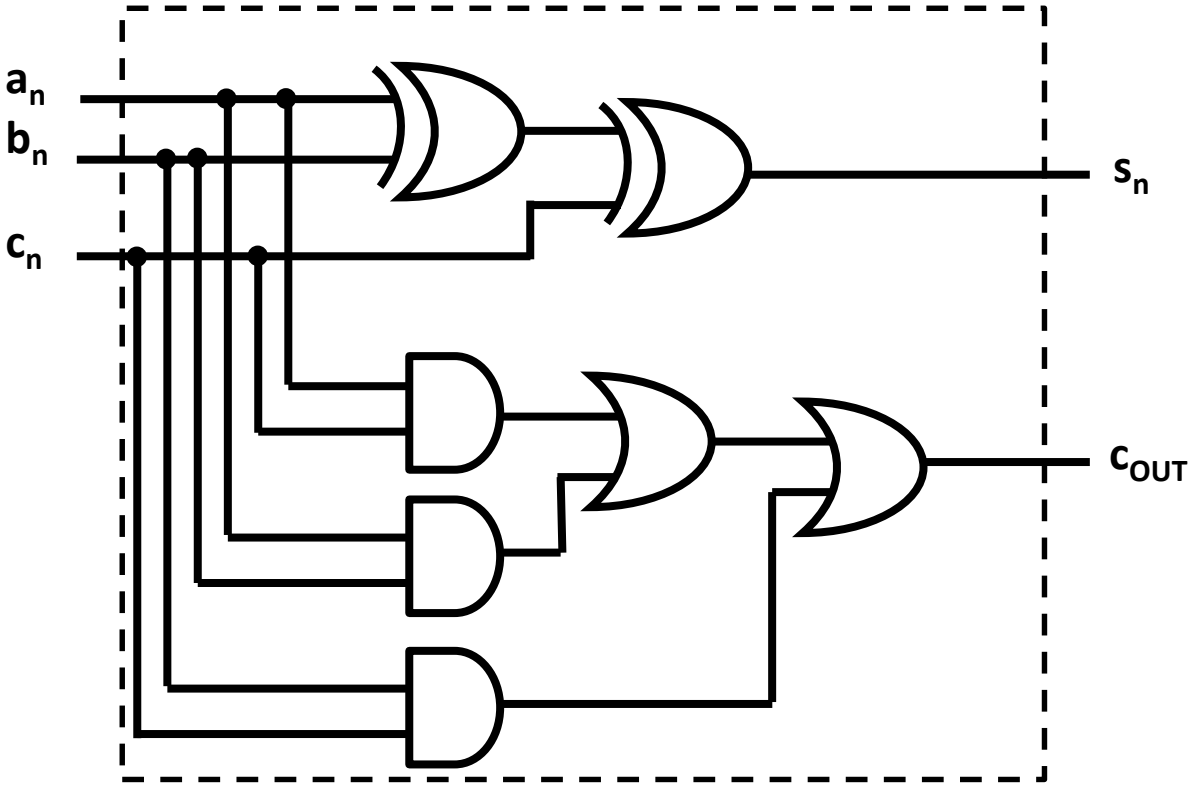
a_n	b_n	c_n	s_n	c_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$c_{out} = (\bar{a}_n \cdot b_n \cdot c_n) + (a_n \cdot \bar{b}_n \cdot c_n) + (a_n \cdot b_n \cdot \bar{c}_n) + (a_n \cdot b_n \cdot c_n)$$

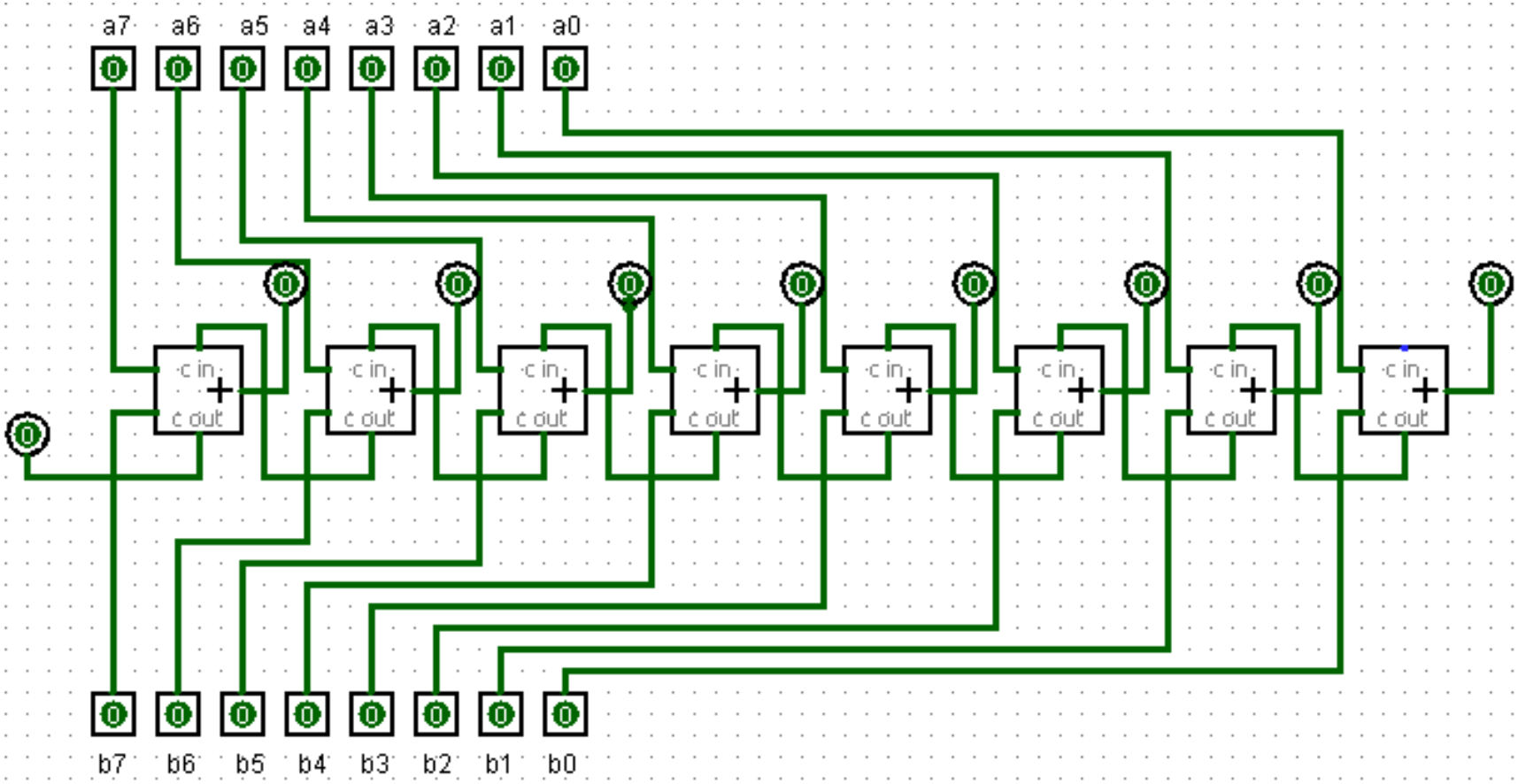


$$c_{out} = (a_n \cdot c_n) + (a_n \cdot b_n) + (b_n \cdot c_n)$$

Somador Completo



Somador de 8 bits

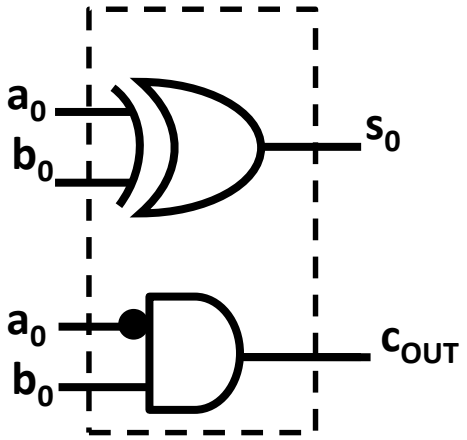


Meio Subtrator

a_0	b_0	s_0	c_{OUT}
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$s_0 = a_0 \oplus b_0$$

$$c_{OUT} = \bar{a}_0 \cdot b_0$$



Subtrator Completo

- Subtrator para os demais bits

a_n	b_n	c_n	s_n	c_{OUT}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$s_n = (\bar{a}_n \cdot \bar{b}_n \cdot c_n) + (\bar{a}_n \cdot b_n \cdot \bar{c}_n) + (a_n \cdot \bar{b}_n \cdot \bar{c}_n) + (a_n \cdot b_n \cdot c_n)$$

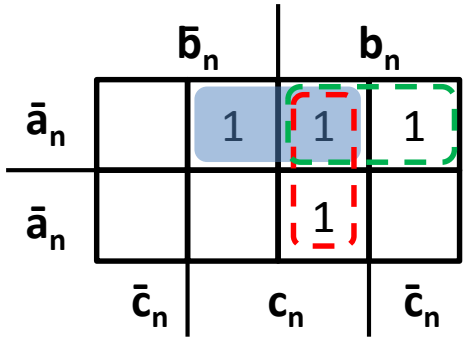
Mesmo caso do somador completo

$$s_n = a_n \oplus b_n \oplus c_n$$

Subtrator Completo

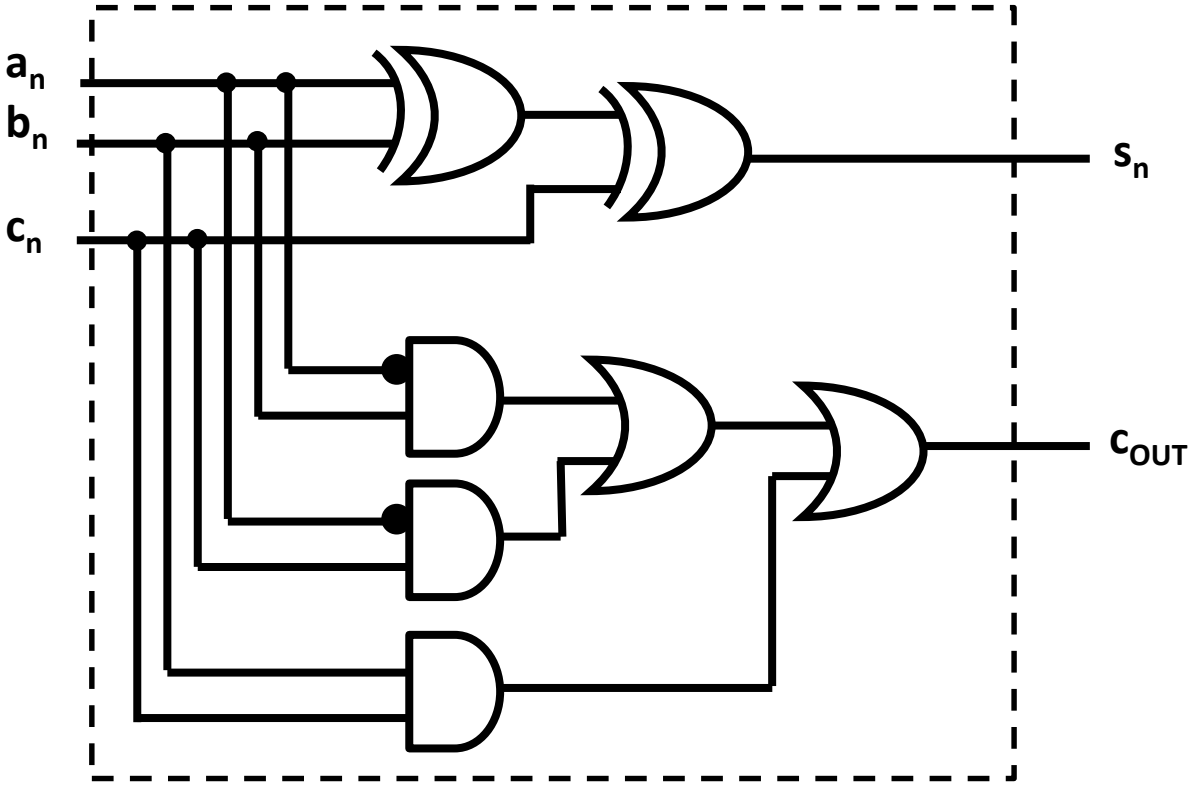
a_n	b_n	c_n	s_n	c_{OUT}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$c_{out} = (\bar{a}_n \cdot \bar{b}_n \cdot c_n) + (\bar{a}_n \cdot b_n \cdot \bar{c}_n) + (\bar{a}_n \cdot b_n \cdot c_n) + (a_n \cdot b_n \cdot c_n)$$

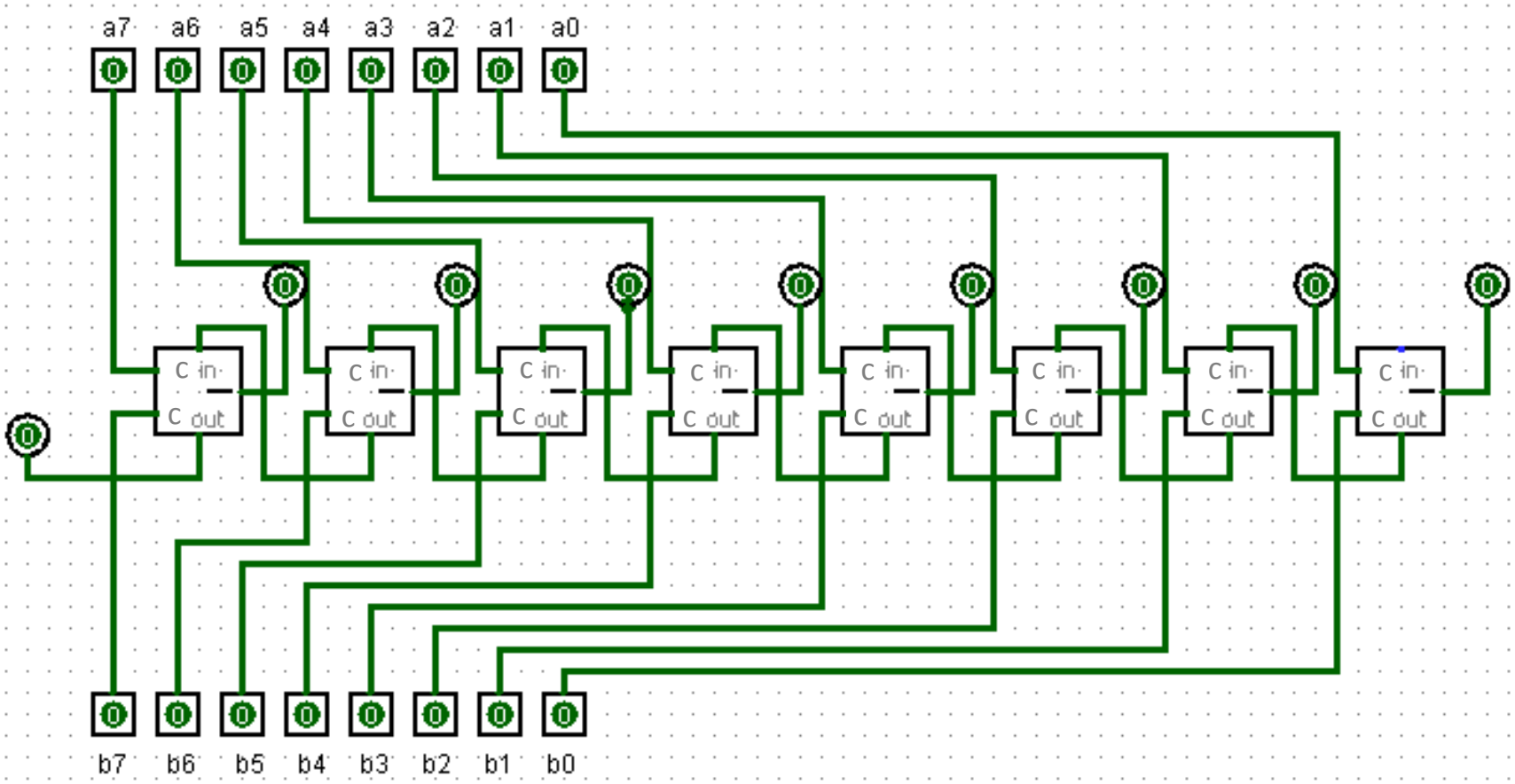


$$c_{out} = (\bar{a}_n \cdot c_n) + (\bar{a}_n \cdot b_n) + (b_n \cdot c_n)$$

Subtrator Completo



Subtrator de 8 bits



Pro Lar

- Leitura (Tocci): 6.9-6.11 (pp. 67-72)
- Leitura (Capuano): 5.3 – 5.3.9 (pp. 168-179)
- Exercícios (Tocci): E = {6.18 – 6.20}
- Exercícios (Capuano): E = {5.3.8}

Bibliografia Comentada

- TOCCI, R. J., WIDMER, N. S., MOSS, G. L. **Sistemas Digitais – Princípios e Aplicações**. 11ª Ed. Pearson Prentice Hall, São Paulo, S.P., 2011, Brasil.

- CAPUANO, F. G., IDOETA, I. V. **Elementos de Eletrônica Digital**. 40ª Ed. Editora Érica.
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