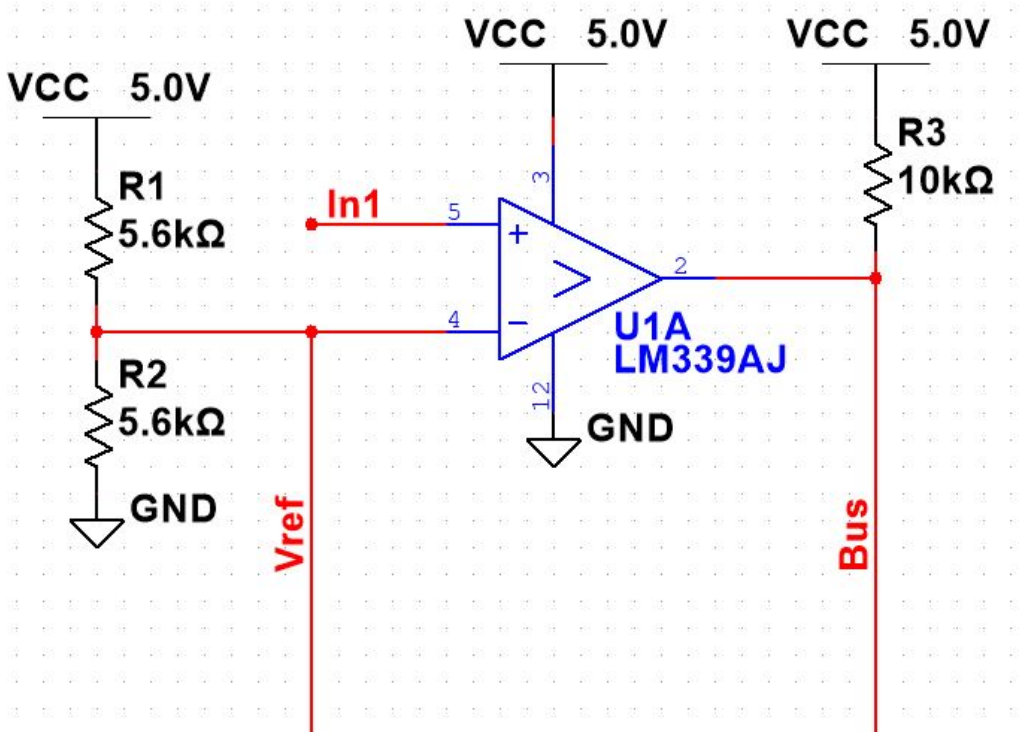
Information

Note: Projects are considered as evaluation tools. As such, you do not have the opportunity to make multiple submissions. Make sure you are ready to submit your work for grading before you do so!

Wired OR Bus

The LM339 IC is a quad open-collector comparator. We will use this IC to emulate four devices connected to a single-wire serial bus. The partially-completed diagram below shows some of the key components of the intended design. You will be required to draw a completed schematic for the project, as outlined in the following discussion.



In your final design, there will be only one IC, the three resistors shown above, a DIP switch, and four logic switch pullup resistors on your breadboard. Keep that in mind as you proceed!

- Vref is intended to be a constant 2.5 V, and will be connected to the inverting inputs of each of the four comparators in your LM339IC. (Typically, a voltage divider is not recommended for generating a reference voltage, but since in this circuit all of the inputs arehigh impedance, no current will be drawn from the voltage divider, so it will not be "loaded" by the connected circuitry.)
- Use four of the switches in an 8-position DIP switch to create four Active-Low Logic switches, of which "In1" in the starterschematic above is one. Connect these to the non-inverting inputs of each of the four comparators in your LM339 IC.
- The outputs of all four of the comparators in your LM339 IC will be connected together to form the "Bus", with the single 10 kΩ pullup shown.

Question 1

Not yet answered

Marked out of 4.00

In Multisim or a similar schematic capture package, draw your completed schematic. Take a screenshot of your finished schematic and upload it here for your instructor to grade out of four possible marks.

Maximum size for new files: 400MB

Files

You can drag and drop files here to add them.

Question 2

Not yet answered

Marked out of 3.00

Build your circuit on a breadboard, and test it as follows, using either an oscilloscope or a DMM to observe the activity of the bus.

1. With all of the other inputs set HIGH, can you communicate clearly with the Bus using any one channel? (Try this with each of the four inputs to verify your answer.) Choose...
2. Set any one of the channels LOW. Can you communicate clearly with the Bus using any one of the other channels? Choose...
3. Remove the pullup resistor from the Bus, and leave its location open. When any one of the inputs attempts to communicate, the bus output Choose...

Question 3

Not yet answered

Marked out of 3.00

Take a picture of your breadboard and upload it here for your instructor to grade out of three possible marks. If your instructor grades this in class, enter the grade given to you in the text field for this question.

Maximum size for new files: 400MB

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Information

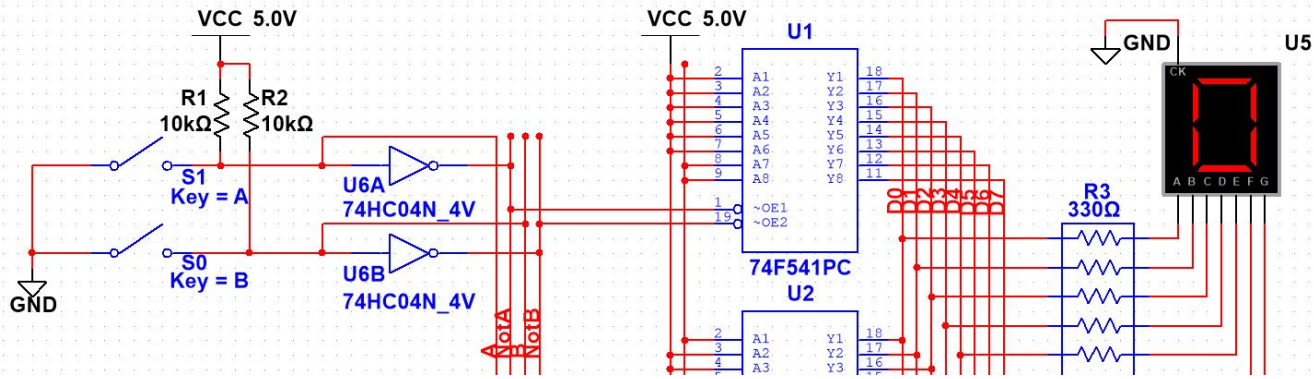
Tristate Bus

This exercise is to be completed in Multisim or a similar schematic capture and simulation package.

The 74541 Octal Buffer is an IC with tristate outputs, controlled by two Active-Low enable inputs. This allows us to individually select up to four devices fairly simply. Rather than manage both a unidirectional address bus and a bidirectional data bus as would be typical of a microcontroller-based system, we will build a simple unidirectional data bus to drive a seven-segment display. The idea is to select which buffer IC is connected to the bus and, therefore, to the seven-segment display. We will set the inputs to the buffers appropriately so we can identify which buffer is driving the bus.

Part 1 -- Design with Discrete Bus wires

The partial schematic below should give you a start on designing this circuit. The discussion that follows will help you develop the rest of it.



- Note that two Active-Low logic switches provide inputs to the active-low inputs of all four of the buffers. Usually, when we have active-low inputs on a logic device, we want the devices to be activated when the controlling circuits are activated. So, in this case, neither switch is activated (closed) so the first of the four buffers is selected while the rest are not. From a logic standpoint, the first buffer is activated because "NotA" and "NotB" are both LOW as a result of "A" and "B" both being HIGH when their switches are open (not activated).
- Your first task is to determine what combinations of A/NotA/B/NotB will enable the other buffers in order from top to bottom when the switches are activated (closed) in a binary sequence. Assume switch A is the MSB and B is the LSB.
- The inputs of the first buffer are wired HIGH or LOW to turn on the segments of the seven-segment display that look like "0". Note that the Seven Segment Display chosen is "Common Cathode", so the common cathode connection is to ground. The LED segments will turn on when the corresponding data line is HIGH, which will drive a current through the 330 Ω resistor in the 7-Line Isolated R-Pack to forward-bias the LED. (By the way, D7 isn't connected to anything on the Seven-Segment display, because this display doesn't have a "DP". Put D7 on your diagram anyway, for completeness.)
- Wire up the inputs for the remaining three buffers to display "1", "2", and "3" for the other switch combinations, keeping in mind that switch A is MSB and switch B is LSB.
- The outputs of all the buffers (Y1 through Y8) are wired together to form the unidirectional data bus.
- In Multisim, you can name and display the various connection nets by right-clicking on the wire, providing it a net name, and checking the box to display the net name. Then you can move/rotate the text that appears as you would anything else in Multisim. The arrow keys on your keyboard can be used for fine movement. Unfortunately, in Multisim you can only display the net name at one point on the schematic, which doesn't help much when it comes to troubleshooting connections! You'll overcome that problem in the next iteration of this design.

Question 4

Not yet answered

Marked out of 5.00

When you have completed your circuit, take screen-shots with the four possible settings of the logic switches showing their corresponding outputs on the seven-segment display, and upload them here. Your instructor will grade these out of five available marks. If your instructor grades this in class, use the text field for this question to enter the grade assigned.

Maximum size for new files: 400MB

Files

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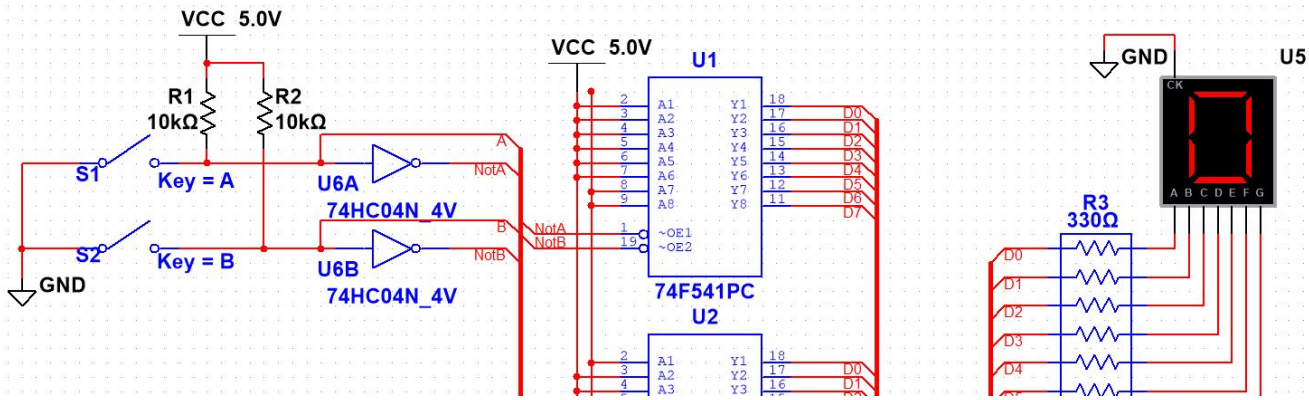
Information

Design with Bus Lines

Clearly, if you had a design with 48 address lines and 64 data lines, the schematic as drawn above would be completely covered with connecting wires. Schematic capture software allows for a variety of ways to clean up a schematic.

You've probably used one of these ways in a previous course -- using ***connectors*** which act as virtual connections between points on a wiring net. Typically in schematic capture software you can name the nets as well, then use the net name on a floating piece of wire to connect it to other points in the schematic.

Another very common way of cleaning up a schematic is that of combining a group of wires into a single thick bus line with bus connectors branching out of it, as shown in the partial schematic below.



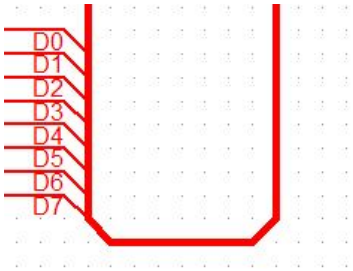
It should be apparent that this circuit is functionally identical to the first one, but much more tidy and more easily interpreted due to the bus lines and the net labels that appear throughout the schematic.

There are two different types of bus line connections available in Multisim, both of which are used in this partial schematic: individually named bus connections and vectored bus connections. We'll investigate both of these below.

- Start a new schematic, and copy/paste your previous schematic's contents into it to save you all the time of placing components.
- Delete the wiring associated with the various enables and data lines.

Individually Named Bus Connections

- Start with the "Enables" bus -- there's a special icon in the toolbar for drawing bus lines. You can draw angles, etc. at the corners of your bus line, can start in free space, and can end in free space with a double-click. Typically, bus lines are drawn with bevelled corners rather than just right angles, as shown below:



- Double-click the bus line, and change its name, which should show up on your schematic.
- In the Bus Properties window that appears when you double-click a bus line, select the "Bus lines" tab, and add. You will now have the option of "Add a bus line", which is the option you want to choose for individually named bus lines. Add the four Enable names.
- When you try to make a connection to the bus, a popup window will appear, allowing you to select the correct name for that connection.
- You will probably see the bus name and an arbitrarily-assigned net number in parentheses. That's a default sheet setting, which we will want to get rid of. Under "Edit -> Sheet Properties" you'll see "Bus entry"; uncheck "Bus entry net names" if it's checked, and the parentheses should disappear on all bus names.
- To keep your schematic tidy and easy to follow, rotate or flip the bus entry symbols so they point in the most likely direction for signal flow.

In Multisim, the bus line labels appear inside the corner of the bus connector, which is a bit non-standard -- many schematic capture packages will always put the label above the wire. When reading a schematic, take care when reading individual net labels.

Vectored Bus Connections

Since many of the buses used on a schematic are made up of a letter and a sequential number, vectored names make sense -- you don't have to individually create each numbered entry.

- Place a data bus line, and change its name to "Data".

- In the Bus Properties dialog "Bus lines" tab, select Add... as before. This time, however, select "Add bus vector", and put 'D' as the prefix. The Start value should be 0, the increment 1, and the Number 8 for the eight required data bus lines.
- As before, when you try to make a connection to the bus, you will get a popup from which you can select one of the eight bus lines.

Question 5

Not yet answered

Marked out of 5.00

When you have completed your bus-connected version of the schematic, again take four screenshots showing the schematic and the outputs for the four combinations of switches A and B, and upload them here for your instructor to grade out of five possible marks. If your instructor grades this in class, use the text field to enter the grade allotted.

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◄ Project 03: Digital Filtering (printable)

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