Current sense resistor - Gauge the flow of current
Low value, high power

Step-down voltage regulator - Buck converter
Reduce input voltage to a desired lower level efficiently
High level of efficiency & Minimizing energy loss
Based on the principle of switching power supply systems
DC-to-DC converter - Transistor and a diode -> Switch on and off ->
Control flow of energy from input to output

- **Duty cycle of switching transistor - Fraction of the total period for which the transistor is switched on - When transistor is on -> Energy stored in an inductor / When transistor is off -> Stored energy is released to the load - Effectively reducing the voltage**

PG Power good
Open-drain output - Whether output within the correct range
Connect to microcontroller / Status LED

FB Feedback pin
Voltage regulation - Set output voltage

EN Enable
Turn the regulator on or off

SW Switch node
Switching output - High-frequency pulsed voltage
Latter regulated by an inductor
ON - MOSFET ON -> Connect SW to VIN - Current to build up in the inductor
OFF - MOSFET OFF -> Release stored energy

TPS62A01 - Step-down (buck) converter
High-efficiency synchronous buck converter
High input voltage -> Low stable output voltage - Minimal power loss
Switching regulator - Rapidly switches an internal MOSFET to transfer energy to output
Input voltage - 2.3V - 5.5V
Output voltage 0.6V-4.8V
Maximum output current - 2A
Efficient - Up to 96%
Switching frequency - 2.4 MHz
Integrated MOSFET - Reduce external component count

5 Pin Configuration and Functions

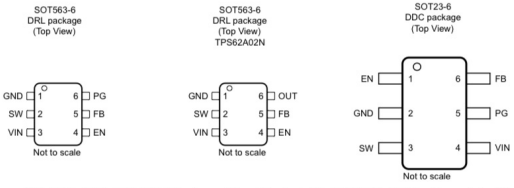


Figure 5-1. 6-Pin DRL SOT-563 Package (Top View), 6-Pin DDC SOT-23 Package (Top View)

Table 5-1. Pin Functions

Pin Number			Type[1]	Description
Name	SOT563-6	SOT23-6		
EN	4	1	I	Device enable logic input. Logic high enables the device. Logic low disables the device and turns the device into shutdown. Do not leave the pin floating.
FB	5	6	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	1	2	G	Ground pin.
PG	6	5	O	Power-good open-drain output pin. The pullup resistor cannot be connected to any voltage higher than 5.5V. If unused, leave the pin open or connect to GND.
OUT[2]		/	I	Output voltage sense pin.
SW	2	3	O	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	3	4	I	Input voltage pin. Connect the input capacitor as close as possible between V_{IN} and GND.

(1) I = Input, O = Output, G = Ground.
(2) Only for TPS62A0x**N** versions.

LD57100JR
Low-dropout regulator (LDO) - DC linear voltage regulator
Operate a small difference between input supply voltage and output voltage
High voltage -> Lower voltage - Ensure the voltage stability in a circuit
Maintain a small voltage difference between the input voltage and output voltage - High efficiency
Power management - Stabilize output voltage levels
Isolate loads from noisy power sources -> Low-noice power supplies - Sensitive electronic circuits

Ferrite bead 铁氧体磁珠 -> Anti-interference
Noise filtering & EMI suppression
Clean power delivery
Electrical function: Resemble an inductor - Frequency response deviates from this functionality at high frequencies
High impedance & Low permeability -> Power filtering
Better high-frequency filtering characteristics than ordinary inductors -> Resistance at high frequencies - Maintain a high impedance in a wide frequency range -> Improving the frequency modulation filtering effect

LDO
FB Feedback pin
Voltage regulation - Set output voltage

VBIAS Bias voltage
Provide internal bias voltage - Improve efficiency / Lower dropout voltage

EN Enable
Turn the regulator on or off

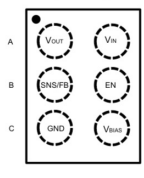


Table 1. **Pin description**

Pin #	Symbol	Functions
A1	V_{OUT}	Output voltage
A2	V_{IN}	Input voltage
B1	SNS / FB	Output voltage sense pin in fixed version. Connect to the load with a separate PCB track. Feedback pin in adjustable version. Connect to the resistor divider central node
B2	EN	Enable pin logic input: low = shutdown, high = active
C1	GND	Common ground
C2	V_{BIAS}	Bias supply input

ADC (HMCAD1511) - High-speed 8 / 10 bits ADC
Used in RF Communications High-speed data acquisition systems
Multi-channels
Output - Differential digital signals

PLL module (Clock management Green box)
Generate and condition ADC sampling clock
Communicate through I^2C (SDA/SCL)

VCM Input common-mode voltage range
DC-coupled inputs + Single-supply power
Input signals fed to amplifier and ADC should be biased at a DC level within the VCM range -> Eliminate a major barrier to amplifier and ADC design - Low distortion + High linearity

Bias point - Operating point
DC voltage / Current - Instantaneous value might vary

UFL connectors
Provide external clock inputs for ADC
ADC_CLK P/N - High-frequency clock input - From Low-jitter clock source (PLL or Oscillator)
External clocking - Synchronized sampling with the system's data processing unit (FPGA / DSP)

FCLK Frame clock
Synchronize data frame transmission from ADC to the processor / FPGA
Ensure proper alignment of the digitized signals

LCLK Line clock
Control data word timing for each line of ADC output
Work in sync with FCLK to maintain data integrity + avoid timing errors

Both clocks are differential signals - Better noise immunity and reduced jitter

VCM Common-mode voltage bias point
Midpoint reference voltage - Bias differential analog signal

Ensure input signals remain within ADC's optimal dynamic range
Provide a stable DC bias for differential pairs - Signal integrity
VCM - Provided by ADC - Connected to external component as to stabilize input signals
Capacitor (C134 100nF) - Decoupling - Reduce noise at the VCM node

Features of HMCAD1511
8-bit High Speed Single/ Dual/ Quad ADC
Single Channel Mode: FSmax = 1000 MSPS
Dual Channel Mode: FSmax = 500 MSPS
Quad Channel Mode: FSmax = 250 MSPS
Integrated Cross Point Switches (Mux Array)
1X to 50X digital gain
No missing codes up to 32X
1X gain: 49.8 dB SNR
10X gain: 48.2 dB SNR
Internal low jitter programmable Clock Divider
Ultra Low Power Dissipation
710 mW including I/O at 1000 MSPS
0.5 μs start-up time from Sleep, 15 μs from Power Down
Internal reference circuitry with no external components required
Coarse and fine gain control
Digital fine gain adjustment for each ADC
Internal offset correction
1.8 V supply voltage
1.7 - 3.6 V CMOS logic on control interface pins
Serial LVDS/RS DS output
7x7 mm QFN 48 Pin (LP7D) Package

Bias point - Operating point -> Ensure signals stay within operating limits
Steady-state voltage or current - Proper operation of active component - Transistors / Amplifier / ADC input stages

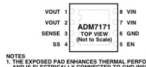
PCIe edge connector (P1)
PCIe x4 interface - Power Data transmission Control signals
Differential TX and RX lanes for PCIe Gen 1/2/3/4 speeds - Data transfer
High-speed serial communication - Reduced noise & Interference

Reference clock - REFCLK 100MHz PCIe clock
Reset control - RERST#
Presence detection - PRSNT

ADM7171ACPZ-5.0
Low-dropout (LDO) linear regulator - Manipulated by Analog devices
High accuracy, Low noise, High power supply rejection ratio
Powering High-speed ADCs DACs PLLs RF circuits High-speed FPGA and DSP power rails
Fixed output voltage - 5.0V
Input voltage range - Up to 6.5V
Maximum output current - 500mA

LM27761 85%
Charge pump inverter - Generate -5V from 5.2V
Low-noise inverting charge pump - Regulated negative output voltage
Generate a stable negative voltage from single positive supply
Low-power + Noise-sensitive applications
Input voltage range - 2.7V - 5.5V
Output voltage - Adjustable negative voltage (Up to -5V)
Output current - Up to 250mA
Efficiency - Up to 85%

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



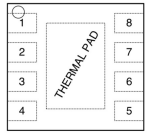
NOTES
1. THE EXPOSED PAD ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO GND INSIDE THE PACKAGE. CONNECT TO GND ON THE GROUND PLANE ON THE BOARD TO ENSURE PROPER OPERATION.

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT	Regulated Output Voltage. Bypass this pin to GND with a 4.7 µF or greater capacitor.
2	VOUT	Regulated Output Voltage. This pin is internally connected to Pin 1.
3	SENSE	Sense Input. Connect this pin as close as possible to the load for best load regulation. Use an external resistor divider to set the output voltage higher than the fixed output voltage.
4	SS	Soft Start. A 1 nF external capacitor connected to SS results in a 1.0 ms start-up time.
5	EN	Regulator Enable. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN (Pin 7 or Pin 8).
6	GND	Ground.
7	VIN	Regulator Input Supply. Bypass this pin to GND with a 4.7 µF or greater capacitor.
8	VIN	Regulator Input Supply. This pin is internally connected to Pin 7.
9	EP	Exposed Pad. The exposed pad is on the bottom of the package. The exposed pad enhances thermal performance and is electrically connected to GND inside the package. Connect the exposed pad to the ground plane on the board to ensure proper operation.

DSG Package
8-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NUMBER	NAME		
1	VIN	P	Positive power supply input.
2	GND	G	Ground
3	CPOUT	P	Negative unregulated output voltage.
4	VOUT	P	Regulated negative output voltage.
5	VFB	P	Feedback input. Connect VFB to an external resistor divider between VOUT and GND. *DO NOT* leave unconnected.
6	EN	I	Active high enable input.
7	C1–	P	Negative terminal for C1.
8	C1+	P	Positive terminal for C1.
—	Thermal Pad	G	Ground. *DO NOT* leave unconnected.

DC_CPL DC coupling control
Configure whether AC or DC coupling is used

PGA_CSn, PGA_SCLK, PGA_SDIO
SPI interface for controlling the PGA settings

TRIM
Calibration or fine tuning for gain and offset

Multi-channel programmable gain amplifier (PGA) front-end system
Analog signal acquisition & conditioning & processing -sent to-> ADC
Differential output (OUT P / OUT N) - High-speed + Low-noise differential format
Controlled via SPI (PGA_CSn, PGA_SCLK, PGA_SDIO) ->
Adjustable gain settings
Amplifiers with adjustable multiples

OP07CDR
Precision operational amplifier - Voltage buffer -> Bias generation
Low-impedance + Noise-free bias source
Low-offset + High-precision operational amplifier (op-amp) -> High-accuracy signal processing applications
Ultra-low input offset voltage + Low-drift + High common-mode rejection
Low input offset voltage - 75µV (max)
Low input bias current - 1.8nA
Low noise
High common-mode rejection ratio 120dB
High open-loop gain - 100dB
Wide supply voltage range - +-3V - +-18V / 6V - 36V
Package type - SOIC-8 (CDR suffix)
ADC front-end buffers
Generate stable bias voltage

TPS7A2033 - 3.3V LDO linear voltage regulator
Power stabilization + Low noise
Powering low-power digital circuits
Output voltage - 3.3V
Input voltage range - 2.7V to 6.5V
Maximum output current - 200mA
Low dropout voltage
Low quiescent - 31µA
Package - SOT-23

Pin Functions: X2SON, SOT-23

PIN			I/O	DESCRIPTION
NAME	X2SON	SOT-23		
IN	4	1	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUT	1	5	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150Ω (typical) pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode ($V_{EN} < V_{ENLOW}$).
EN	3	3	I	Enable input. A low voltage (< V_{ENLOW}) on this pin turns the regulator off and discharges the output pin to GND. A high voltage (> V_{ENHI}) on this pin enables the regulator output. This pin has an internal 500kΩ pulldown resistor to hold the regulator off by default. When $V_{EN} > V_{ENHI}$, the 500kΩ pulldown is disconnected to reduce input current.
GND	2	2	—	Common ground.
N/C	—	4	—	No internal electrical connection.
Thermal Pad	5	—	—	Thermal pad for the X2SON package. Connect this pad to GND or leave floating. Do not connect to any potential other than GND. Connect the thermal pad to a large-area ground plane for best thermal performance.

MCP4432T-503E - Qual-channel Digital potentiometer
I^2C-controlled - Adjustable resistance trimming
Resistor taps - 128 position (7-bit resolution)
Resistance options - 5kΩ 10kΩ 50kΩ 100kΩ
Operating voltage 1.8V to 5,5V
Wiper Non-volatile memory (EEPROM) - Retain settings after power los

MCP4728 - Qual-channel DAC
4-channel 12-bits DAC
I^2C-controlled -> Precise analog voltage trimming / generation
Resolution - 12-bit (4096 discrete voltage levels)
Output voltage - Configurable (Buffered)
Operating voltage - 2.7V to 5.5V
Non-volatile memory (EEPROM) - Store DAC settings

DMN62D0UW - MOSFET -> Level shifting

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Name	Pin Type	Function
1	V_{DD}	P	Supply Voltage
2	SCL	OI	I^2C Serial Clock Input **(Note 1)**
3	SDA	OI/OO	I^2C Serial Data Input and Output **(Note 1)**
4	$\overline{LDAC}$	ST	This pin is used for two purposes: (a) Synchronization Input. It is used to transfer the contents of the DAC input registers to the output registers (V_{OUT}). (b) Select the device for reading and writing I^2C address bits. **(Note 2)**
5	RDY/$\overline{BSY}$	OO	This pin is a status indicator of EEPROM programming activity. An external pull-up resistor (about 100 kΩ) is needed from RDY/$\overline{BSY}$ pin to V_{DD} line. **(Note 1)**
6	V_{OUT} A	AO	Buffered analog voltage output of channel A. The output amplifier has rail-to-rail operation.
7	V_{OUT} B	AO	Buffered analog voltage output of channel B. The output amplifier has rail-to-rail operation.
8	V_{OUT} C	AO	Buffered analog voltage output of channel C. The output amplifier has rail-to-rail operation.
9	V_{OUT} D	AO	Buffered analog voltage output of channel D. The output amplifier has rail-to-rail operation.
10	V_{SS}	P	Ground reference.

Legend: P = Power, OI = Open-Drain Input, OO = Open-Drain Output, ST = Schmitt Trigger Input Buffer, AO = Analog Output

Note 1: This pin needs an external pull-up resistor from V_{DD} line. Leave this pin float if it is not used.
2: This pin can be driven by MCU.

Attenuation - Loss in signal strength

BNC connector (Bayonet Neill-Concelman)
Coaxial connector - Radio frequency connection
Quick and secure connections in various electronic and networking applications
Provide input / output for high-frequency signals

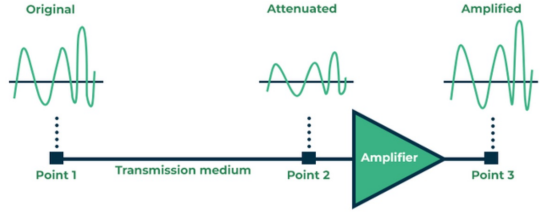
Relay
Electrically operated switch - One circuit to control another circuit
Switch the signal path between direct transmission / attenuation

MOSFET transistor Metal Oxide Semiconductor Field-Effect Transistor
Field-effect -> Switching and amplifying signals
Structure - Source Drain Gate Body
Function - Voltage - Gate controls -> Conductivity between source and drain - Efficient control of electrical current
Switch -> Control relay activation

Protection diode
Two-terminal electronic component -Conduct current in one direction
Protect circuit & Transforming AC into DC
Prevent voltage spikes

Relays toggle between direct signal transmission and attenuation
Transistors and diodes manage relay control and protection
Capacitors and resistors ensure proper. Impedance matching

Attenuation	Amplification
It is the reduction in signal strength as it propagates from source to destination.	It is the method to increase the signal strength to compensate the loss of signal.
It is a passive process which occurs naturally due to intrinsic and extrinsic factors.	It is a active process which occurs through the use of amplification devices.
It causes signal degradation, data loss and limits range.	It results in enhanced signal quality, data reliability and improved range by overcoming attenuation.
It happens because of interference, scattering, absorption, bending losses.	It is done using signal boosters, amplifiers, repeaters.



DMN62D0UW MOSFET transistor
N-channel enhancement-mode MOSFET
Low-voltage switching application
Maximum Drain-Source Voltage - 20V
Continuous Drain Current - 1.5A
Low on-resistance ~0.1Ω
Grate threshold voltage - 0.6V~1.5V

1N4148 - Fast switching diode
High-speed Si switching diode - Signal processing & Protection circuit
Maximum Drain-source voltage - 100V
Forward current - 300mA
Forward voltage drop ~0.7V at 10mA
Switching speed 4ns
Package - DO-35
Limiting voltage spike

BSS84
P-channel MOSFET
Switching applications in low-voltage power control circuit
Maximum Drain-source voltage - 50V
Continuous Drain current - 130mA
On-resistance - 10Ω
Grate threshold voltage -0.8V to -2V
Package - SOT-23

FTR-B3SA4.5Z - Signal relay
Series - FTR-B3 (Subminiature Signal Relay)
Coil voltage - 4.5V DC
Contact form - SPST-NO (Single Pole Single Throw)
Coil type - Non-latching
Contact rating - Up to 1A at 30V DC / 0.5A at 125V AC
Features:
- **High sensitivity**
- **Small size**
- **Designed for signal switching**
- **Low power consumption**

OP07C/RC - Amplify voltage
Precision amplifier for signal conditioning
Low-offset precision op-amp
High-accuracy signal processing
Control signal path

- **Amplification - Boosting signal strength**
- **Mathematical operations - Analog computer**
- **Oscillators and waveform generation**
- **Filtering - Shaping the frequency spectrum**
- **Comparison - Detecting voltage level**

LMH6518
Digitally controlled variable gain amplifier (VGA)
Adjust signal gain dynamically
Control signal path

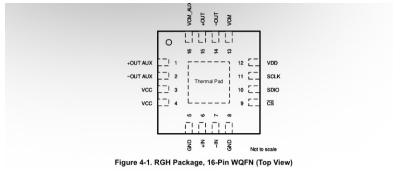


Figure 4-1. RGH Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	+OUT AUX	O	Auxiliary positive output
2	–OUT AUX	O	Auxiliary negative output
3	VCC	P	Analog power supply
4	VCC	P	Analog power supply
5	GND	G	Ground, electrically connected to the WQFN heat sink
6	+IN	I	Positive input
7	–IN	I	Negative input
8	GND	G	Ground, electrically connected to the WQFN heat sink
9	$\overline{CS}$	I	Serial chip select (SPI, active low): While this signal is asserted, SCLK is used to accept serial data present on SDIO and to source serial data on SDO. When this signal is deasserted, SDIO is ignored and SDIO is in a high-impedance state.
10	SDIO	I/O	Serial data-in or data-out (SPI): During a write operation, serial data are shifted into the device (8-bit command and 16-bit data) on this pin while $\overline{CS}$ signal is asserted. During a read operation, serial data are shifted out of the device on this pin while $\overline{CS}$ signal is asserted. At other times, and after one complete access cycle (24 bits; see Figure 6-1 and Figure 6-2), this input is ignored. This output is in a high-impedance state when $\overline{CS}$ is deasserted. This pin is bidirectional.
11	SCLK	I	Serial clock (SPI): Serial data are shifted into and out of the device synchronous with this clock signal. SCLK transitions with $\overline{CS}$ deasserted are ignored. To minimize digital crosstalk, stop SCLK when not used.
12	VDD	P	Digital power supply
13	VCM	I	Input from ADC to control main output common mode (CM) voltage
14	–OUT	O	Main negative output
15	+OUT	O	Main positive output
16	VCM_AUX	I	Input to control auxiliary output CM voltage
Pad	Thermal Pad	—	Thermal pad (WQFN heat sink), electrically connected to pins 5 and 8 (GND)

(1) G = ground, I = input, O = output, P = power

BNC / UFL connector
High-frequency signal input / output

Biasing circuit(R_bias C_bias Voltage divider)
Biasing network for op-amp and amplifier circuits
Provide stable reference voltage for amplifier

SPI/I^2C control signal (SDA SCLK SDIO SDO)
Digital programmability
Allow Dynamic gain adjustment

VGA Variable Gain Amplifier - Voltage-Controlled Amplifier
Adjust its gain based on a control voltage
Function - Vary amplification level according to a control signal ->
Flexible signal strength management

Signal conditioning
Electronic circuit -> Manipulation of an analog signal to prepare for further processing / measurement / transmission -> Improve accuracy + reliability - Suitable for subsequent stage

RF application Radio frequency
Enable wireless transmission and reception of information over airwaves for seamless communication

BUF802 Wideband Buffered Operational Amplifier
High-speed, wideband buffer amplifier
-> Low noise / High bandwidth / High slew rate
Signal conditioning / RF application
High bandwidth >2GHz -> High-speed analog applications
Low input bias current
Low noise
High slew rate -> Fast signal transitions
Wide supply voltage range +-2.5V to +-6.5V (Dual supply) / 5V to 13V (Single supply)
Can be used as a Buffer / Active gain configuration
Integrated ESD protection - Protect against electrostatic discharge - Reliability in sensitive circuits

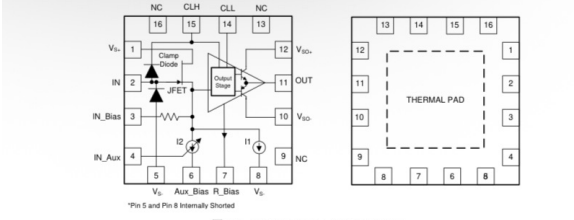


图 5-1. RGT Package, 16-Pin VQFN (Top View and Bottom View)

表 5-1. Pin Functions

PIN		TYPE(4)	Operating Mode(1) (2)	DESCRIPTION
NAME	NO.			
Aux_Bias	6	P	CL	Connect to V_{S-} to enable control of OUT through the In_Aux.
CLH	15	I	BF, CL	Input pin for setting positive clamp voltage
CLL	14	I	BF, CL	Input pin for setting negative clamp voltage
IN	2	I	BF, CL	Signal input
In_Aux	4	I	CL	Auxiliary input for controlling OUT through an external amplifier.
In_Bias	3	I	CL	JFET biasing pin
NC	16, 13, 9	—	—	Do not connect.
OUT	11	O	BF, CL	Signal output
R_Bias	7	I	BF, CL	Output stage bias current setting pin
V_{S+}	1	P	BF, CL	Positive power supply connection for Input Stage.
V_{S-}	5, 8	P	BF, CL	Negative power supply connection for Input Stage. Pin 5 and Pin 8 are internally shorted.
V_{SO+} (3)	12	P	BF, CL	Positive power supply connection for Output Stage.
V_{SO-} (3)	10	P	BF, CL	Negative power supply connection for Output Stage.
Thermal Pad		—	—	The thermal pad is electrically isolated from the die and pins. Connect the thermal pad to any potential.

(1) See 节 8.4 for more information on *Buffer Mode (BF)* and *Composite Loop Mode (CL)* functional modes.
(2) Pins specified as *CL* should only be used when operating in *Composite Loop Mode* and left floating when operating in *Buffer Mode*.
(3) V_{SO} and V_S should be tied to the same potential since they are internally connected to each other through back-to-back diodes.
(4) I = input, O= output, P= power, NC = no connect.

TS12A4516 Analog switch
Single-pole, single-throw (SPST) analog switch Normally Open (ON)
-> Low-voltage + High-speed signal switching application
CMOS technology - Low power consumption + Low ON resistance
Operating voltage - 1.65V - 5.5V - Low-power application
ON resistance - 1.5Ω typical - Minimal signal loss
Fast switching time

- **Turn-on time - 23ns**
- **Turn-odd time - 18ns**

Low leakage current - Signal integrity when switch is off
Low power consumption - CMOS - Reduce overall power usage
Package option - Available in small SOT-23 / SC-70 packages for compact circuit designs

- **Enable / disable a signal path**
- **Controlled by a logic signal**
- **Low ON resistance - Minimal signal distortion / attenuation**
- **Fast switching time - Suitable for high-speed signal application**

Absolute Minimum and Maximum Ratings(1)(2)

voltages referenced to 0 V

			MIN	MAX	UNIT
V_+	Supply voltage range		–0.3	13	V
V_{NC} V_{NO} V_{COM}	Analog voltage range(3)		V_- –0.3	V_+ + 0.3	V
V_{IN}	Logic input range		V_- –0.3	V_+ + 0.3	V
	Continuous current into any terminal			±20	mA
	Peak current, NO or COM (pulsed at 1 ms, 10% duty cycle)			±30	mA
	ESD per method 3015.7			>2000	V
	Continuous power dissipation (T_A = 70°C)	8-pin SOIC (derate 5.88 mW/°C above 70°C)		471	mW
		5-pin SOT23-5 (derate 7.1 mW/°C above 70°C)		571	
T_A	Operating temperature range		–40	85	°C
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) Voltages exceeding V_+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

DC_CTRL DC control signal
Digital control signal - Enable or disable a circuit function
A control signal - Enable / disable part of the circuit

- **Turn on / off a transistor or MOSFET switch**
- **Activating / Deactivating an analog switch**
- **Controlling a relay or power gate**

High signal (logic 1 /3.3V or 5V) - Turn ON a circuit
Low signal (logic 0 / 0V)- Turn OFF a circuit
Control signal to turn the MOSFET on / off

AVSEE Power rail / Analog voltage reference

- **Analog voltage supply**
- **Reference voltage**
- **Low-noise analog power**

Analog voltage supply or reference used in signal processing circuit - Powering op-amps / Analog signal paths
Likely an analog or auxiliary power source

Mounting hole
Chassis grounding and mechanical mounting points for PCB stability and Electromagnetic interference EMI shielding
Connected to GND for EMI shielding

MGT_TXx_P/N & MGT_RXx_P/N
High-speed differential TX / RX signals for PCIe

PERx_P/N & PETx_P/N
PCIe Transmit and Receive lanes
Transmitting and receiving high-speed data - High-speed communication

PERx_REFCLK_P/N
Reference clock signal to synchronize data transmission

M2_X4_TX & M2_X4_RX
PCIe signal lanes for M.2 interface

M.2 PCIe interface
High-speed connector standard -> Compact storage and expansion device
Support multiple protocols - PCIe / SATA / USB3.0/2.0
Connector keying - 75-pin edge connector - Multiple key notches
Key types
- **M-key - SSD**
- **B-key - WWAN**
- **A+E key - Wi-Fi**

High-speed data transfer
- **PCIe Gen 3.0 x4 - 3.94GB/s**
- **PCIe Gen 4.0 x4 - 7.88GB/s**
- **PCIe Gen 5.0 x4 - 15.75GB/s**

Low power consumption & Efficiency - Support Active State Power Management ASPM

PCIe - Peripheral Component Interconnect Express
High-speed serial communication interface

- **Differential signaling - Noise-resistant high-speed data transfer**
- **Support multiple generation - Increasing bandwidth**

Lane based architecture - Differential pairs -> Lanes
Point-to-point topology (No bus sharing)

- **Communicate directly to root complex (CPU / chipset)**
- **X share bandwidth & Each device gets dedicated lanes**

Backwards compatibility - PCIe 4.0 can work with PCIe 3.0 slot

ADC differential pairs
High-speed ADC input channels for data acquisition

Merged SPI buses - PGA_SDI / PGA_SCLK / PGA_CSn
SPI communication for configuring PGAs and ADCs

Joint Test Action Group JTAG header
Standardized debugging + testing + programming interface - Communicate with digital ICs (FPGAs Microcontrollers(MCU) CPUs)
Programming - Flash firmware onto FPGAs MCUs CPLDs
Debugging - Real-time debugging breakpoints and register access in processors
Boundary scan testing - Board-level testing
Debugging and programming interface for an FPGA / microcontroller

Hermaphroditic connector - High-density board interface
Connector can mate with itself - Eliminate the need for male and female connector
High-density connectors for interfacing with baseboards / expansion modules
Self-mating design - No need for separate male / female parts
Reduce inventory complexity - One connector type fits both end
High-density board-to-board connectors -> ADC differential signal routing
SPI clock signal

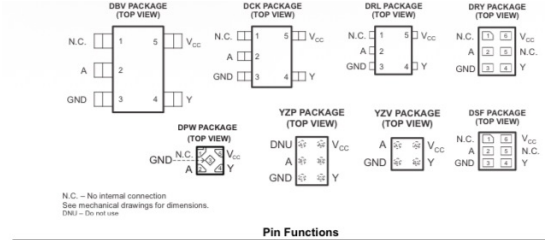
TPS7A2025 - LDO regulator - 3.3V to 2.5V
Low-noise stable efficient power source -> Clean power for LVDS signaling
Output voltage - Fixed 2.5V
Input voltage range - 2.7V to 6.5V
Maximum output current - 300mA
Low quiescent current - 25µA
High power supply rejection ratio (PSRR)
Ultra-low noise - 14µV RMS(10Hz-100kHz) - High-precision analog
Package option - 5-pin package

M.2 key M interface
PCIe-based NVMe SSDs / High-speed expansion cards
Custom pinout for an M.2 connector -> Communication between the main board and an M.2 device
Support PCIe NVMe SSDs - PCIe x4 lanes -> High-speed data transfer
Pin layout & keying - Different keying notches

M.2 key M connector
Main physical interface for connecting an M.2 device
Pin count - 75-pin edge connector
Support PCIe x4 lanes - Faster
Usage - NVMe SSDs AI accelerators High-speed PCIe cards

PERx_P/N (PCIe transmit / receive pairs)
High-speed data lanes for PCIe communication

REFCLK_P/N (Reference clock)
Provide timing reference for PCIe transaction



Pin Functions

PIN					DESCRIPTION
NAME	DBV, DCK, DRL, DPW	DRY, DSF	YZP	YZV	
NC	1	1, 5	A1, B2	-	Not connected
A	2	2	B1	A1	Input
GND	3	3	C1	B1	Ground
Y	4	4	C2	B2	Output
V_{CC}	5	6	A2	A2	Power terminal

Front end (Analog input stage) -> Signal conditioning

- Differential signal outputs <- Analog front-end circuit (AFE) - Process analog sensor data before conversion
- VCM - Reference voltage -> Differential signal processing
- SPI SCLK / SDIO / PGA control signal - Configuring PGA

ADC - Digitizing data

- REFINOUT - Reference voltage connection
- SPI control signals-> ADC configuration + operation
- I^2C lines -> Controlling a phase-locked loop (PLL) circuit - Clock synchronization

FPGA module - Real-time computation

- TE0712 (FPGA board) - System-on-module (SOM) FPGA board -> High-speed data processing
- High-speed differential signal line - Connecting ADC to FPGA
- Clock signals -> Synchronizing ADC data
- ACQ_EN / OSC_OE - Control signals -> Requisition and clock management

M.2 interface -> High-speed data transfer to a host system

- M2_TX/RX - High-speed communication lines for an M.2 device
- M2_GPIO - General-purpose I/O pins -> Additional control

Analog front-end (AFE) circuit
Process analog signals --> Digital form by ADC
Functions:

- Amplification - Boost weak signals - Op-amp / PGA
- Filtering - Remove unwanted noise and interference - Filters
- Impedance matching - Proper signal transfer - Sensor & Processing circuits
- Signal conditioning - Offset correction + Attenuation + DC biasing
- Differential to singe-ended conversion - Differential signals -> Single-ended signals - Easier processing

Phase-locked loop (PLL) circuit
Feedback control system - Stable, synchronized output clock signal - Locking onto the phase of an input signal
Components:

- **Phase detector (PD) - Phase difference between the input signal & PLL output**
- **Low-pass filter (LPF) - Filter out high-frequency noise from phase detector**
- **Voltage-controlled oscillator (VCO) - Output signal - Frequency is adjusted based on the phase error**
- **Frequency divider - Adjust the output frequency by dividing it down to match the reference signal**

System-on-module (SOM) FPGA board
Simplify FPGA-based development - Ready-to-use platform
Pros:

- **Modular design - Easily integrate into custom hardware**
- **Pre-validated hardware - Reduce development time - Providing test components**
- **Scalability - Upgrading to more powerful FPGAs**

BNC connector
Coaxial RF connector - Signal transmission

- **Bayonet locking mechanism - Stable connection + Prevent accidental disconnection**
- **Frequency range - 4GHz**
- **Coaxial design - Shielding against interference and signal loss**
- **Versatile usage - Support analog and digital signals**

Allowing connection of oscilloscope probes

- **SYNC1 - Synchronization signal output for external measurement**
- **REFINOUT1 - Distribute a reference output voltage for synchronization**

TPD1E10B04 Transient voltage suppression TVS diode
Used for Electrostatic discharge (ESD) protection
Prevent voltage spikes from damaging sensitive electronic circuits

- **Low capacitance ~0.55 pF - Protecting high-speed signal**
- **ESD protection - IEC 61000-4-2 standard - Withstand +-25 kV air discharge + +-15 kV contact discharge**
- **Low leakage current ~10nA max - Minimal power loss**
- **Unidirectional protection - Clamp voltage spikes above a safe threshold**

SYNC1
Synchronization signal output -> Timing alignment between multiple devices

- **Clock synchronization - Multiple-system operation**
- **Triggering events - Trigger oscilloscope measurements / test equipment**
- **Data alignment - Phase-coherent data acquisition**

REFINOUT1 - Reference signal output
Provide stable reference voltage / frequency for calibration + synchronization
Functions:

- **Voltage reference distribution - Share a common reference voltage with multiple circuits**
- **Clock reference - Frequency reference for PLLs or ADCs**
- **Stabilizing measurement systems - Same voltage reference to reduce measurement error**

R1 - 0Ω
Zero-ohm resistor - Jumper for flexibility in PCB design - Can be replaced

SN74LVC1G17 - Schmitt trigger buffer
Single Schmitt-trigger inverter - 74LVC1G17
Clean up noisy / slow input signals <- Hysteresis (滞后现象) - Well-defined digital output
Features:

- **Schmitt trigger action - Hysteresis - Different threshold voltages for high-to-low & low-to-high transitions -> Clean noisy / slow signal**
- **Wide operating voltage - 1.65V to 5.5V**
- **Fast propagation delay - 4.6 ns**
- **Low power consumption - CMOS technology - Low power operation**
- **Output drive strength - Source / sink up to 32mA**

Functionality:

- **Input signal processing - Noisy slow analog-like signal -> Sharp digital output**
- **Hysteresis effect - Input voltage rises above a certain threshold -> HIGH & Input voltage falls below a lower threshold -> LOW - Prevent unwanted switching - Noise**

10MHz crystal oscillator
Stable reference clock for the PLL
Precise clock source -> Timing-sensitive application
Frequency - 10MHz
Low phase noise & jitter - Essential for high-precision timing circuits
High stability - Consistent clock signals over varying temperature and voltages

ZL30260LDG1 - High-performance clock management and distribution IC
Generate and distribute precise clock signals for ADC synchronization
Clock inputs - External crystal oscillators (10MHz reference clock)
Clock outputs - Multiple synchronized clocks for ADCs FPGAs Processors
I^2C / SPI interface - Configuration via software
Jitter attenuation & Frequency translation - Reduce timing error for clock signals
Power supply - 3.3V and 1.8V (dual supply)

Table 1 - Pin Descriptions

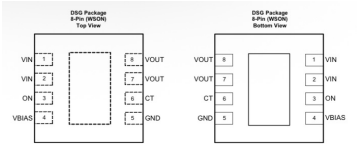
Pin #	Name	Type	Description
15, 16 18, 19 20	IC1P, IC1N IC2P, IC2N IC3P	I I I	**Input Clock Pins** Differential or Single-ended signal format. Programmable frequency. *Differential:* See Table 9 for electrical specifications, and see Figure 15 for recommended external circuitry for interfacing these differential inputs to LVDS, LVPECL, CML or HSCL output pins on neighboring devices. *Single-ended:* For input signal amplitude >2.5V, connect the signal directly to ICxP pin. For input signal amplitude ≤2.5V, AC-coupling the signal to ICxP is recommended. Connect the N pin to a capacitor (0.1µF or 0.01µF) to VSS. As shown in Figure 15, the ICxP and ICxN pins are internally biased to approximately 1.3V. Treat the ICxN pin as a sensitive node; minimize stubs; do not connect to anything else including other ICxN pins. *Unused:* Set ICEN.ICxEN=0. The ICxP and ICxN pins can be left floating. Note that the IC3N pin is not bonded out. A differential signal can be connected to IC3P by AC-coupling the POS trace to IC3P and terminating the signal on the driver side of the coupling cap.
12 13	XA XB	A / I	**Crystal or Input Clock Pins** *Crystal:* MCR2.XAB=01. An on-chip crystal driver circuit is designed to work with an external crystal connected to the XA and XB pins. See section 5.3.2 for crystal characteristics and recommended external components. *Input Clock:* MCR2.XAB=10. An external local oscillator or clock signal can be connected to the XA pin. The XB pin must be left unconnected. The signal on XA can be as large as 3.3V even when VDDH is only 2.5V.
8, 9 6, 5 2, 3 55, 56 53, 52 47, 48 45, 44 41, 40 37, 38 35, 34	OC1P, OC1N OC2P, OC2N OC3P, OC3N OC4P, OC4N OC5P, OC5N OC6P, OC6N OC7P, OC7N OC8P, OC8N OC9P, OC9N OC10P, OC10N	O	**Output Clock Pins** LVDS, programmable differential (which includes LVPECL), HCSL, HSTL or 1 or 2 CMOS. Programmable frequency. Programmable VCM and VOD in programmable differential mode. Programmable drive strength in CMOS and HSTL modes. See Figure 17 for example external interface circuitry. See Table 10, Table 11 and Table 12 for electrical specifications for LVDS, LVPECL and HCSL, respectively. See Table 13 for electrical specifications for interfacing to CMOS and HSTL inputs on neighboring devices. Outputs OC2, OC5, OC7 and OC10 are not present on 6-output products.
29	RSTN	I	**Reset (Active Low)** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as RSTN is low. Minimum low time is 1µs.
23 22 28	AC0/GPIO0 AC1/GPIO1 AC2/GPIO2	I/O	**Auto-Configure [2:0] / General Purpose I/O 0, 1 and 2** *Auto Configure:* On the rising edge of RSTN these pins behave as AC[2:0] and specify one of the configurations stored in ROM or EEPROM. See section 5.2.

Pin #	Name	Type	Description
			bidirectional data line between the device and an external I²C master. In I²C mode this pin should be externally pulled high by a 1kΩ to 5kΩ resistor. *SPI MOSI:* When the device is configured as a SPI slave, an external SPI master sends commands, addresses and data to the device on MOSI. When the device is configured as a SPI master (ZL30260, ZL30262 only), the device sends commands, addresses and data on MOSI to an external SPI EEPROM during auto-configuration.
11,17, 32,42	VDDH	P	**Higher Core Power Supply.** 2.5V or 3.3V ±5%. When VDDH=3.3V the device has additional internal power supply regulators enabled.
4,10, 14,31, 33,39, 49,50, 51	VDDL	P	**Lower Core Power Supply.** 1.8V ±5% or same voltage as VDDH.
30	VDDIO	P	**Digital Power Supply for Non-Clock I/O Pins.** 1.8V to VDDH.
7	VDDOA	P	**Power Supply for OC1P/N and OC2P/N.** 1.5V to VDDH.
1	VDDOB	P	**Power Supply for OC3P/N.** 1.5V to VDDH.
54	VDDOC	P	**Power Supply for OC4P/N and OC5P/N.** 1.5V to VDDH.
46	VDDOD	P	**Power Supply for OC6P/N and OC7P/N.** 1.5V to VDDH.
43	VDDOE	P	**Power Supply for OC8P/N.** 1.5V to VDDH.
36	VDDOF	P	**Power Supply for OC9P/N and OC10P/N.** 1.5V to VDDH.
E-pad	VSS	P	**Ground.** 0 Volts.

Important Note: The voltages on VDDL, VDDIO, and all VDDOx pins must not exceed VDDH. Not complying with this requirement may damage the device.

Pin #	Name	Type	Description
			General-Purpose I/O: After reset these pins are GPIO0, GPIO1 and GPIO2. GPIOCR1 and GPIOCR2.GPIO2C configure these pins. Their states are indicated in GPIOSR which has both real-time and latched status bits. Note that when the power supply arrangement for the device has VDDL=1.8V, during the interval between VDDH ramping and VDDL ramping these pins can briefly behave as an output driving high.
21	TEST/GPIO3	I/O	**Factory Test / General Purpose I/O 3** *Factory Test:* On the rising edge of RSTN the pin behaves as TEST. Factory test mode is enabled when TEST is high. Typically TEST should be low on the rising edge of RSTN, but see section 5.2 for some options where TEST can be high on the rising edge of RSTN. *General-Purpose I/O:* After reset this pin is GPIO3. GPIOCR2.GPIO3C configures the pin. It state is indicated in GPIOSR which has both real-time and latched status bits. Note that when the power supply arrangement for the device has VDDL=1.8V, during the interval between VDDH ramping and VDDL ramping this pin can briefly behave as an output driving high.
27	IF0/CSN	I/O	**Interface Mode 0 / SPI Chip Select (Active Low)** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF0 and, together with IF1, specifies the interface mode for the device. See section 5.2. *SPI Chip Select:* After reset this pin is CSN. When the device is configured as a SPI slave, an external SPI master must assert (low) CSN to access device registers. When the device is configured as a SPI master (ZL30260, ZL30262 only), the device asserts CSN to access an external SPI EEPROM during auto-configuration and then changes CSN to an input during normal operation. CSN should not be allowed to float.
26	IF1/MISO	I/O	**Interface Mode 1 / SPI Master-In-Slave-Out** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF1 and, together with IF0, specifies the interface mode for the device. See section 5.2. *SPI MISO:* After reset this pin is MISO. When the device is configured as a SPI slave, the device outputs data to an external SPI master on MISO during SPI read transactions. When the device is configured as a SPI master (ZL30260, ZL30262 only), the device receives data on MISO from an external SPI EEPROM during auto-configuration.
24	SCL/SCLK	I/O	**I²C Clock / SPI Clock** *I²C Clock:* When the device is configured as an I²C slave, an external I²C master must provide the I²C clock signal on the SCL pin. In I²C mode this pin should be externally pulled high by a 1kΩ to 5kΩ resistor. *SPI Clock:* When the device is configured as a SPI slave, an external SPI master must provide the SPI clock signal on SCLK. When the device is configured as a SPI master (ZL30260, ZL30262 only), the device drives SCLK as an output to clock accesses to an external SPI EEPROM during auto-configuration.
25	SDA/MOSI	I/O	**I²C Data / SPI Master-Out-Slave-In** *I²C Data:* When the device is configured as an I²C slave, SDA is the

TPS22975 - Load switch IC - High-current load switch
Control 3.3V power to relays
Input voltage range - 0.6V to 5.7V
Maximum load current - 6A
Loon-resistance
Integrated soft-start
Fast shutdown



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2. See the *Application and Implementation* section for more information
2			
3	ON	I	Active high switch control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.7 V. See the *Application and Implementation* section for more information
5	GND	—	Device ground
6	CT	O	Switch slew rate control. Can be left floating. See the *Adjustable Rise Time* section under *Feature Description* for more information
7	VOUT	O	Switch output
8			
—	Thermal Pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout Example* section for layout guidelines

TPS61023 - Boost converter (Step-up regulator)
High-efficiency boost converter - Step up low voltage to higher voltages
Convert VUSB to 5.23V
Output voltage - Adjustable up to 5.5V
Maximum output current - 2.4A
High efficiency - Up to 95%

5 Pin Configuration and Functions

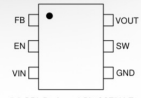


Figure 5-1. DRL Package 6-Pin SOT563 Top View

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	FB	I	Voltage feedback of adjustable output voltage
2	EN	I	Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode.
3	VIN	I	IC power supply input
4	GND	PWR	Ground pin of the IC
5	SW	PWR	The switch pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.
6	VOUT	PWR	Boost converter output

TPS562202 - Buck converter (Step-down regulator)
Synchronous step-down converter - Reduce high voltages
Convert 12V to 5V
Input voltage - 4.5V to 17V
Output voltage - Adjustable from 0.76V to input voltage
Output current - 2A maximum
Efficiency - Up to 95%

FE_EN / ACO_EN - Enable control signal
Enable signal for controlling power sections
FE_EN (Front-end enable)
Control power to the front-end analog circuitry

ACO_EN (Acquisition enable)
Enable power switch (TPS22975) to activate relays or acquisition circuits

6 Pin Configuration and Functions

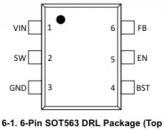
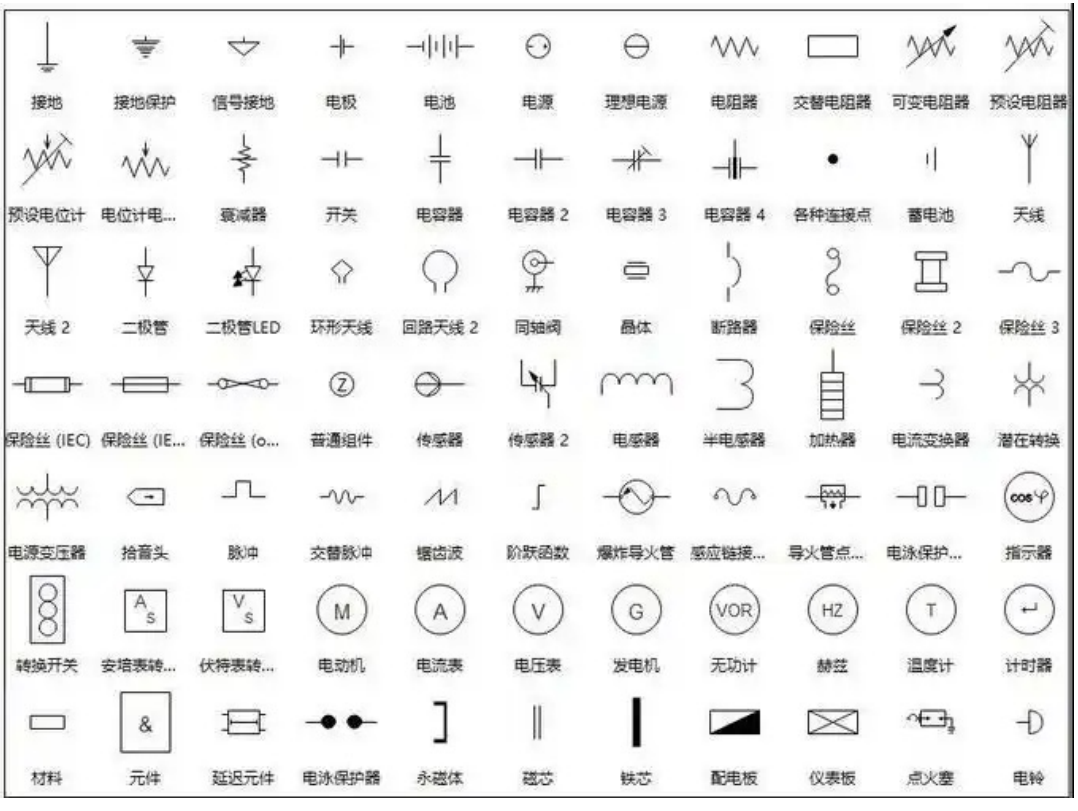


Figure 6-1. 6-Pin SOT563 DRL Package (Top View)

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	Input voltage supply pin
SW	2	O	Switch node connection between high-side NFET and low-side NFET
GND	3	—	Ground pin source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive FB to this GND at a single point.
BST	4	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1-µF capacitor between BST and SW pin.
EN	5	I	Enable input control. Active high. Must be pulled up to enable the device.
FB	6	I	Converter feedback input. Connect to output voltage with feedback resistor divider.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信号接地
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理想电源
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预设电阻器
预设电位计
电位计电...
衰减器
开关
电容器
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电容器 3
电容器 4
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天线
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潜在转换
电源变压器
拾音头
脉冲
交替脉冲
锯齿波
阶跃函数
爆炸导火管
感应链接...
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指示器
转换开关
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伏特表转...
电动机
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电压表
发电机
无功计
赫兹
温度计
计时器
材料
元件
延迟元件
电泳保护器
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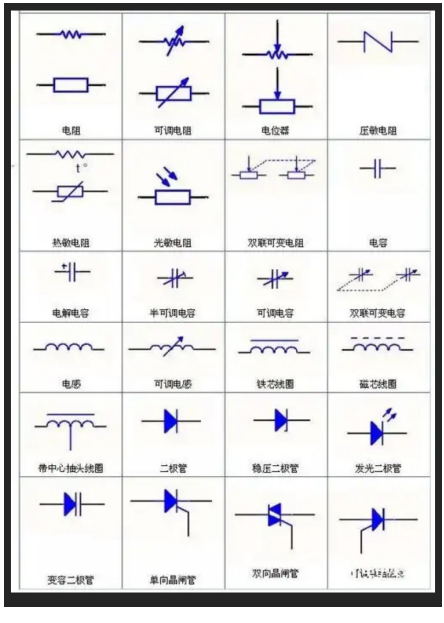
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电解电容
半可调电容
可调电容
双联可变电容
电感
可调电感
铁芯线圈
磁芯线圈
带中心抽头线圈
二极管
稳压二极管
发光二极管
变容二极管
单向晶闸管
双向晶闸管