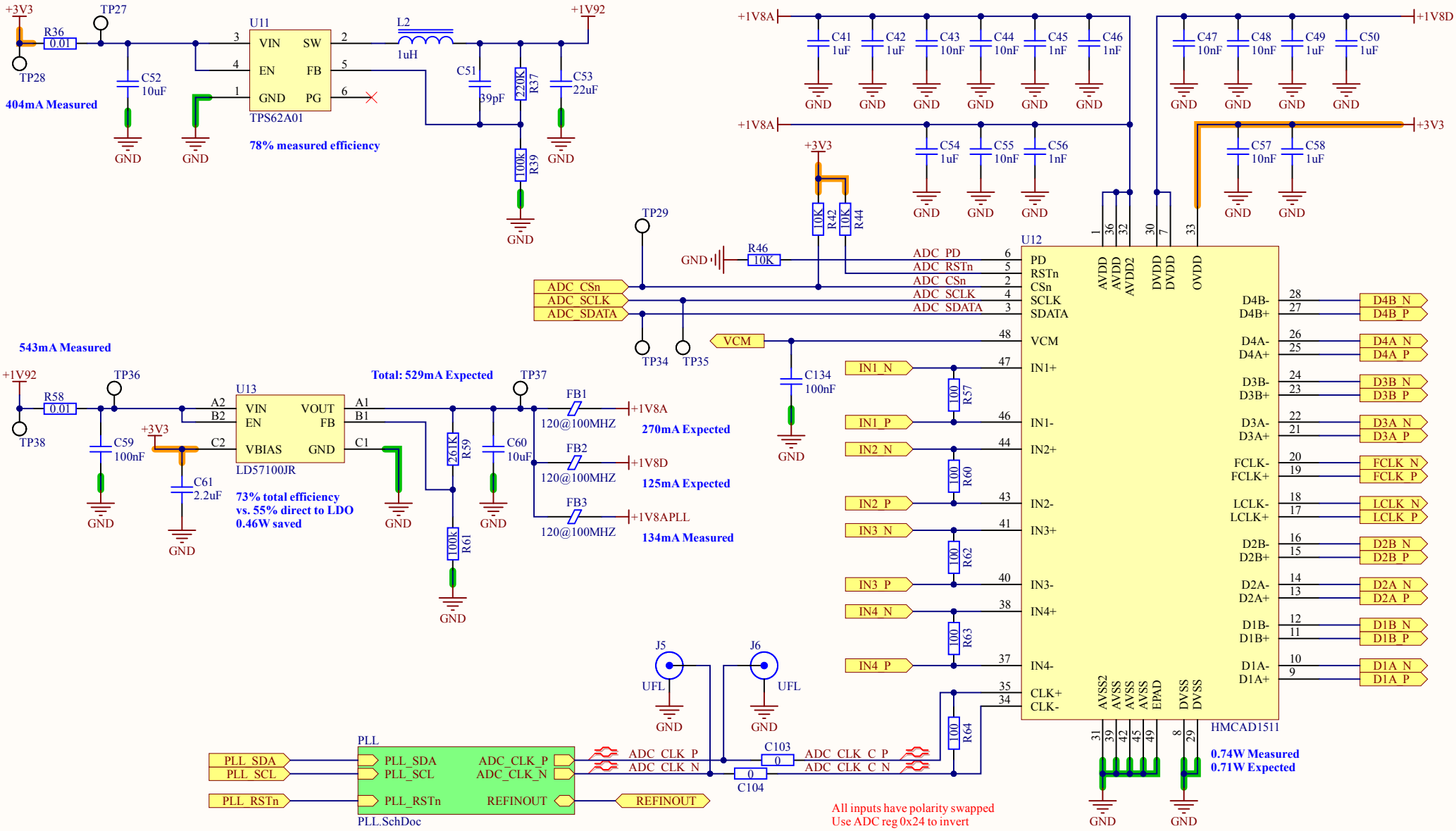
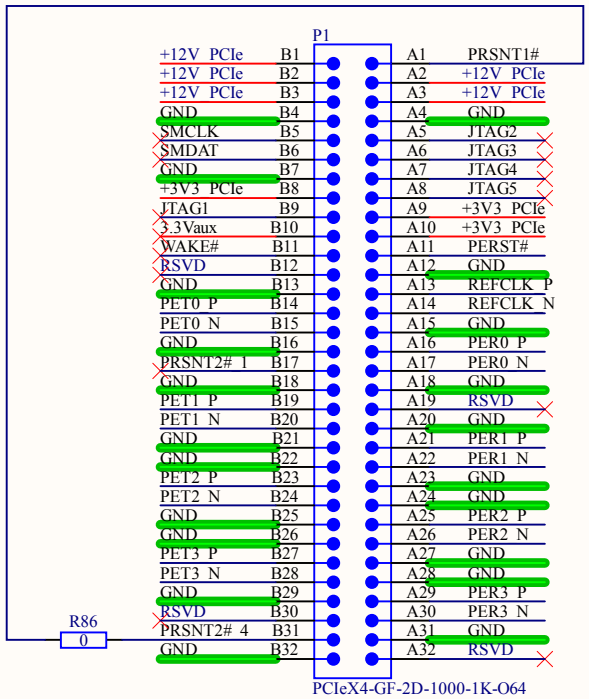
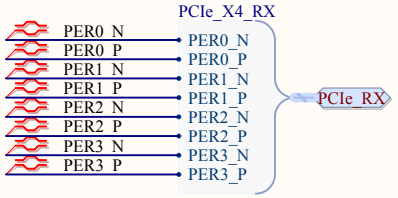
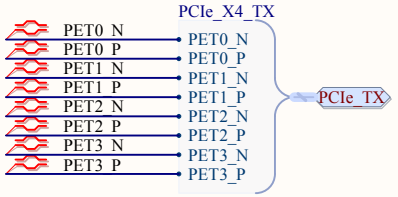
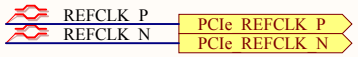

+3V3
TP27
R36
0.01
TP28
404mA Measured
C52
10uF
U11
VIN
SW
EN
FB
GND
PG
TPS62A01
L2
1uH
78% measured efficiency
C51
39pF
220K
R37
100k
R39
+1V92
C53
22uF
GND
543mA Measured
+1V92
TP36
R58
0.01
TP38
C59
100nF
U13
A2
B2
C2
VIN
VOUT
EN
FB
VBIAS
GND
A1
B1
C1
LD57100JR
+3V3
C61
2.2uF
73% total efficiency
vs. 55% direct to LDO
0.46W saved
Total: 529mA Expected
TP37
261K
R59
100k
R61
C60
10uF
FB1
120@100MHZ
+1V8A
270mA Expected
FB2
120@100MHZ
+1V8D
125mA Expected
FB3
120@100MHZ
+1V8APLL
134mA Measured
+1V8A
C41
1uF
C42
1uF
C43
10nF
C44
10nF
C45
1nF
C46
1nF
+1V8D
C47
10nF
C48
10nF
C49
1uF
C50
1uF
C54
1uF
C55
10nF
C56
1nF
C57
10nF
C58
1uF
+3V3
10K
R42
10K
R44
TP29
R46
10K
ADC_CSn
ADC_SCLK
ADC_SDATA
TP34
TP35
VCM
C134
100nF
U12
PD
RSTn
CSn
SCLK
SDATA
VCM
IN1+
IN1-
IN2+
IN2-
IN3+
IN3-
IN4+
IN4-
CLK+
CLK-
AVDD
AVDD
AVDD2
DVDD
DVDD
OVDD
AVSS2
AVSS
AVSS
AVSS
EPAD
DVSS
DVSS
D4B-
D4B+
D4A-
D4A+
D3B-
D3B+
D3A-
D3A+
FCLK-
FCLK+
LCLK-
LCLK+
D2B-
D2B+
D2A-
D2A+
D1B-
D1B+
D1A-
D1A+
HMCAD1511
0.74W Measured
0.71W Expected
IN1_N
IN1_P
IN2_N
IN2_P
IN3_N
IN3_P
IN4_N
IN4_P
100
R57
100
R60
100
R62
100
R63
100
R64
D4B_N
D4B_P
D4A_N
D4A_P
D3B_N
D3B_P
D3A_N
D3A_P
FCLK_N
FCLK_P
LCLK_N
LCLK_P
D2B_N
D2B_P
D2A_N
D2A_P
D1B_N
D1B_P
D1A_N
D1A_P
J5
UFL
J6
UFL
PLL
PLL_SDA
PLL_SCL
PLL_RSTn
ADC_CLK_P
ADC_CLK_N
REFINOUT
PLL.SchDoc
C103
0
C104
0
ADC_CLK_C_P
ADC_CLK_C_N
All inputs have polarity swapped
Use ADC reg 0x24 to invert
Title
ThunderScope 1000E
Size
A4
Number
ADC.SchDoc
Revision
1
Date:
3/08/2025
Sheet of
File:
Y:\器件资料\..\ADC.SchDoc
Drawn By:
Aleksa Bjelogrlic

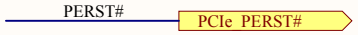
- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

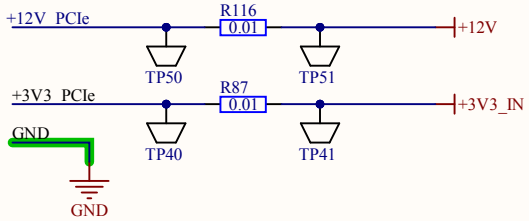












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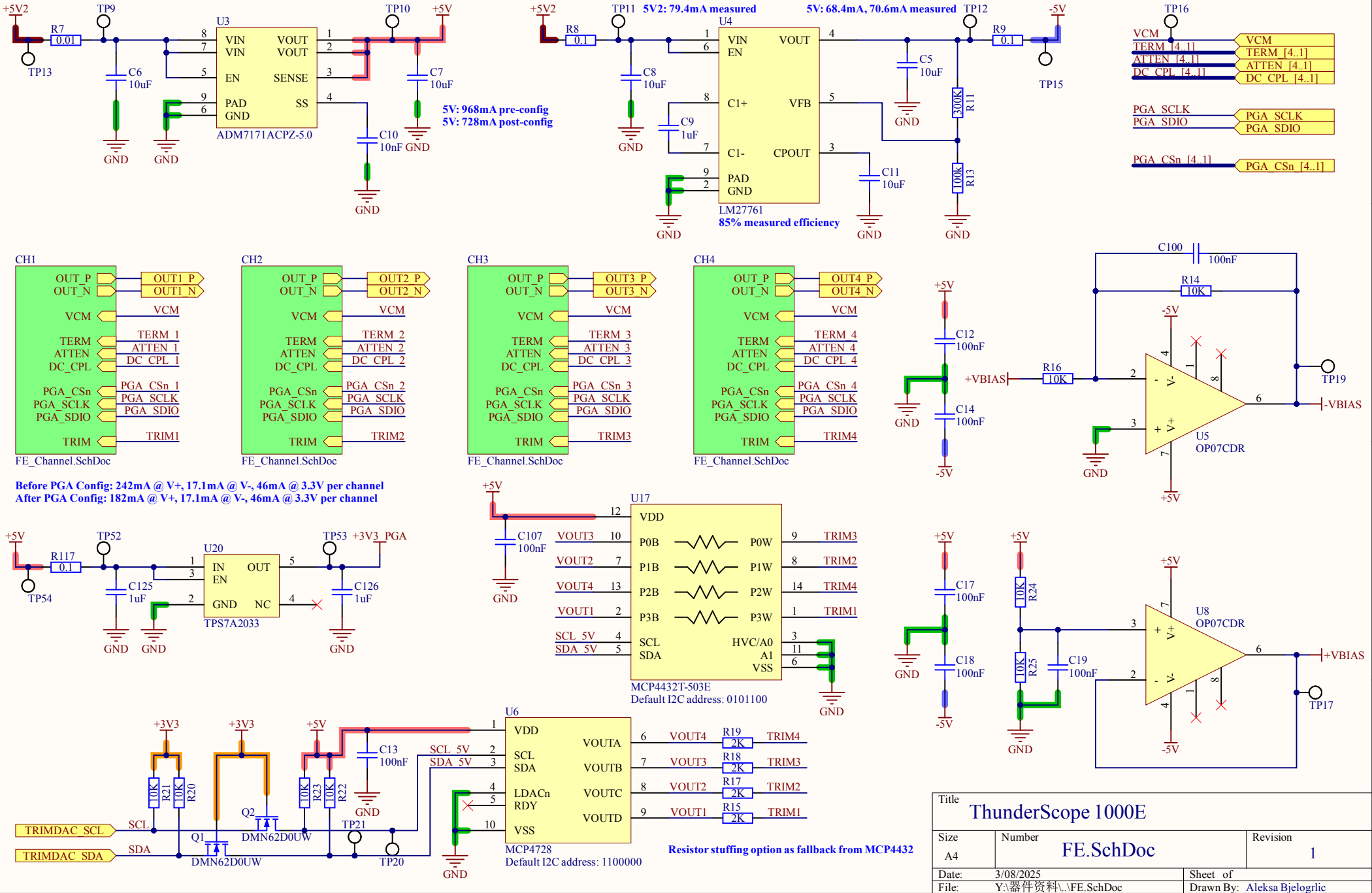
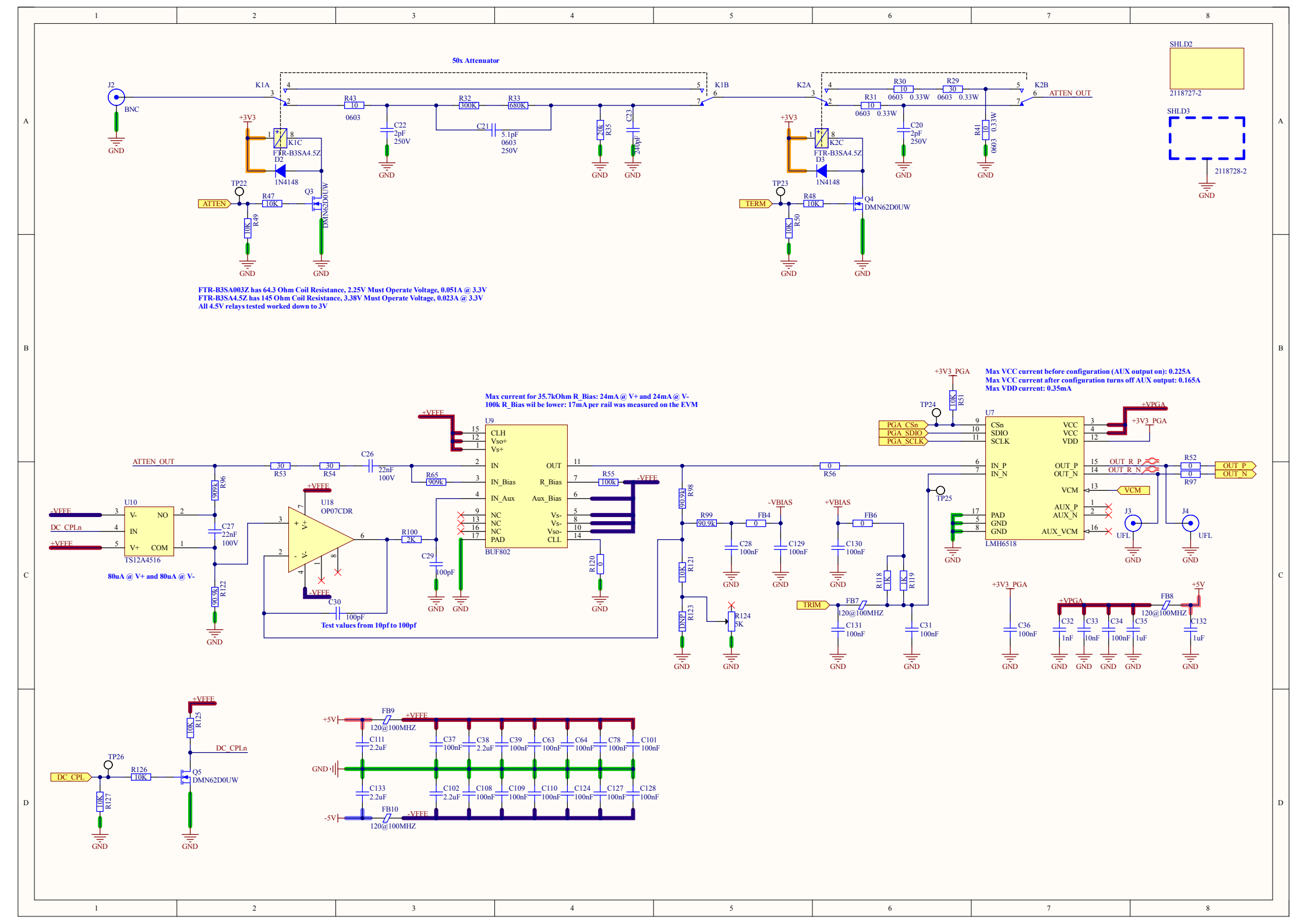
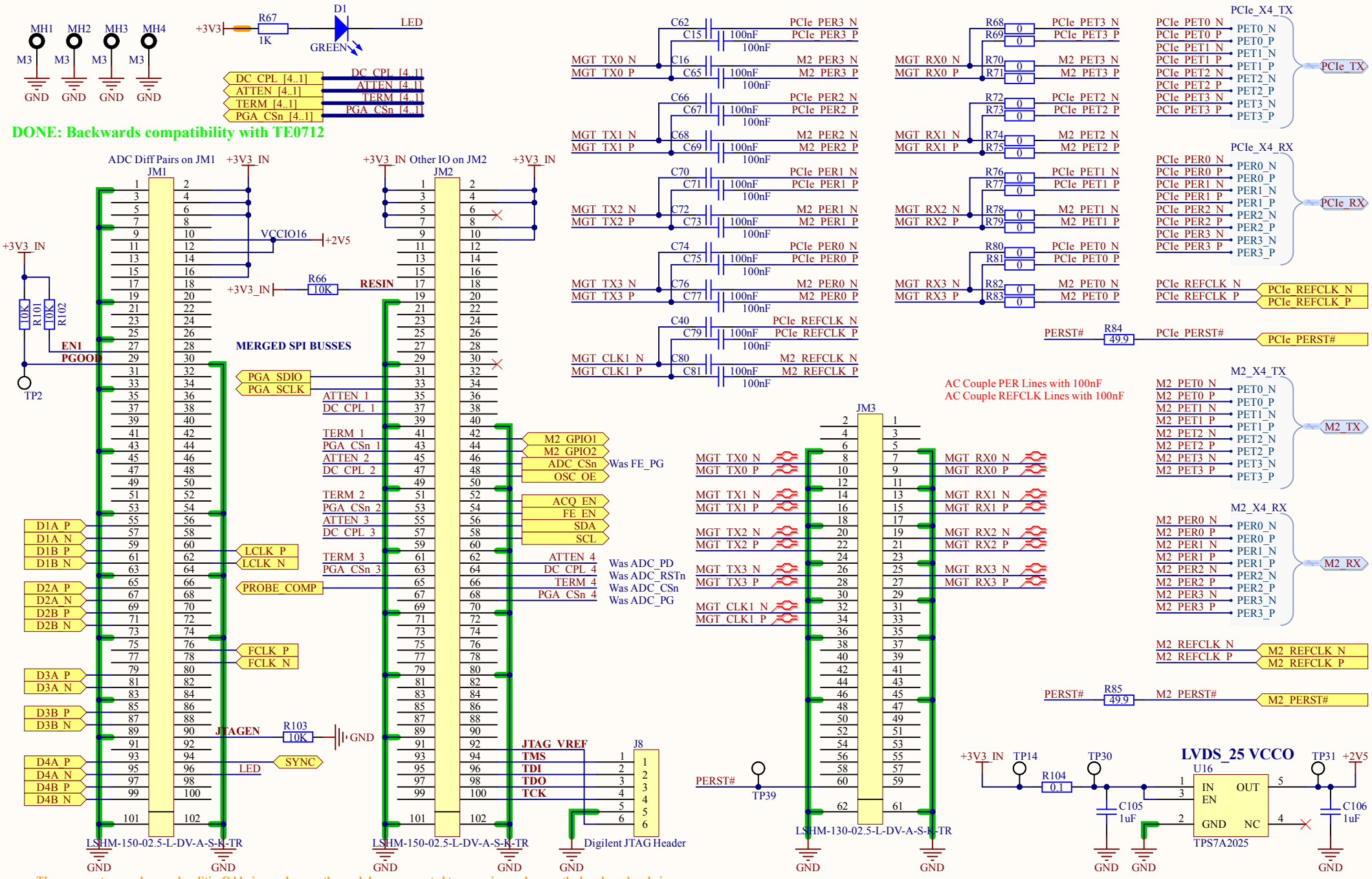
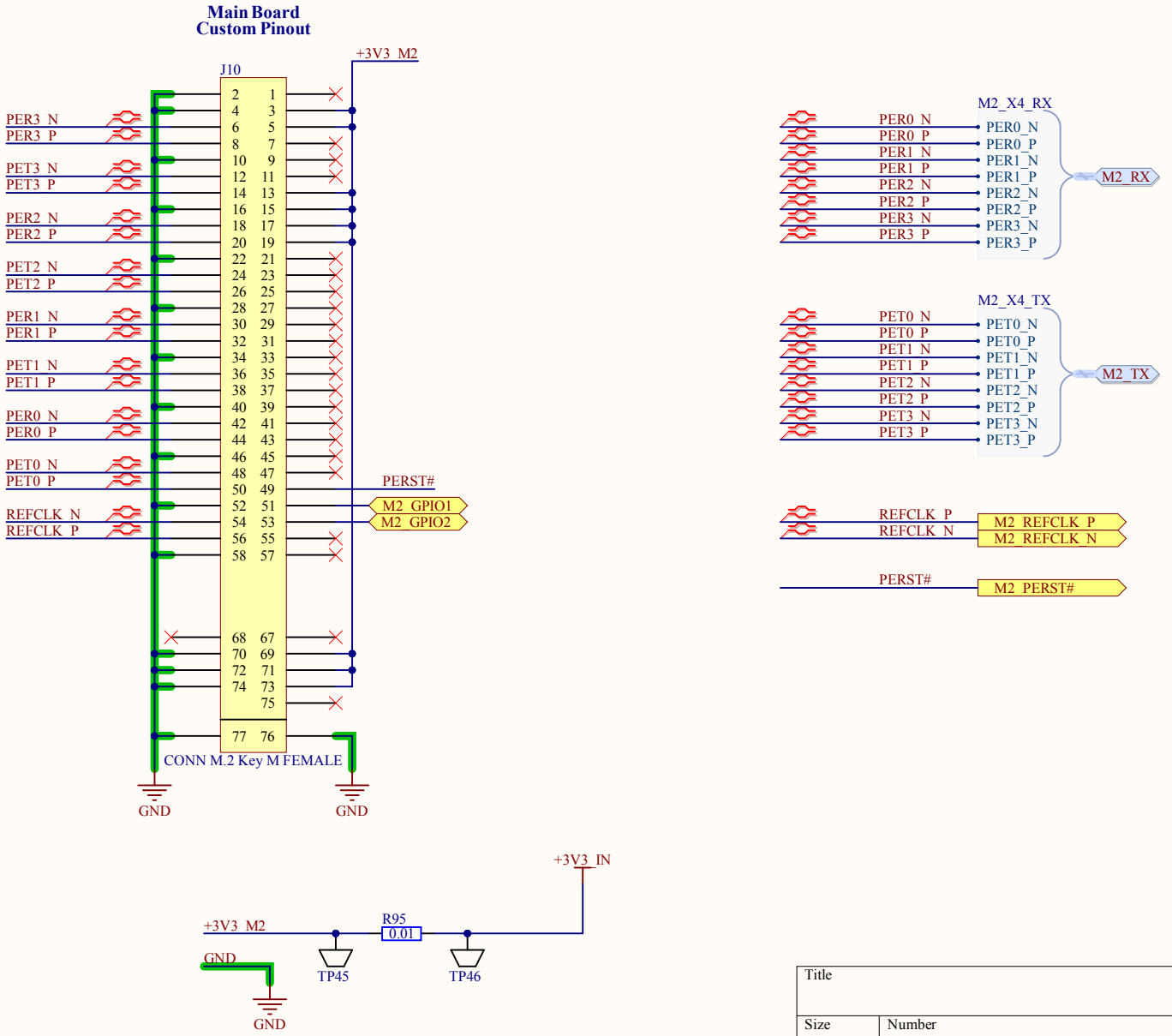
Size: A4	Number:*	Revision:1	
Date: 2025/3/8	Time: 22:36:49	Sheet * of *	
File: Y:\器件资料\oscilloscope\ThunderScope-master\Hardware\Altium\Thunderscope_Rev4.1\Managed\Sheets\FC1D1A13-1D8			


+5V2
TP9
R7
0.01
TP13
C6
10uF
U3
VIN
VIN
EN
PAD
GND
VOUT
VOUT
SENSE
SS
ADM7171ACPZ-5.0
TP10
+5V
C7
10uF
C10
10nF
5V: 968mA pre-config
5V: 728mA post-config
TP11
5V2: 79.4mA measured
5V: 68.4mA, 70.6mA measured
TP12
-5V
R8
0.1
R9
0.1
TP15
C8
10uF
C9
1uF
U4
VIN
EN
C1+
C1-
PAD
GND
VOUT
VFB
CPOUT
LM27761
85% measured efficiency
C5
10uF
300K
R11
100k
R13
C11
10uF
TP16
VCM
TERM [4..1]
ATTEN [4..1]
DC_CPL [4..1]
PGA_SCLK
PGA_SDIO
PGA_CSn [4..1]
CH1
CH2
CH3
CH4
OUT_P
OUT_N
OUT1_P
OUT1_N
OUT2_P
OUT2_N
OUT3_P
OUT3_N
OUT4_P
OUT4_N
VCM
TERM
ATTEN
DC_CPL
PGA_CSn
PGA_SCLK
PGA_SDIO
TRIM
TERM_1
ATTEN_1
DC_CPL_1
PGA_CSn_1
PGA_SCLK
PGA_SDIO
TRIM1
TERM_2
ATTEN_2
DC_CPL_2
PGA_CSn_2
PGA_SCLK
PGA_SDIO
TRIM2
TERM_3
ATTEN_3
DC_CPL_3
PGA_CSn_3
PGA_SCLK
PGA_SDIO
TRIM3
TERM_4
ATTEN_4
DC_CPL_4
PGA_CSn_4
PGA_SCLK
PGA_SDIO
TRIM4
FE_Channel.SchDoc
Before PGA Config: 242mA @ V+, 17.1mA @ V-, 46mA @ 3.3V per channel
After PGA Config: 182mA @ V+, 17.1mA @ V-, 46mA @ 3.3V per channel
C12
100nF
C14
100nF
+VBIAS
R16
10K
C100
100nF
R14
10K
U5
OP07CDR
TP19
-VBIAS
+5V
-5V
GND
R117
0.1
TP54
TP52
C125
1uF
U20
IN
EN
GND
OUT
NC
TPS7A2033
TP53
+3V3_PGA
C126
1uF
U17
VDD
P0B
P1B
P2B
P3B
SCL
SDA
P0W
P1W
P2W
P3W
HVC/A0
A1
VSS
MCP4432T-503E
Default I2C address: 0101100
C107
100nF
VOUT3
VOUT2
VOUT4
VOUT1
SCL_5V
SDA_5V
TRIM3
TRIM2
TRIM4
TRIM1
C17
100nF
C18
100nF
10K
R24
10K
R25
C19
100nF
U8
OP07CDR
TP17
+VBIAS
+3V3
10K
R21
10K
R20
10K
R23
10K
R22
C13
100nF
Q2
Q1
DMN62D0UW
DMN62D0UW
TRIMDAC_SCL
TRIMDAC_SDA
SCL
SDA
TP21
TP20
U6
VDD
SCL
SDA
LDACn
RDY
VSS
VOUTA
VOUTB
VOUTC
VOUTD
MCP4728
Default I2C address: 1100000
R19
2K
R18
2K
R17
2K
R15
2K
Resistor stuffing option as fallback from MCP4432
Title
ThunderScope 1000E
Size
A4
Number
FE.SchDoc
Revision
1
Date:
3/08/2025
Sheet of
File:
Y:\器件资料\..\FE.SchDoc
Drawn By:
Aleksa Bjelogrlic


50x Attenuator
J2
BNC
GND
K1A
K1B
K2A
K2B
ATTEN_OUT
R43
10
0603
C22
2pF
250V
R32
300K
R33
680K
C21
5.1pF
0603
250V
R35
20k
C23
240pF
R30
10
0603 0.33W
R29
30
0603 0.33W
R31
10
0603 0.33W
C20
2pF
250V
R41
10
0603 0.33W
+3V3
K1C
FTR-B3SA4.5Z
D2
1N4148
K2C
D3
TP22
ATTEN
R47
10K
Q3
DMN62D0UW
R49
10K
TP23
TERM
R48
10K
Q4
R50
SHLD2
2118727-2
SHLD3
2118728-2
FTR-B3SA003Z has 64.3 Ohm Coil Resistance, 2.25V Must Operate Voltage, 0.051A @ 3.3V
FTR-B3SA4.5Z has 145 Ohm Coil Resistance, 3.38V Must Operate Voltage, 0.023A @ 3.3V
All 4.5V relays tested worked down to 3V
Max current for 35.7kOhm R_Bias: 24mA @ V+ and 24mA @ V-
100k R_Bias wil be lower: 17mA per rail was measured on the EVM
U9
BUF802
CLH
Vso+
Vs+
IN
IN_Bias
IN_Aux
OUT
R_Bias
Aux_Bias
NC
Vs-
Vso-
CLL
PAD
+VEFE
-VEFE
ATTEN_OUT
R53
30
R54
30
C26
22nF
100V
R65
909k
R55
100k
R56
0
U10
TS12A4516
V-
NO
IN
V+
COM
DC_CPLn
+VEFE
-VEFE
R96
909k
C27
22nF
100V
R122
90.9k
80uA @ V+ and 80uA @ V-
U18
OP07CDR
R100
2K
C29
100pF
C30
100pF
Test values from 10pf to 100pf
R98
90.9k
R99
90.9k
FB4
0
C28
100nF
C129
100nF
-VBIAS
+VBIAS
FB6
0
C130
100nF
C131
100nF
R118
1K
R119
1K
FB7
120@100MHZ
C31
100nF
TRIM
R121
10K
DNP
R123
R124
5K
R120
0
+3V3_PGA
TP24
R51
10K
PGA_CSn
PGA_SDIO
PGA_SCLK
U7
LMH6518
CSn
SDIO
SCLK
IN_P
IN_N
PAD
GND
VCC
VDD
OUT_P
OUT_N
VCM
AUX_P
AUX_N
AUX_VCM
+VPGA
TP25
R52
0
R97
0
OUT_P
OUT_N
J3
J4
UFL
Max VCC current before configuration (AUX output on): 0.225A
Max VCC current after configuration turns off AUX output: 0.165A
Max VDD current: 0.35mA
C36
100nF
C32
1nF
C33
10nF
C34
100nF
C35
1uF
FB8
120@100MHZ
C132
1uF
+5V
TP26
DC_CPL
R126
10K
Q5
DMN62D0UW
R125
10K
R127
10K
FB9
120@100MHZ
FB10
120@100MHZ
-5V
C111
2.2uF
C133
2.2uF
C37
100nF
C38
2.2uF
C39
100nF
C63
100nF
C64
100nF
C78
100nF
C101
100nF
C102
2.2uF
C108
100nF
C109
100nF
C110
100nF
C124
100nF
C127
100nF
C128
100nF


MH1 MH2 MH3 MH4
M3 M3 M3 M3
GND GND GND GND
+3V3
R67
1K
D1
LED
GREEN
DC_CPL [4..1]
ATTEN [4..1]
TERM [4..1]
PGA_CSn [4..1]
DONE: Backwards compatibility with TE0712
ADC Diff Pairs on JM1
+3V3_IN
JM1
+3V3_IN Other IO on JM2
JM2
VCCIO16
+2V5
R66
10K
RESIN
+3V3_IN
10K
R101
10K
R102
EN1
PGOOD
TP2
MERGED SPI BUSSES
PGA_SDIO
PGA_SCLK
ATTEN_1
DC_CPL_1
TERM_1
PGA_CSn_1
ATTEN_2
DC_CPL_2
TERM_2
PGA_CSn_2
ATTEN_3
DC_CPL_3
TERM_3
PGA_CSn_3
M2_GPIO1
M2_GPIO2
ADC_CSn
OSC_OE
Was FE_PG
ACQ_EN
FE_EN
SDA
SCL
ATTEN_4
DC_CPL_4
TERM_4
PGA_CSn_4
Was ADC_PD
Was ADC_RSTn
Was ADC_CSn
Was ADC_PG
D1A_P
D1A_N
D1B_P
D1B_N
LCLK_P
LCLK_N
D2A_P
D2A_N
D2B_P
D2B_N
PROBE_COMP
FCLK_P
FCLK_N
D3A_P
D3A_N
D3B_P
D3B_N
JTAGEN
R103
10K
GND
SYNC
LED
D4A_P
D4A_N
D4B_P
D4B_N
JTAG_VREF
TMS
TDI
TDO
TCK
J8
Digilent JTAG Header
LSHM-150-02.5-L-DV-A-S-K-TR
LSHM-150-02.5-L-DV-A-S-K-TR
C62 C15 100nF PCIe_PER3_N PCIe_PER3_P
C16 C65 100nF M2_PER3_N M2_PER3_P
C66 C67 100nF PCIe_PER2_N PCIe_PER2_P
C68 C69 100nF M2_PER2_N M2_PER2_P
C70 C71 100nF PCIe_PER1_N PCIe_PER1_P
C72 C73 100nF M2_PER1_N M2_PER1_P
C74 C75 100nF PCIe_PER0_N PCIe_PER0_P
C76 C77 100nF M2_PER0_N M2_PER0_P
C40 C79 100nF PCIe_REFCLK_N PCIe_REFCLK_P
C80 C81 100nF M2_REFCLK_N M2_REFCLK_P
MGT_TX0_N
MGT_TX0_P
MGT_TX1_N
MGT_TX1_P
MGT_TX2_N
MGT_TX2_P
MGT_TX3_N
MGT_TX3_P
MGT_CLK1_N
MGT_CLK1_P
R68 R69 PCIe_PET3_N PCIe_PET3_P
R70 R71 M2_PET3_N M2_PET3_P
R72 R73 PCIe_PET2_N PCIe_PET2_P
R74 R75 M2_PET2_N M2_PET2_P
R76 R77 PCIe_PET1_N PCIe_PET1_P
R78 R79 M2_PET1_N M2_PET1_P
R80 R81 PCIe_PET0_N PCIe_PET0_P
R82 R83 M2_PET0_N M2_PET0_P
MGT_RX0_N
MGT_RX0_P
MGT_RX1_N
MGT_RX1_P
MGT_RX2_N
MGT_RX2_P
MGT_RX3_N
MGT_RX3_P
PCIe_X4_TX
PCIe_PET0_N
PCIe_PET0_P
PCIe_PET1_N
PCIe_PET1_P
PCIe_PET2_N
PCIe_PET2_P
PCIe_PET3_N
PCIe_PET3_P
PET0_N
PET0_P
PET1_N
PET1_P
PET2_N
PET2_P
PET3_N
PET3_P
PCIe_TX
PCIe_X4_RX
PCIe_PER0_N
PCIe_PER0_P
PCIe_PER1_N
PCIe_PER1_P
PCIe_PER2_N
PCIe_PER2_P
PCIe_PER3_N
PCIe_PER3_P
PER0_N
PER0_P
PER1_N
PER1_P
PER2_N
PER2_P
PER3_N
PER3_P
PCIe_RX
PCIe_REFCLK_N
PCIe_REFCLK_P
PERST#
R84
49.9
PCIe_PERST#
AC Couple PER Lines with 100nF
AC Couple REFCLK Lines with 100nF
M2_X4_TX
M2_PET0_N
M2_PET0_P
M2_PET1_N
M2_PET1_P
M2_PET2_N
M2_PET2_P
M2_PET3_N
M2_PET3_P
M2_TX
M2_X4_RX
M2_PER0_N
M2_PER0_P
M2_PER1_N
M2_PER1_P
M2_PER2_N
M2_PER2_P
M2_PER3_N
M2_PER3_P
M2_RX
M2_REFCLK_N
M2_REFCLK_P
R85
49.9
M2_PERST#
JM3
LSHM-130-02.5-L-DV-A-S-K-TR
PERST#
TP39
+3V3_IN
TP14
R104
0.1
TP30
LVDS_25 VCCO
U16
IN
EN
GND
OUT
NC
TPS7A2025
C105
1uF
C106
1uF
TP31
+2V5
These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.



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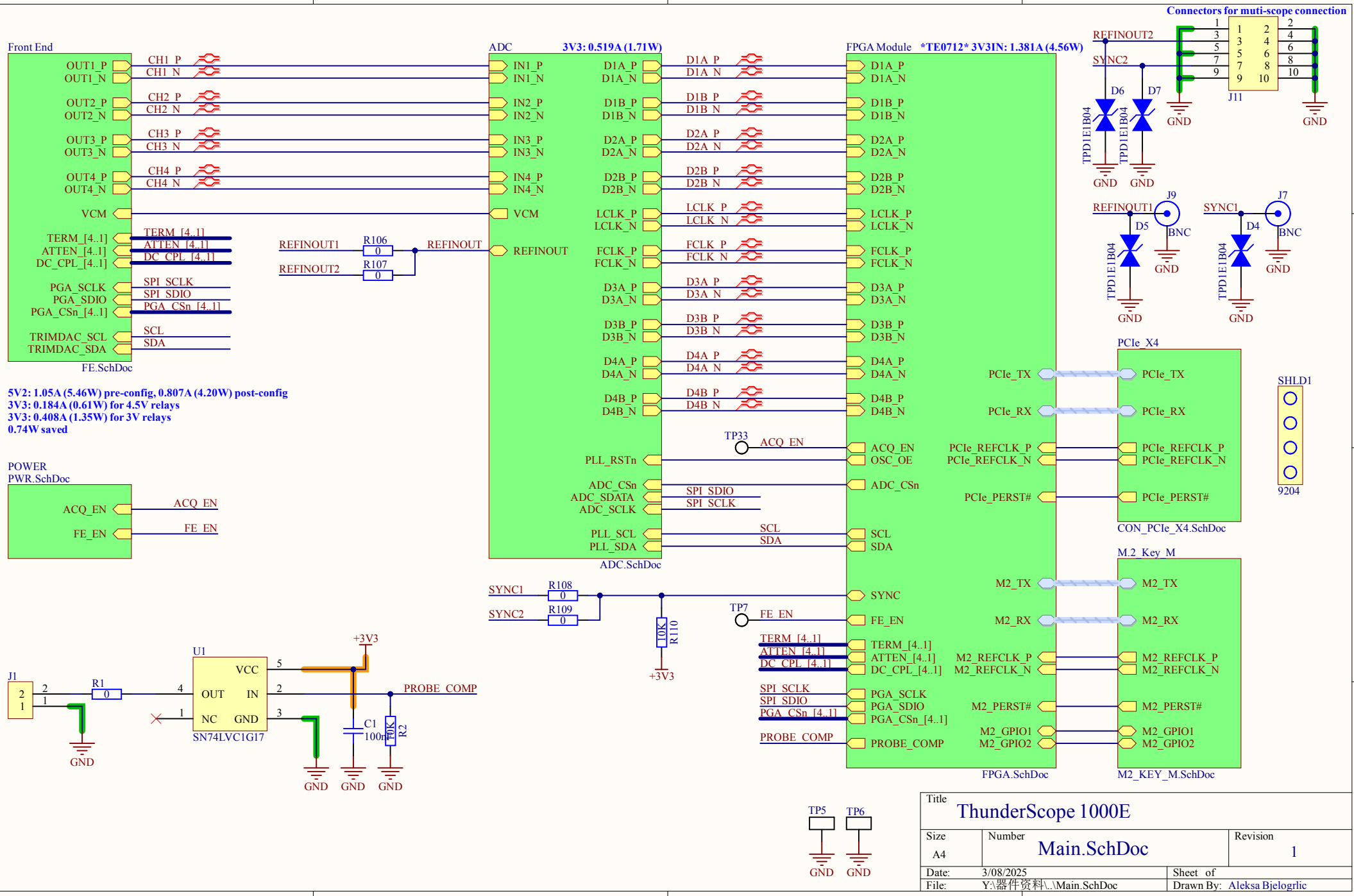
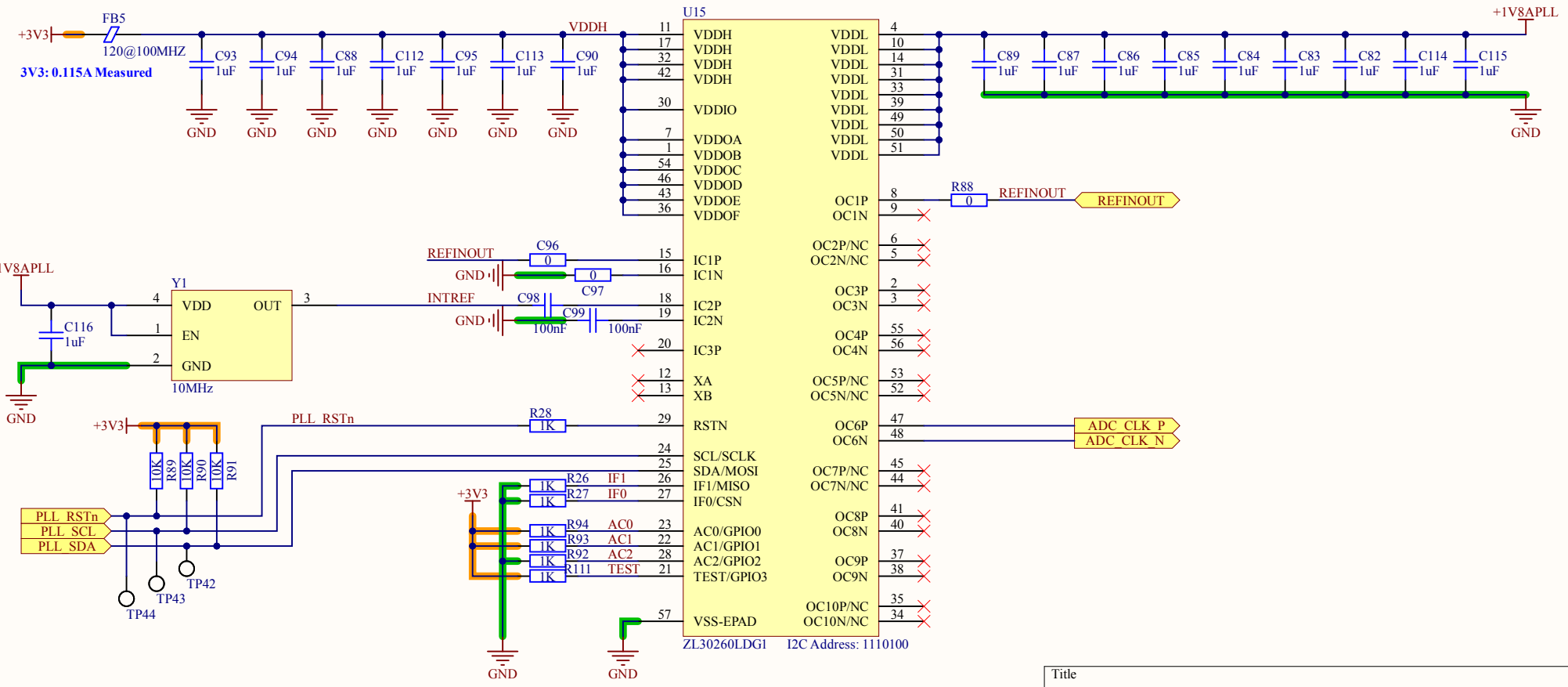
Size: A4	Number	Revision
Date: 3/08/2025		Sheet of
File: Y:\器件资料\..\M2_KEY_M.SchDoc		Drawn By:


Front End
OUT1_P
OUT1_N
OUT2_P
OUT2_N
OUT3_P
OUT3_N
OUT4_P
OUT4_N
VCM
TERM_[4..1]
ATTEN_[4..1]
DC_CPL_[4..1]
SPI_SCLK
SPI_SDIO
PGA_CSn_[4..1]
SCL
SDA
FE.SchDoc
CH1_P
CH1_N
CH2_P
CH2_N
CH3_P
CH3_N
CH4_P
CH4_N
REFINOUT1
REFINOUT2
R106
R107
REFINOUT
ADC
3V3: 0.519A (1.71W)
IN1_P
IN1_N
IN2_P
IN2_N
IN3_P
IN3_N
IN4_P
IN4_N
VCM
REFINOUT
D1A_P
D1A_N
D1B_P
D1B_N
D2A_P
D2A_N
D2B_P
D2B_N
LCLK_P
LCLK_N
FCLK_P
FCLK_N
D3A_P
D3A_N
D3B_P
D3B_N
D4A_P
D4A_N
D4B_P
D4B_N
PLL_RSTn
ADC_CSn
ADC_SDATA
ADC_SCLK
PLL_SCL
PLL_SDA
ADC.SchDoc
FPGA Module
TE0712 3V3IN: 1.381A (4.56W)
FPGA.SchDoc
5V2: 1.05A (5.46W) pre-config, 0.807A (4.20W) post-config
3V3: 0.184A (0.61W) for 4.5V relays
3V3: 0.408A (1.35W) for 3V relays
0.74W saved
POWER
PWR.SchDoc
ACQ_EN
FE_EN
TP33
TP7
SYNC1
SYNC2
R108
R109
SYNC
OSC_OE
SPI_SDIO
SPI_SCLK
SCL
SDA
R110
10K
+3V3
J1
R1
U1
VCC
OUT
IN
NC
GND
SN74LVC1G17
PROBE_COMP
C1
100n
R2
10K
GND
Connectors for muti-scope connection
REFINOUT2
SYNC2
J11
D6
D7
TPD1E1B04
REFINOUT1
SYNC1
J9
J7
D5
D4
BNC
PCIe_X4
PCIe_TX
PCIe_RX
PCIe_REFCLK_P
PCIe_REFCLK_N
PCIe_PERST#
CON_PCIe_X4.SchDoc
SHLD1
9204
M.2_Key_M
M2_TX
M2_RX
M2_REFCLK_P
M2_REFCLK_N
M2_PERST#
M2_GPIO1
M2_GPIO2
M2_KEY_M.SchDoc
TP5
TP6
Title
ThunderScope 1000E
Size
A4
Number
Main.SchDoc
Revision
1
Date:
3/08/2025
Sheet of
File:
Y:\器件资料\..\Main.SchDoc
Drawn By:
Aleksa Bjelogrlic

IF1	IF0	Processor Interface	Configuration Memory to Use
0	0	I^2C, slave address 11101 00	Internal ROM
0	1	I^2C, slave address 11101 01	Internal ROM
1	0	SPI Slave	Internal ROM
1	1	SPI Master during auto-configuration then SPI Slave	External SPI EEPROM

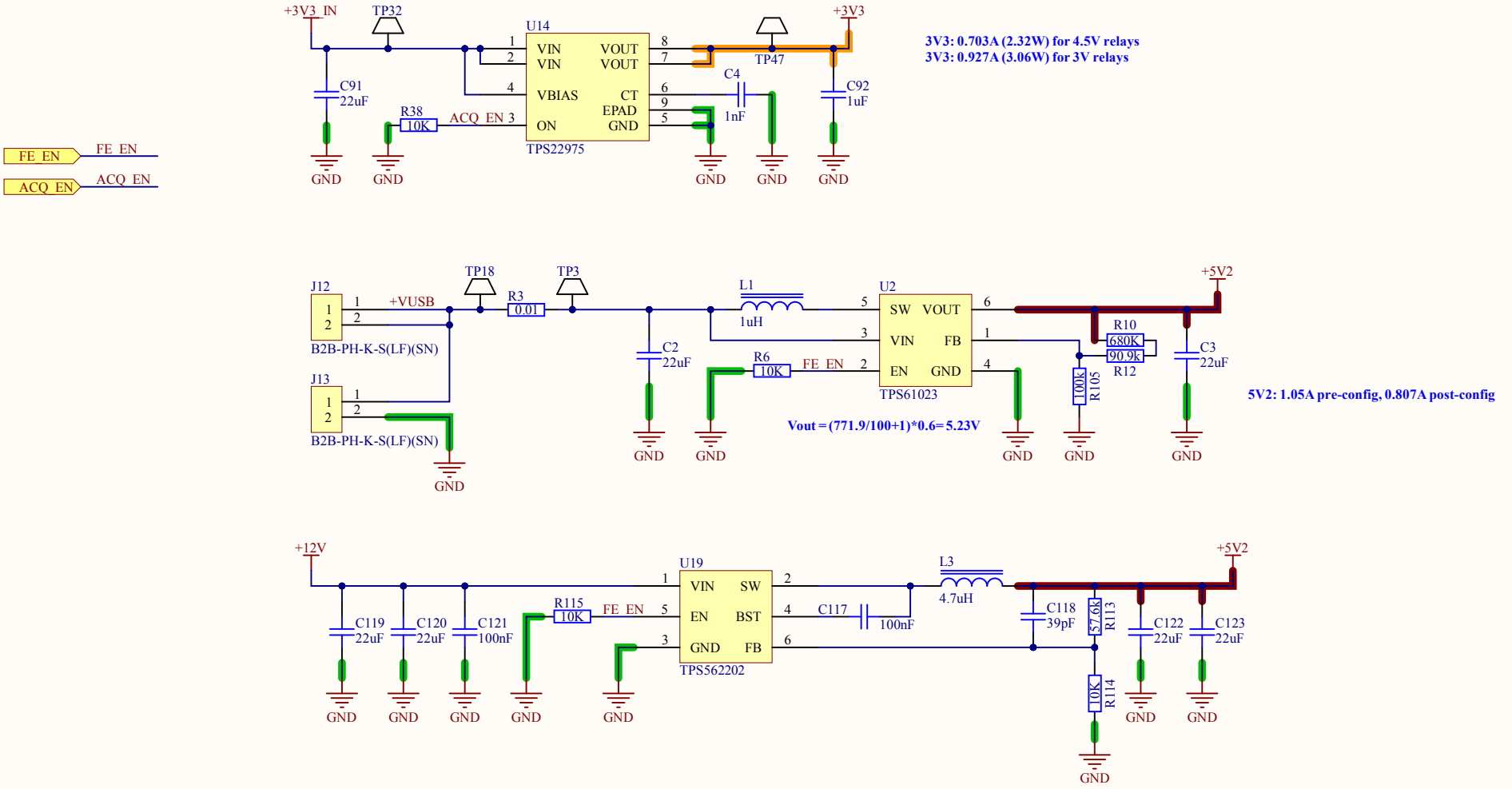
To configure the device as specified in the first three rows above but *without* auto-configuring from internal ROM, wire devices pins as follows: TEST=1 and AC[2:0]=011, as described in section 5.2.

AC2	AC1	AC0	Auto Configuration
0	0	0	Configuration 0
0	0	1	Configuration 1
0	1	0	Configuration 2
0	1	1	Configuration 3
1	0	0	Configuration 4
1	0	1	Configuration 5
1	1	0	Configuration 6
1	1	1	Configuration 7

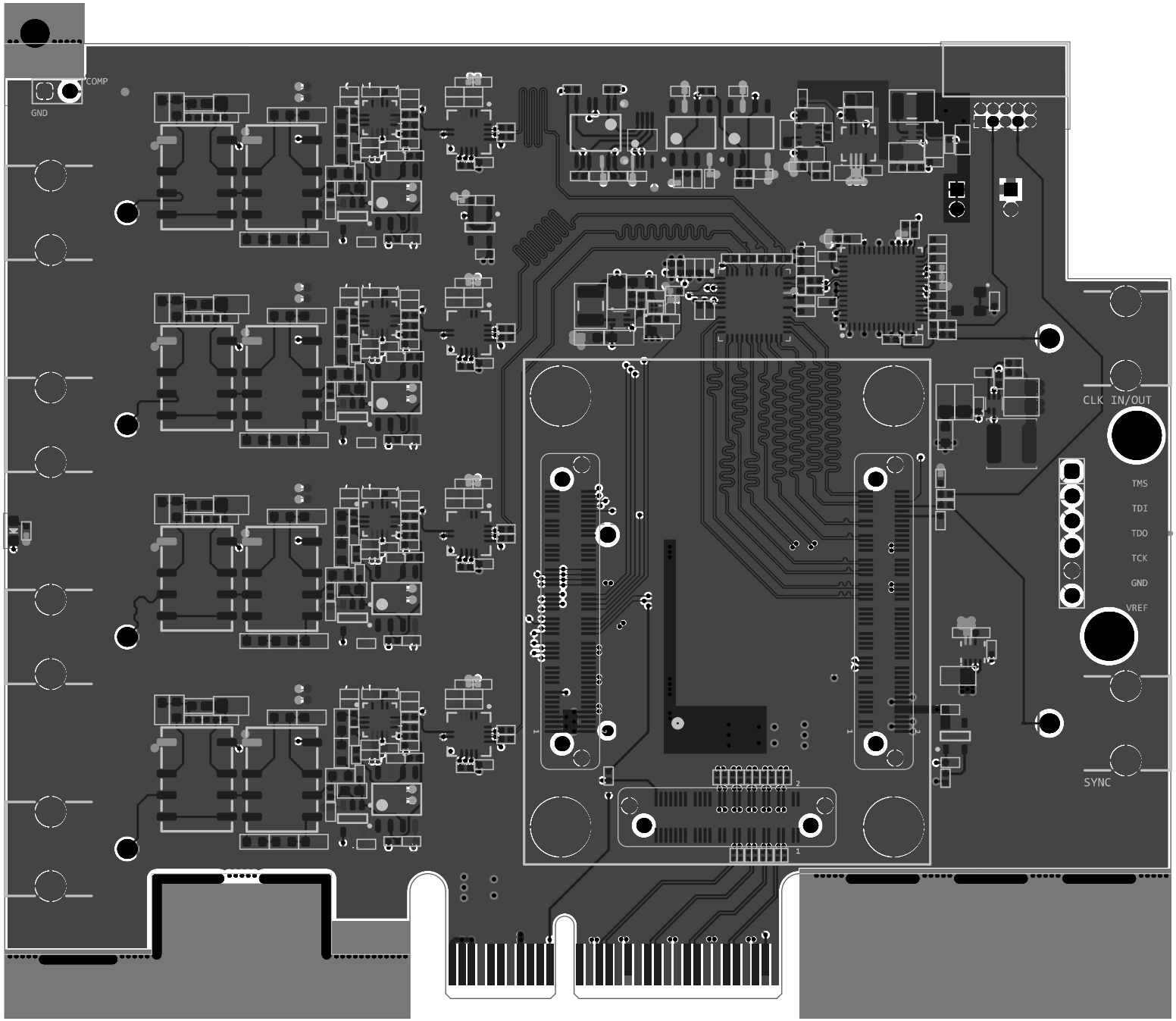


3.3 + 1.8V operation w/ one input one output: 0.67W Expected
0.62W Measured

Title		
Size A4	Number	Revision
Date: 3/08/2025		Sheet of
File: Y:\器件资料\..\PLL.SchDoc		Drawn By:



Title		
Size: A4	Number	Revision
Date: 3/08/2025		Sheet of
File: Y:\器件资料\..\PWR.SchDoc		Drawn By:


COMP
GND
CLK IN/OUT
TMS
TDI
TDO
TCK
GND
VREF
SYNC