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lze4
9/13/23
Lab 03

The screenshots below taken for the lab exercise represent the following. Each number pertains to a screenshot in the order they are shown. Measurements for screenshots 1-5 were taken from an inverter CMOS Circuit. Measurements for screenshots 6-7 were taken from a NAND CMOS Circuit. Measurements for screenshots 8-9 were taken from a NOR CMOS Circuit. Measurements for screenshots 10-11 were taken from an XOR CMOS Circuit. Two zoomed-in screenshots (3a and 3b) are shown at the end. A pulse voltage was applied to each gate in order to simulate a 1 or 0. A DC voltage was also used.

1. The inverter circuit.

2. A voltage versus time graph where the green curve represents the input voltage (Vin) and the blue curve represents the output voltage (Vout).

3. The same graph as screenshot 2, but with a capacitor that varies in value. Each green curve represents a different capacitor value.

4. The same graph as screenshot 2, but with widths of 900nm for both transistors.

5. The same graph as screenshot 2, but with widths of 1800nm for both transistors.

6. The NAND circuit.

7. A voltage versus time graph where the green curve represents the input voltage(Vinputa), the blue curve represents the other input voltage (Vinputb) applied to, and the red curve represents the output voltage V(out).

8. The NOR circuit.

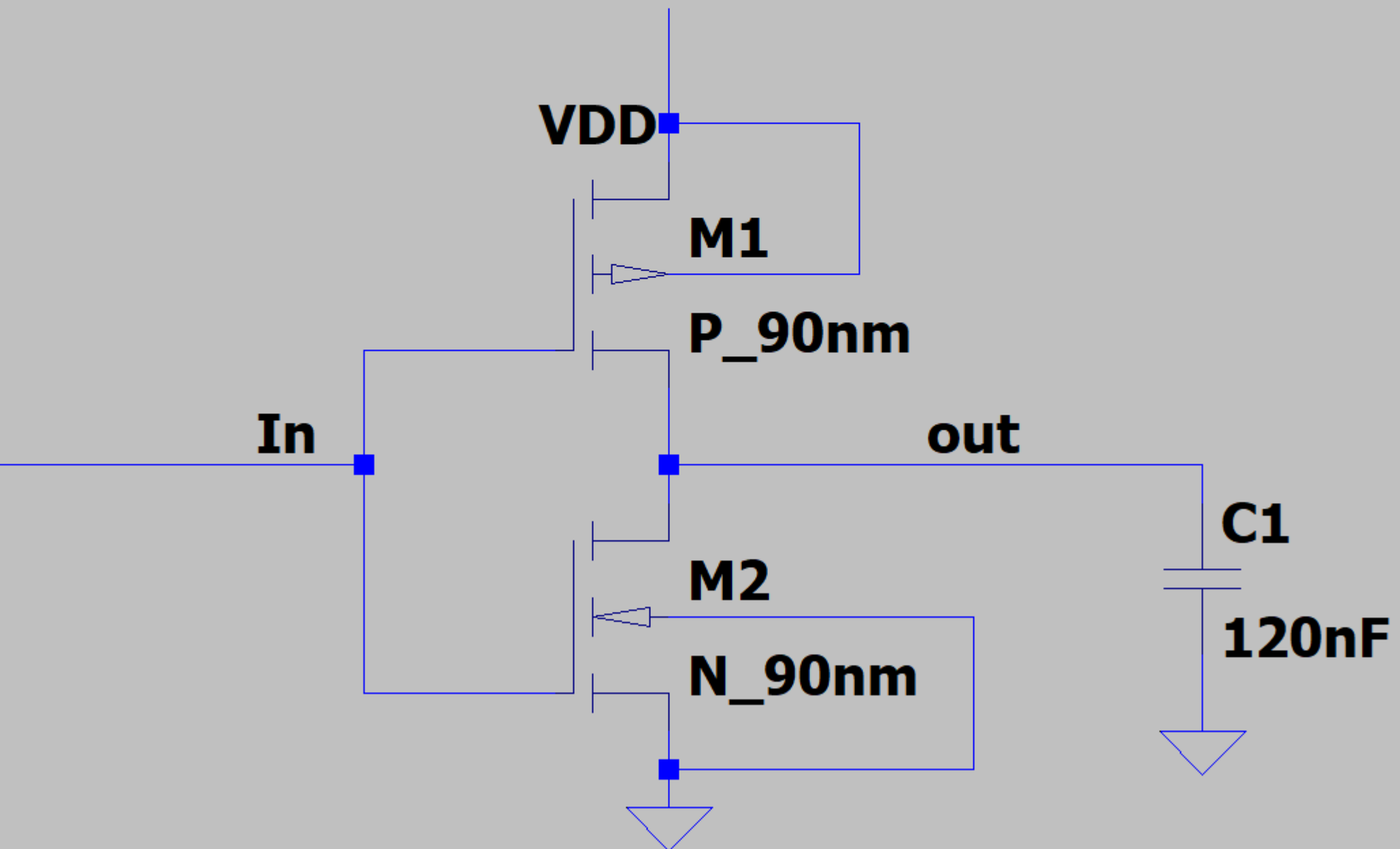
9. A voltage versus time graph where the green curve represents the input voltage(Vinputa), the blue curve represents the other input voltage (Vinputb), and the red curve represents the output voltage V(out).

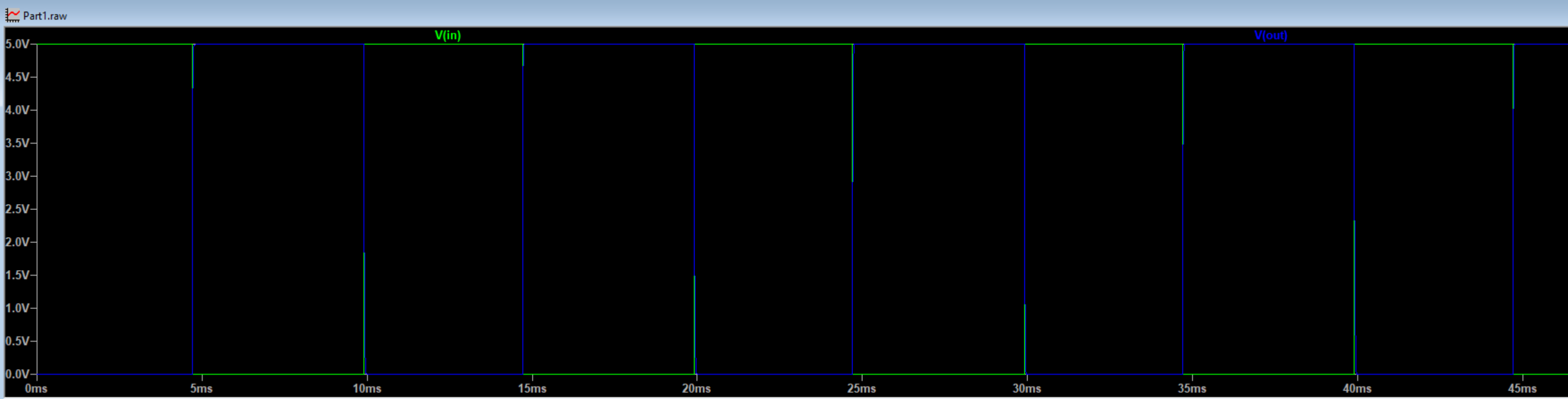
10. The XOR circuit

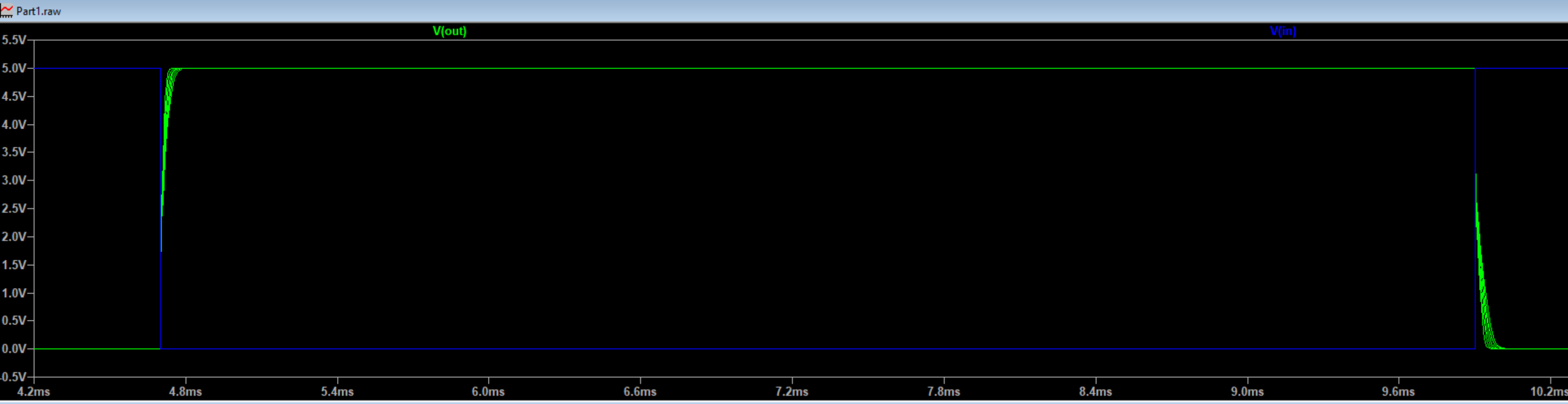
11. A voltage versus time graph where the green curve represents the input voltage(Va), the blue curve represents the other input voltage (Vb), and the red curve represents the output voltage (Vxor).

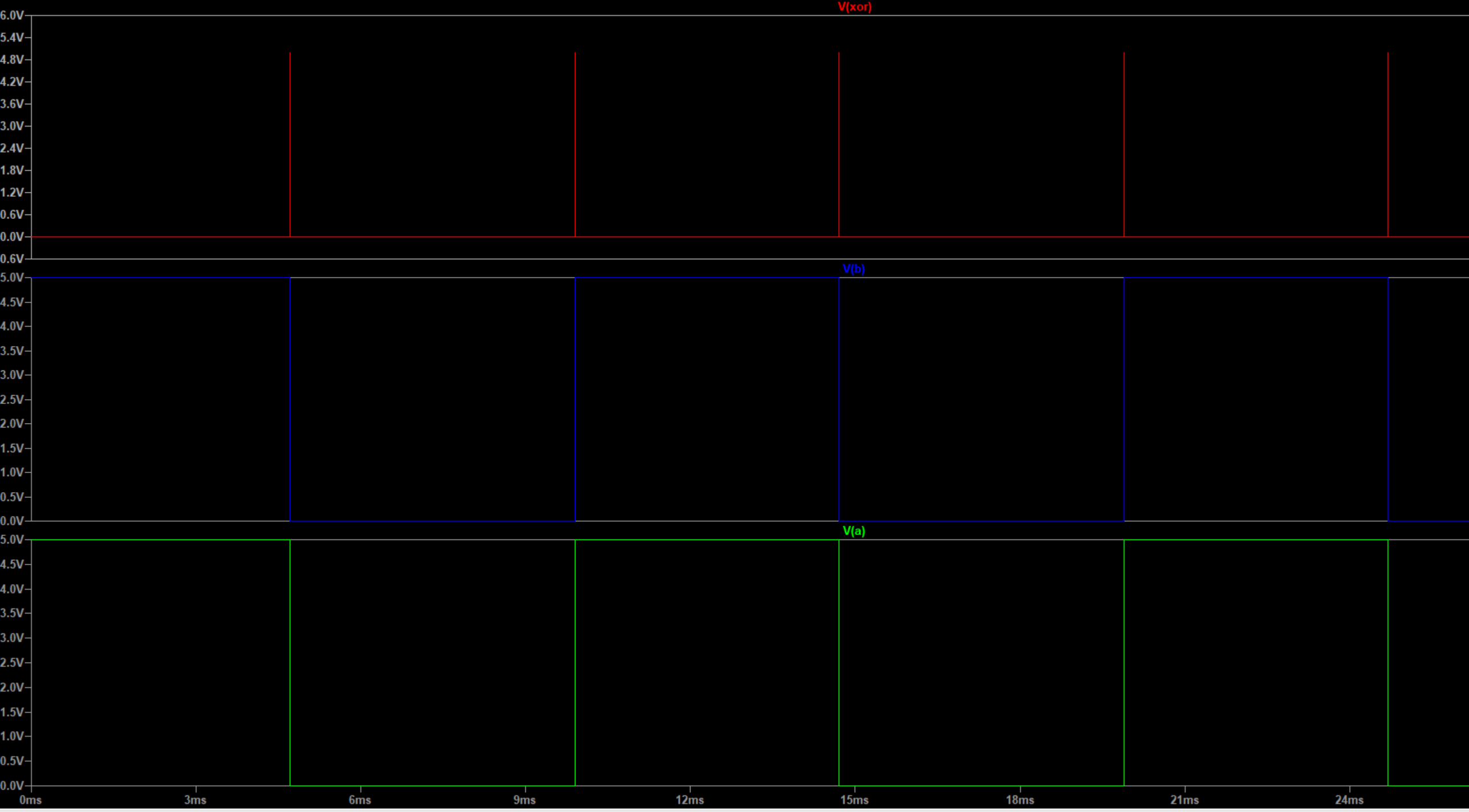
3a. Shows the charing of the varied capacitors from screenshot 3.
3b. Shows the discharing of the varied capacitors from screenshot 3.

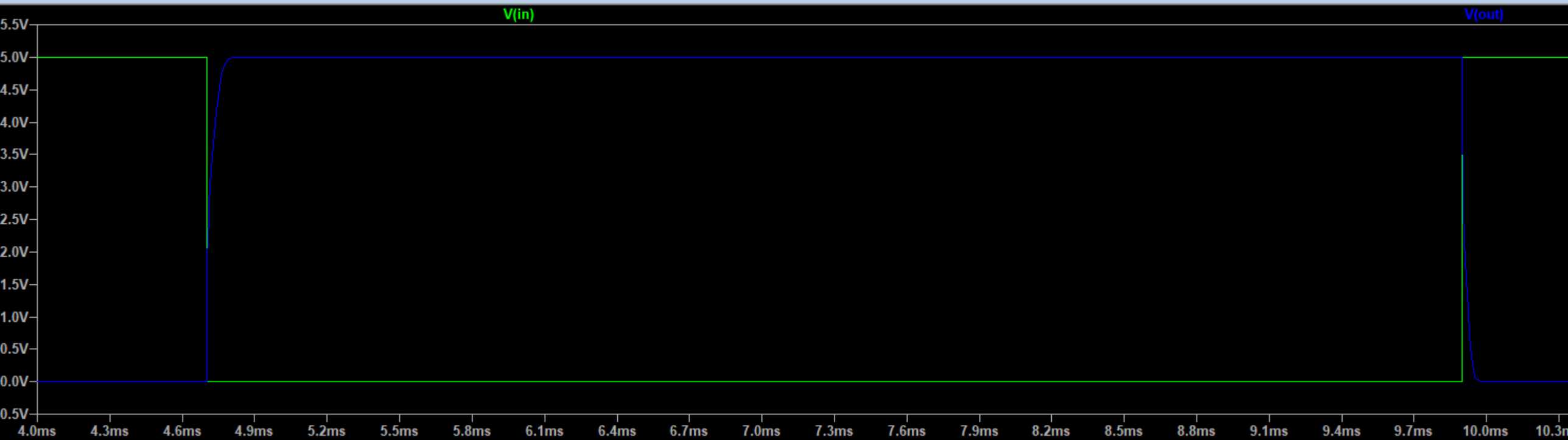
```
.include BSIM_90nm_L4.txt
.tran 0 50m 0.1m
VIn In 0 PULSE(0 5 100n 100n 100n 4.8m 10m 5)
VDD VDD 0 dc 5
```

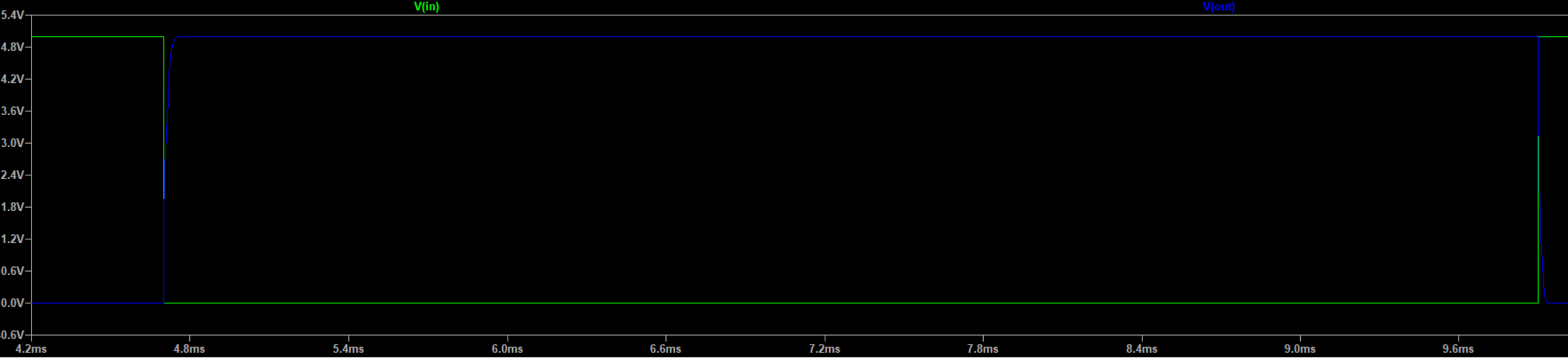


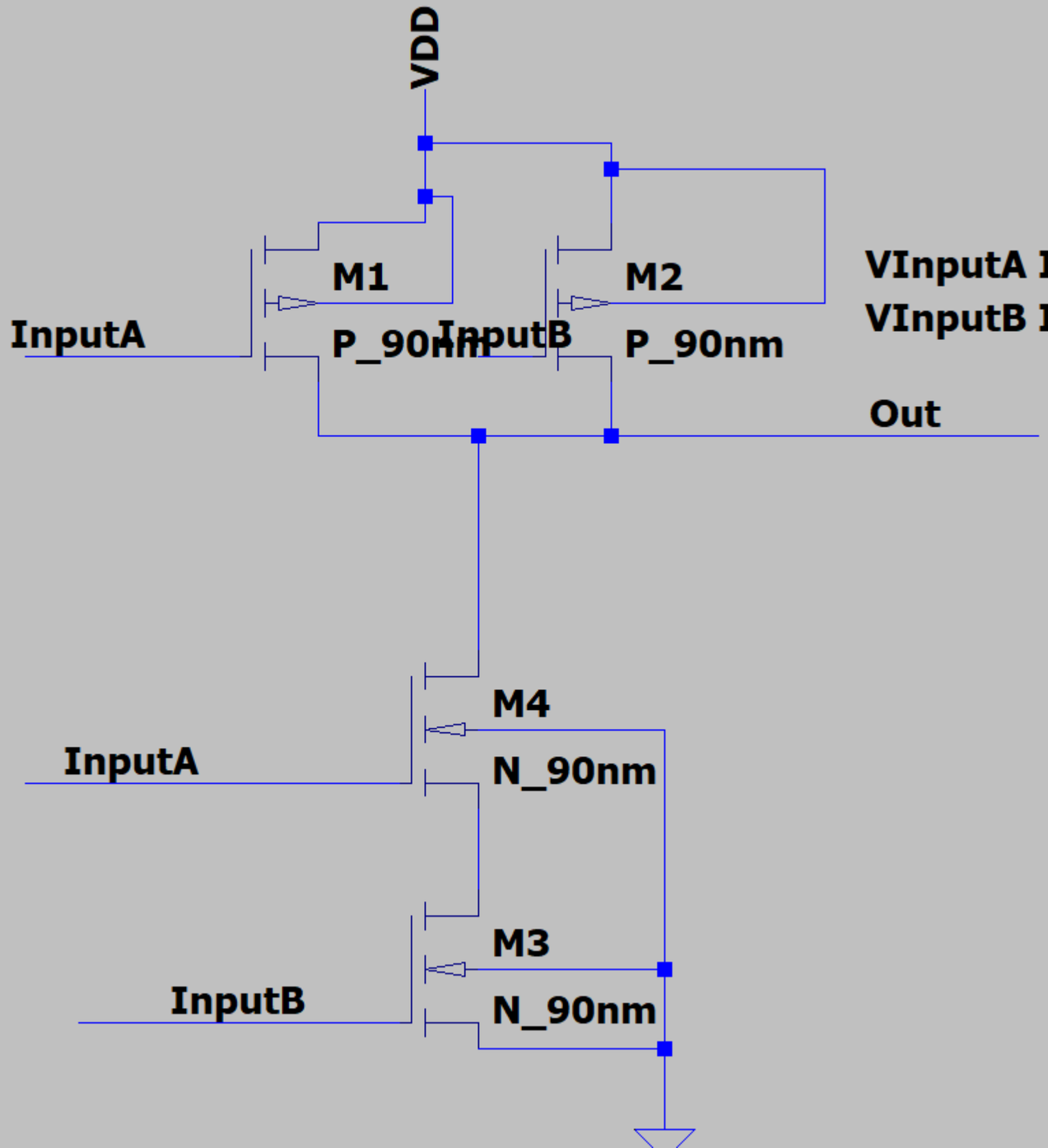

Part1.raw
V(in)
V(out)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms


Part1.raw
V(out)
V(in)
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
4.2ms
4.8ms
5.4ms
6.0ms
6.6ms
7.2ms
7.8ms
8.4ms
9.0ms
9.6ms
10.2ms

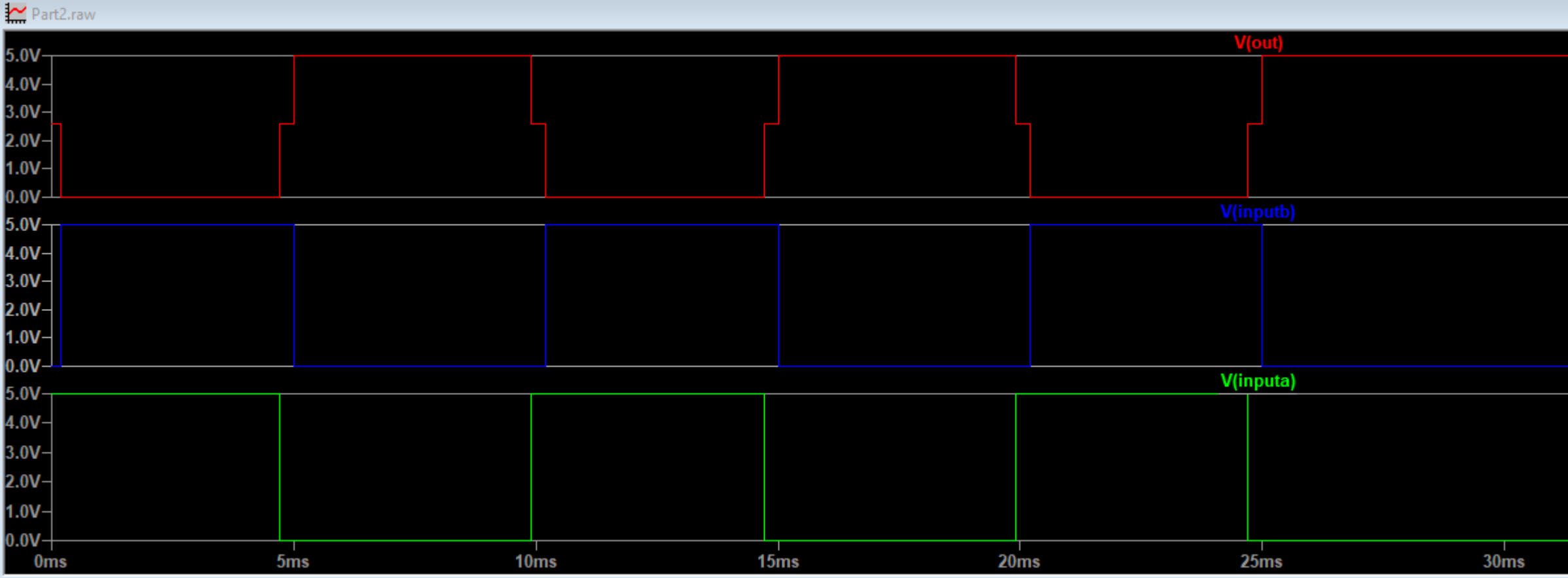

V(xor)
6.0V
5.4V
4.8V
4.2V
3.6V
3.0V
2.4V
1.8V
1.2V
0.6V
0.0V
0.6V
V(b)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V(a)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0ms
3ms
6ms
9ms
12ms
15ms
18ms
21ms
24ms

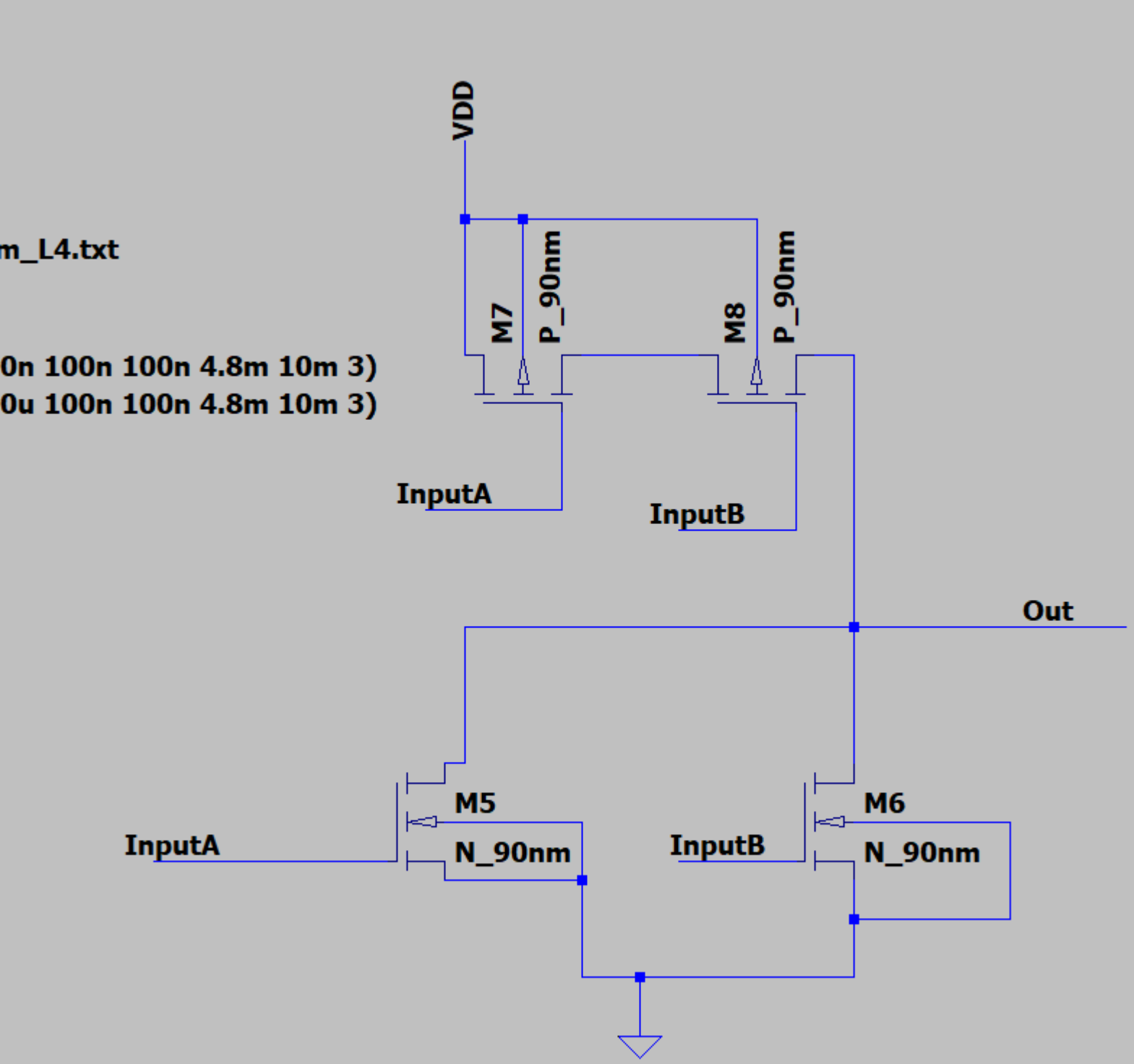

V(in)
V(out)
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.5V
4.0ms
4.3ms
4.6ms
4.9ms
5.2ms
5.5ms
5.8ms
6.1ms
6.4ms
6.7ms
7.0ms
7.3ms
7.6ms
7.9ms
8.2ms
8.5ms
8.8ms
9.1ms
9.4ms
9.7ms
10.0ms

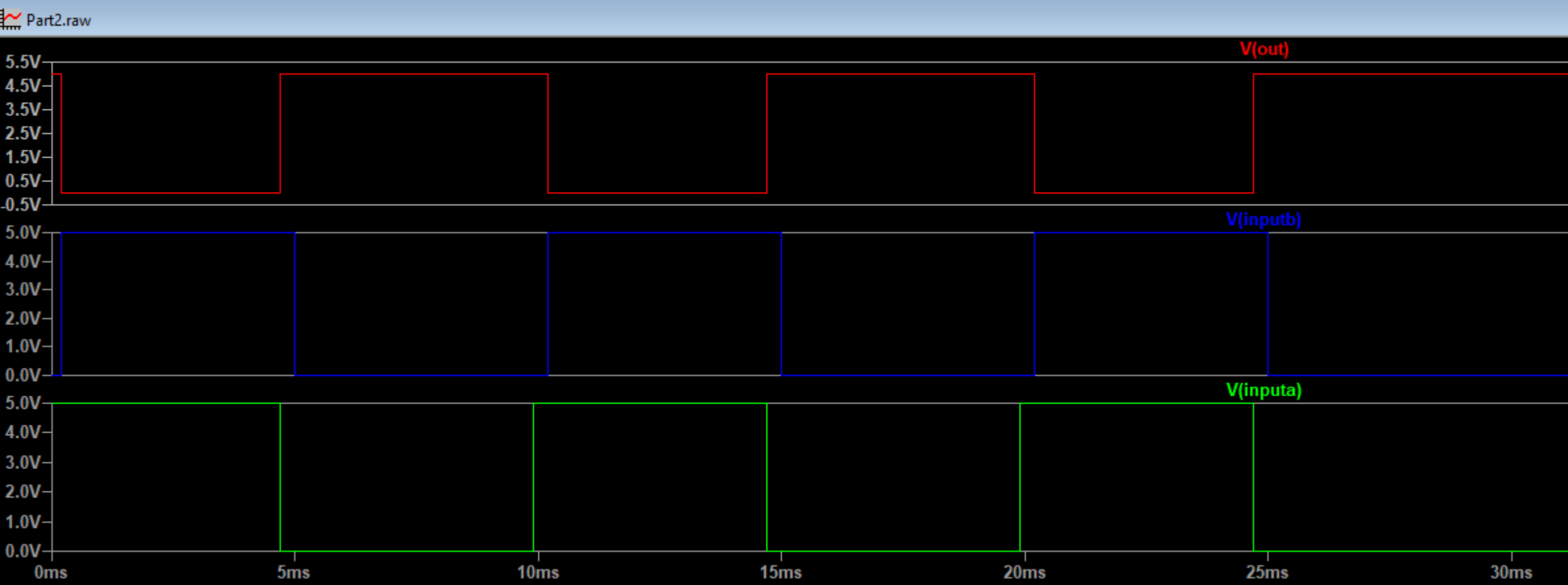

V(in)
V(out)
5.4V
4.8V
4.2V
3.6V
3.0V
2.4V
1.8V
1.2V
0.6V
0.0V
0.6V
4.2ms
4.8ms
5.4ms
6.0ms
6.6ms
7.2ms
7.8ms
8.4ms
9.0ms
9.6ms

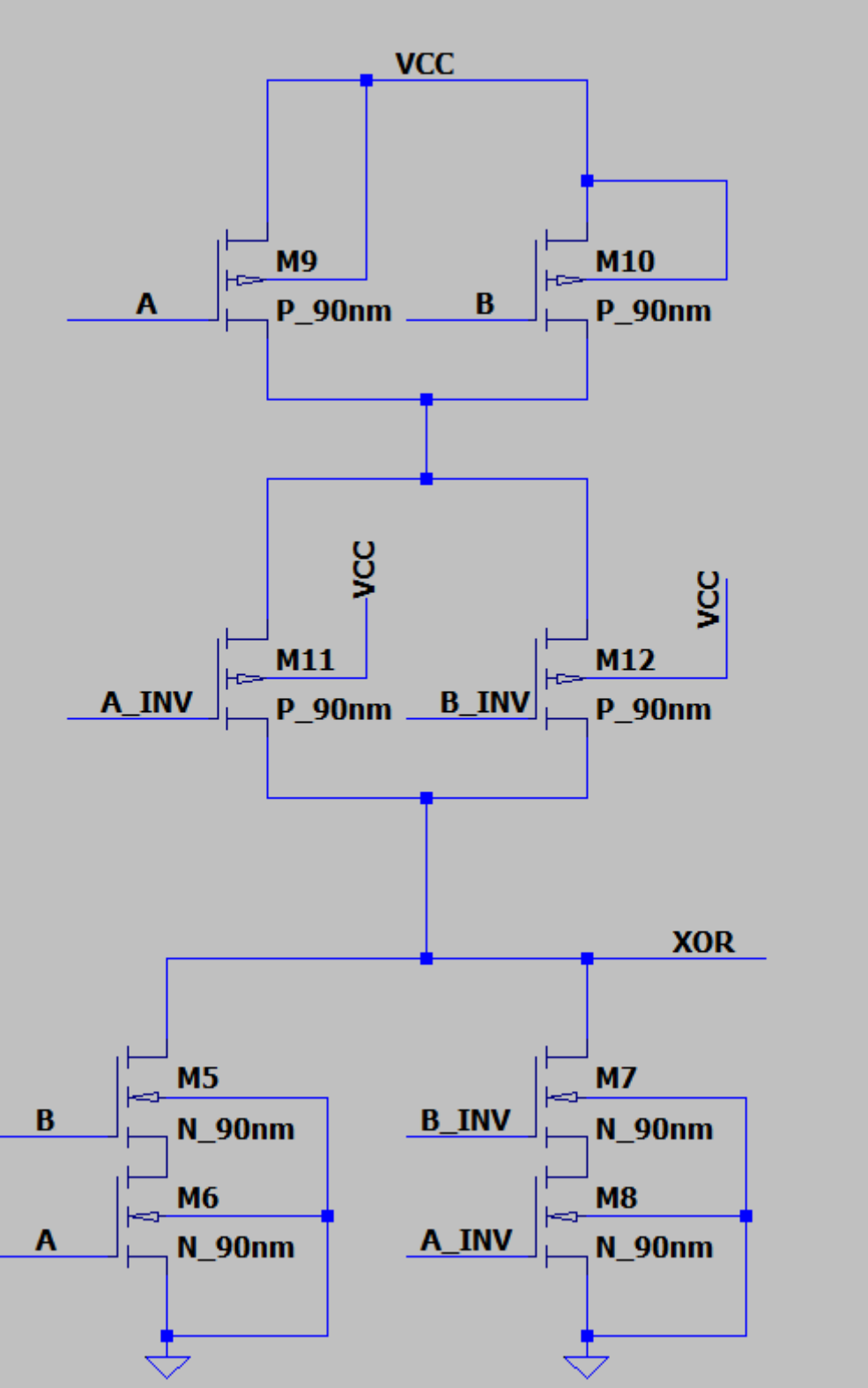


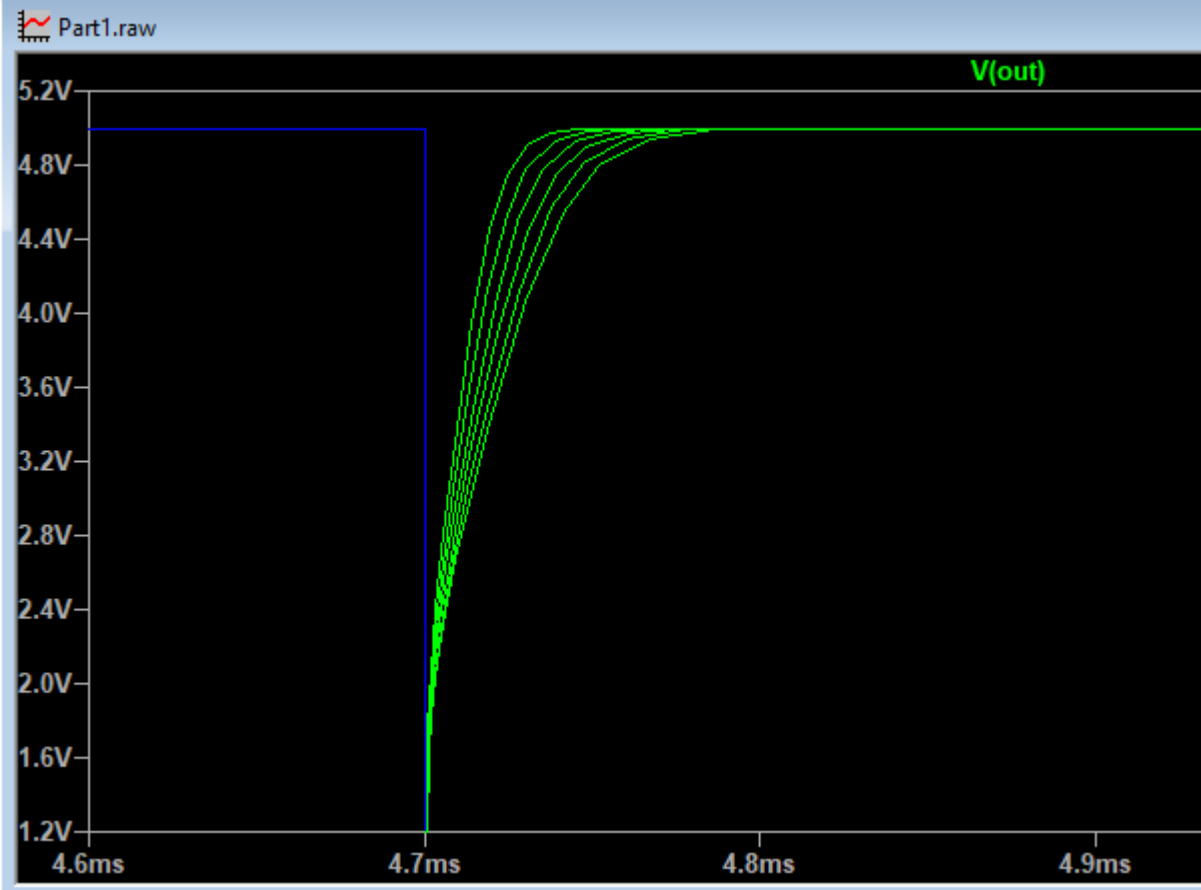

```
.include BSIM_90nm_L4.txt

VDD VDD 0 dc 5

VInputA InputA 0 PULSE(0 5 100n 100n 100n 4.8m 10m 3)
VInputB InputB 0 PULSE(0 5 100n 100n 100n 4.8m 10m 3)
```

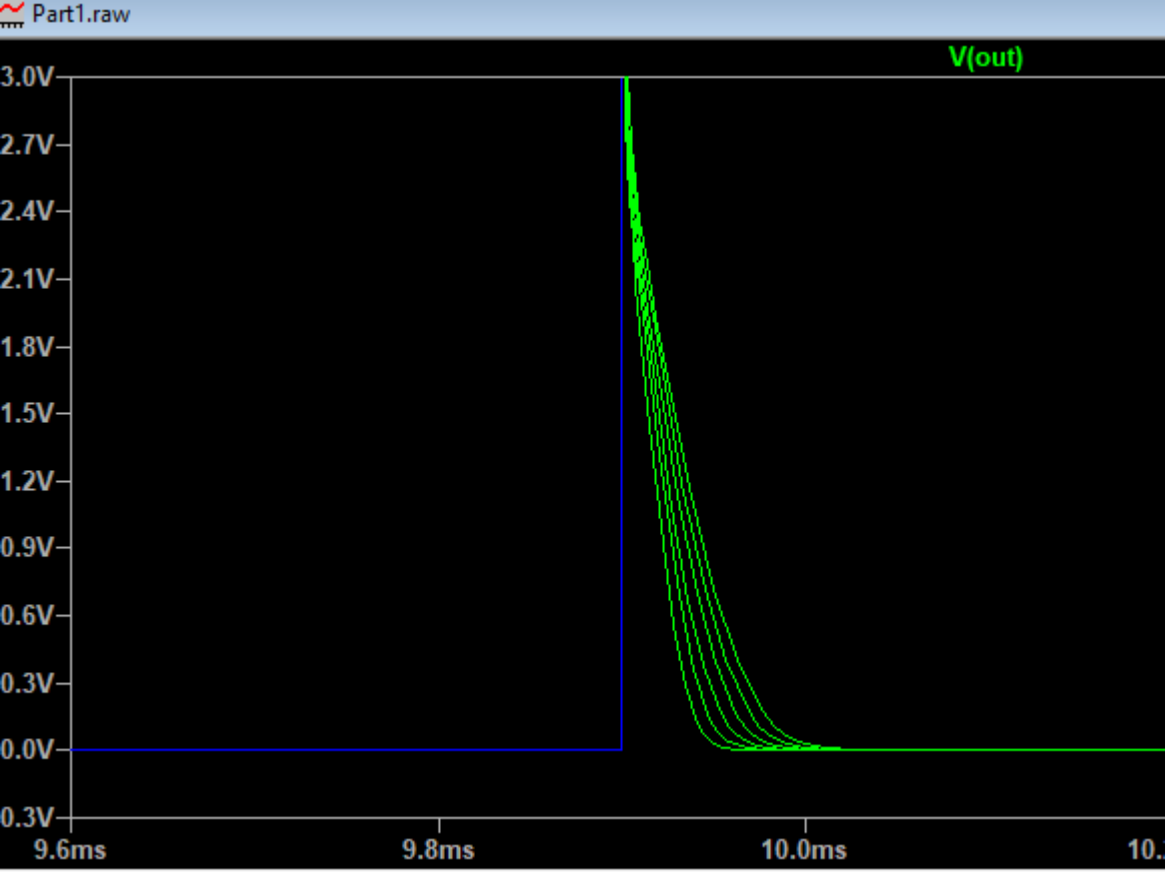

Part2.raw
V(out)
V(inputb)
V(inputa)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms


m_L4.txt
0n 100n 100n 4.8m 10m 3)
0u 100n 100n 4.8m 10m 3)
VDD
M7
P_90nm
M8
P_90nm
InputA
InputB
Out
M5
N_90nm
M6
N_90nm
InputA
InputB


Part2.raw
V(out)
5.5V
4.5V
3.5V
2.5V
1.5V
0.5V
-0.5V
V(inputb)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
V(inputa)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms


VCC
M9
M10
A
P_90nm
B
P_90nm
VCC
VCC
M11
M12
A_INV
P_90nm
B_INV
P_90nm
XOR
M5
M7
B
N_90nm
B_INV
N_90nm
M6
M8
A
N_90nm
A_INV
N_90nm


Part1.raw
V(out)
5.2V
4.8V
4.4V
4.0V
3.6V
3.2V
2.8V
2.4V
2.0V
1.6V
1.2V
4.6ms
4.7ms
4.8ms
4.9ms


Part1.raw
V(out)
3.0V
2.7V
2.4V
2.1V
1.8V
1.5V
1.2V
0.9V
0.6V
0.3V
0.0V
0.3V
9.6ms
9.8ms
10.0ms
10.