Evan Varan
lze4
8/31/23
Lab 02

The screenshots below taken for the lab exercise represent the following. Each number pertains to a screenshot in the order they are shown. Measurements for screenshots 1-3 were taken from an inverter Circuit that contained a capacitor and a resistor in series with an inverter. Measurements for screenshots 4-6 were taken from an NAND Circuit that contained a capacitor and a resistor in series with an NAND gate. Measurements for screenshots 7-9 were taken from an NOR Circuit that contained a capacitor and a resistor in series with an NOR gate. A pulse voltage was applied to each gate in order to simulate a 1 or 0.

1. The inverter circuit.

2. A voltage versus time graph where the green curve represents the input voltage (Vx) applied to the inverter and the blue curve represents the capacitor output voltage (Vout).

3. The same graph as screenshot 2, but with a capacitor that varies in value. Each blue curve represents a different capacitor value.

4. The NAND circuit.

5. A voltage versus time graph where the green curve represents the input voltage(Va) applied to the NAND gate, the blue curve represents the other input voltage (Vb) applied to the NAND gate, and the red curve represents the capacitor output voltage.

6. The same graph as screenshot 5, however the input voltage (Vb) is delayed by 2 milliseconds.

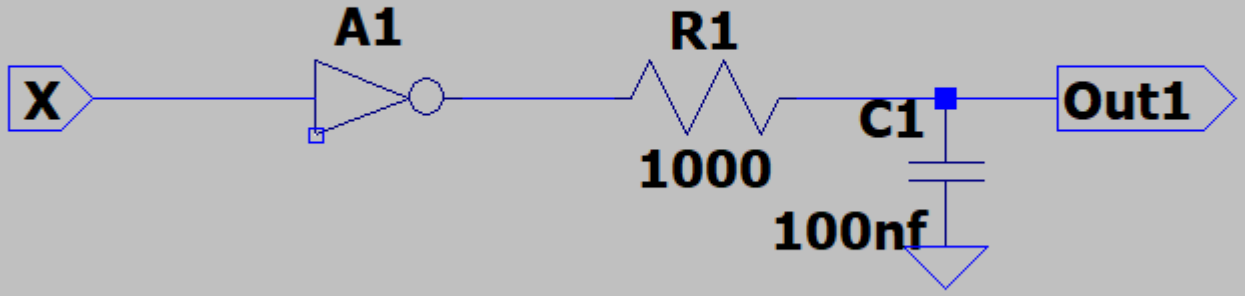
7. The NOR circuit.

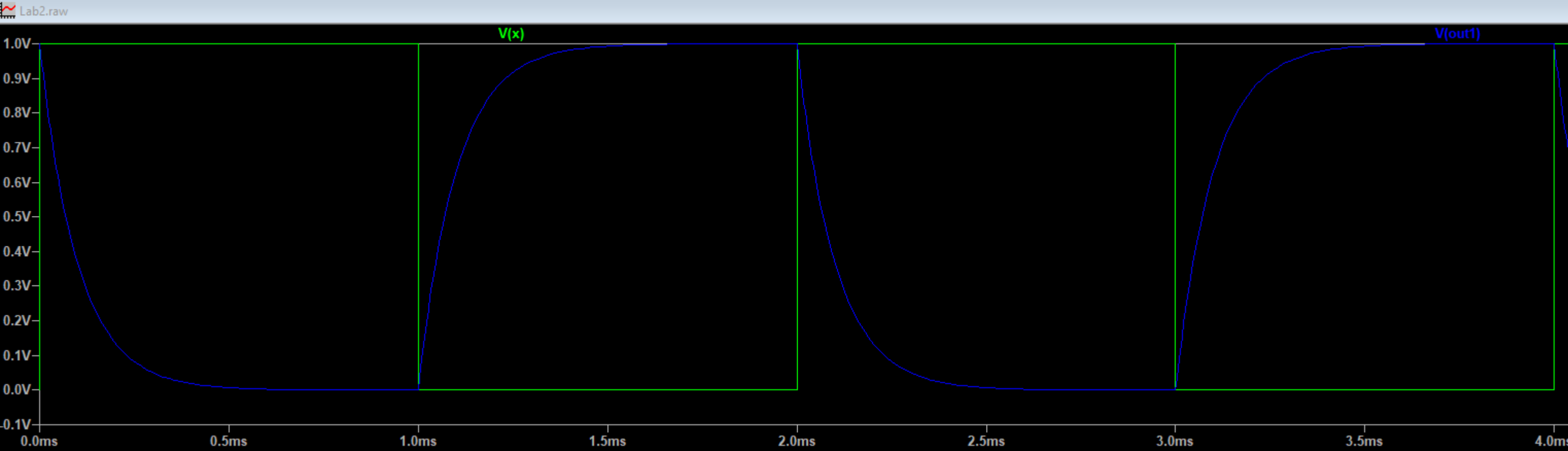
8. A voltage versus time graph where the green curve represents the input voltage(Vc) applied to the NOR gate, the blue curve represents the other input voltage (Vd) applied to the NOR gate, and the red curve represents the capacitor output voltage.

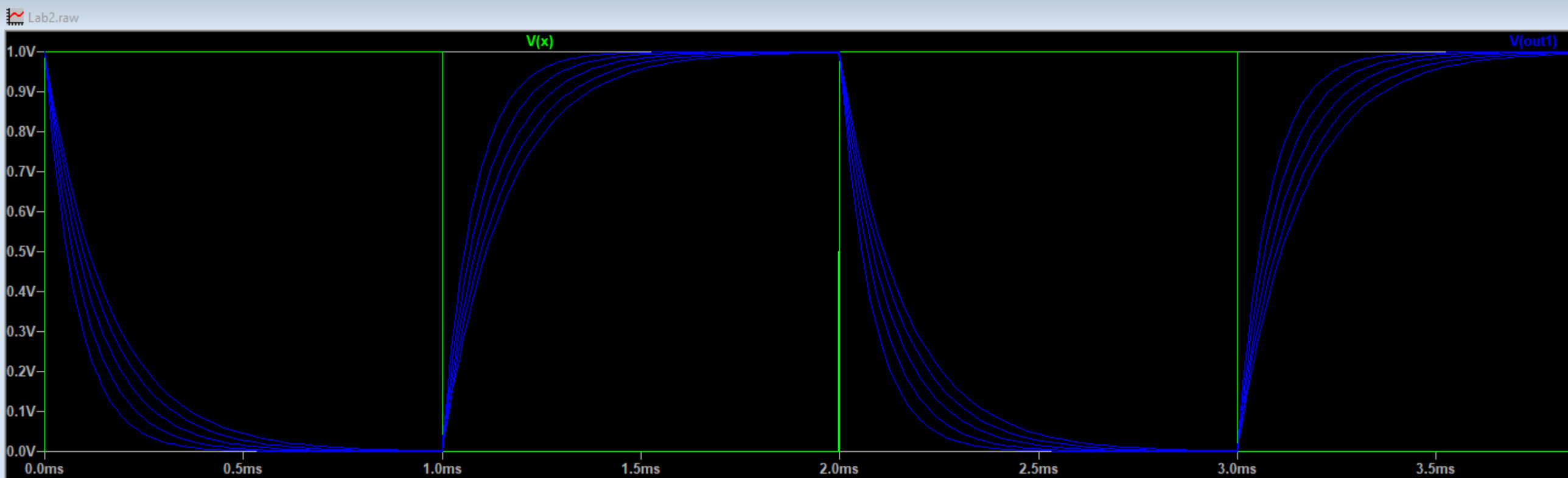
9. The same graph as screenshot 8, however the input voltage (Vd) is delayed by 2 milliseconds.

VX X 0 PULSE(0 1 0ms 100ns 100ns 1ms 2ms 5)

.tran 0 5m



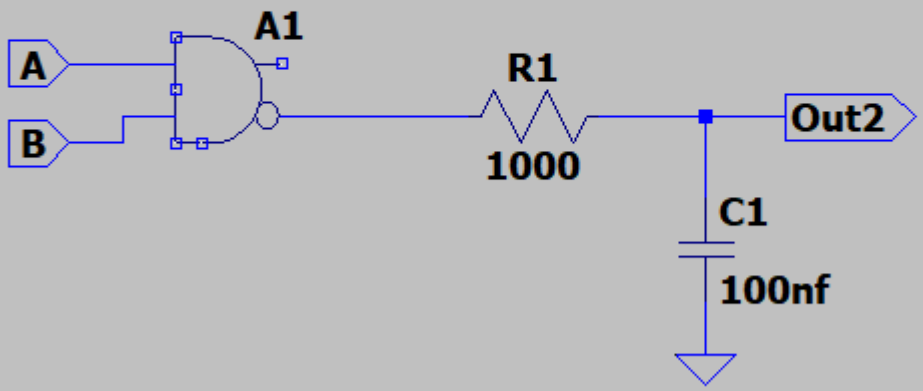

Lab2.raw
V(x)
V(out1)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
-0.1V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms

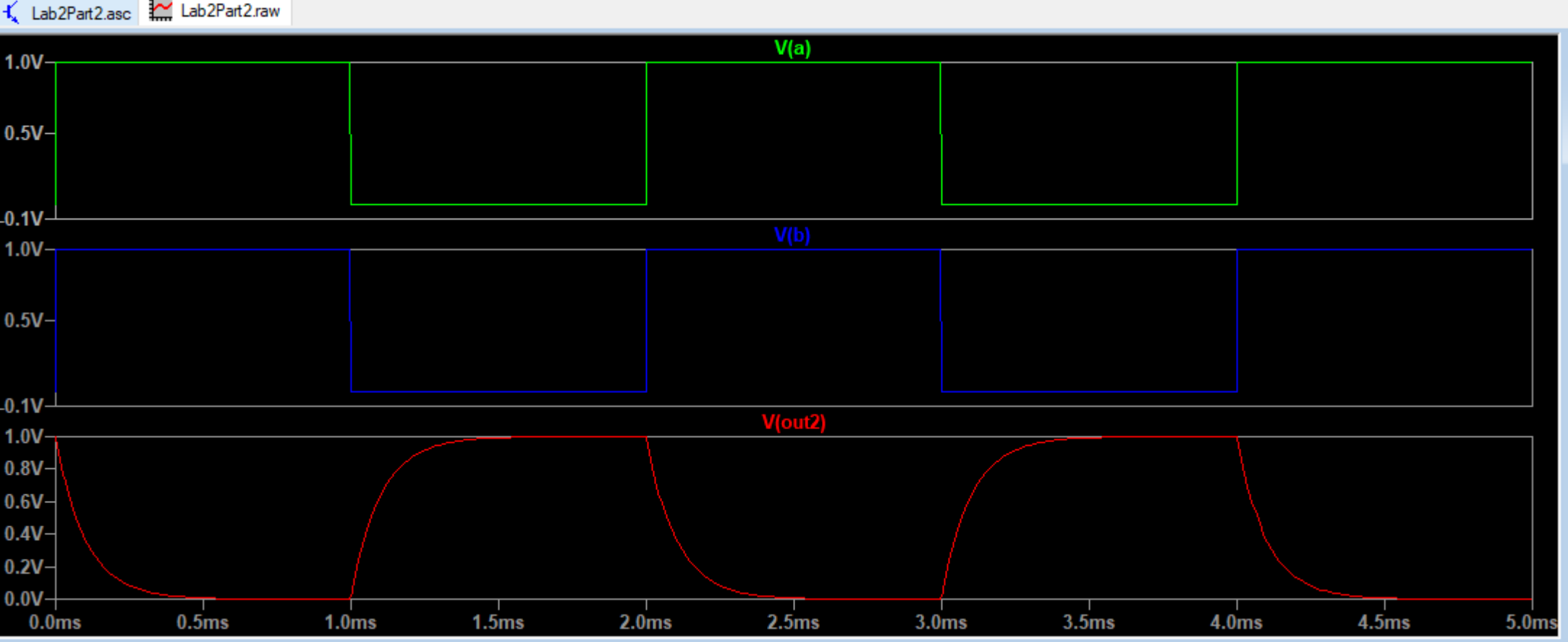

Lab2.raw
V(x)
V(out1)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms

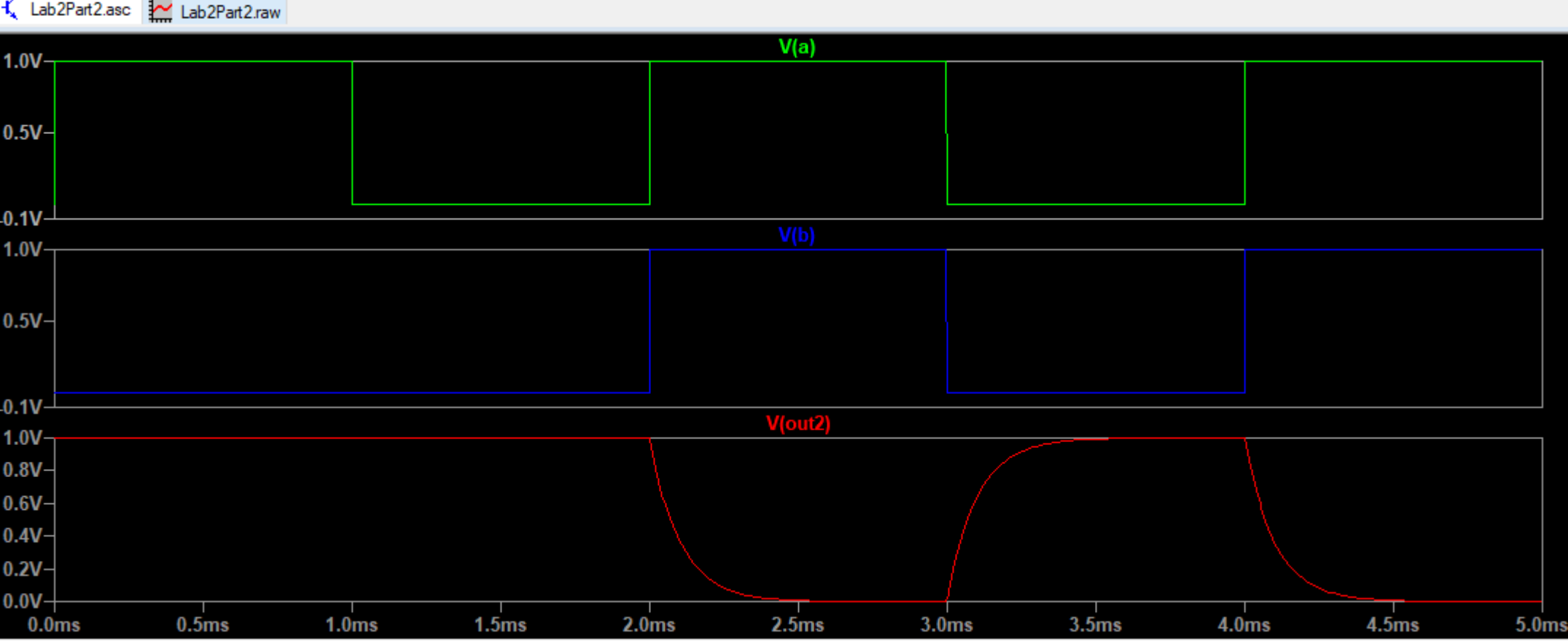
.tran 0 5m

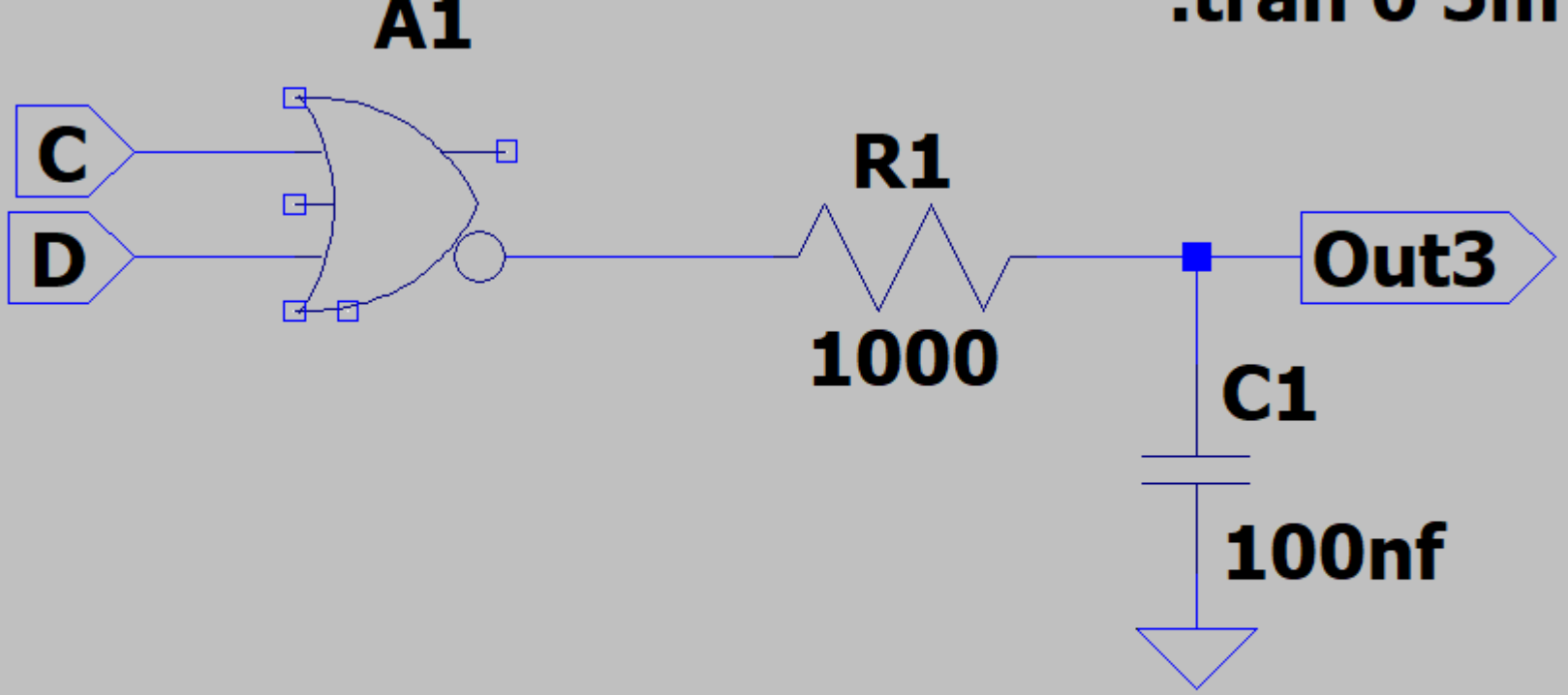
VA A 0 PULSE(0 1 0ms 100ns 100ns 1ms 2ms 5)

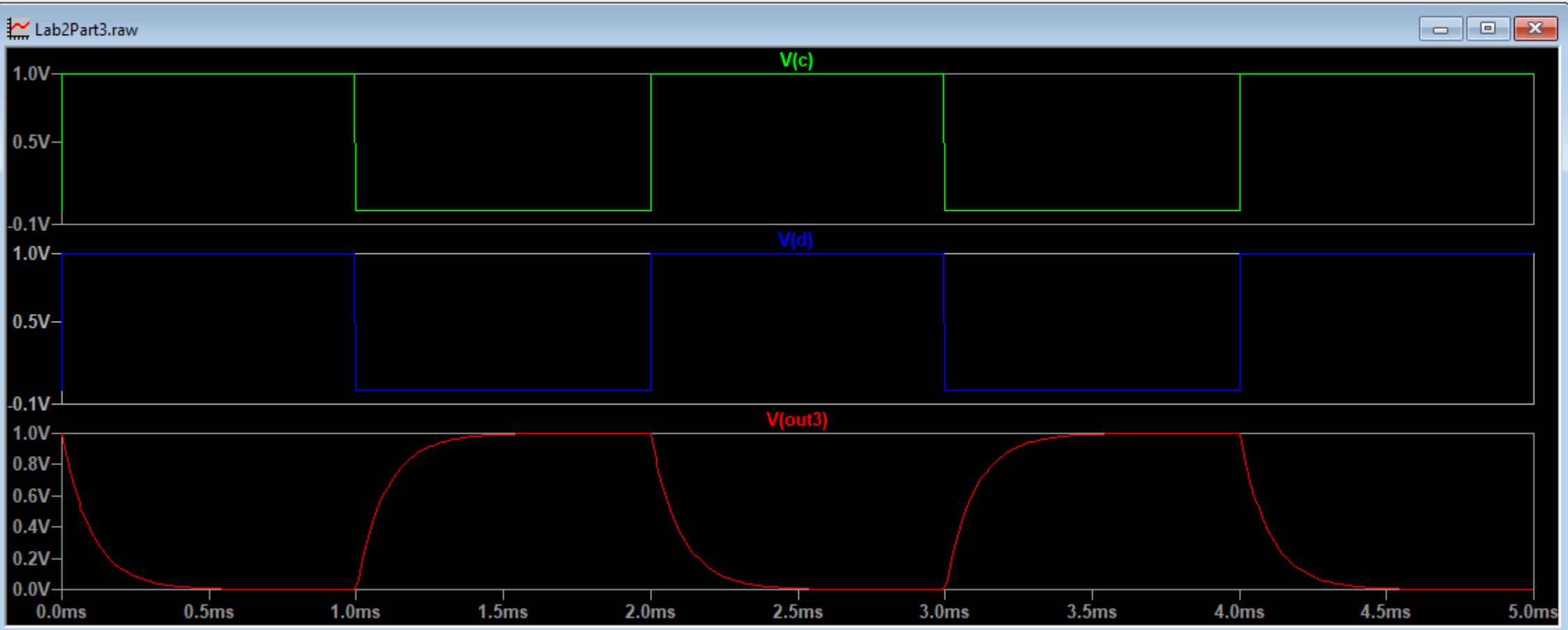
VB B 0 PULSE(0 1 2ms 100ns 100ns 1ms 2ms 5)

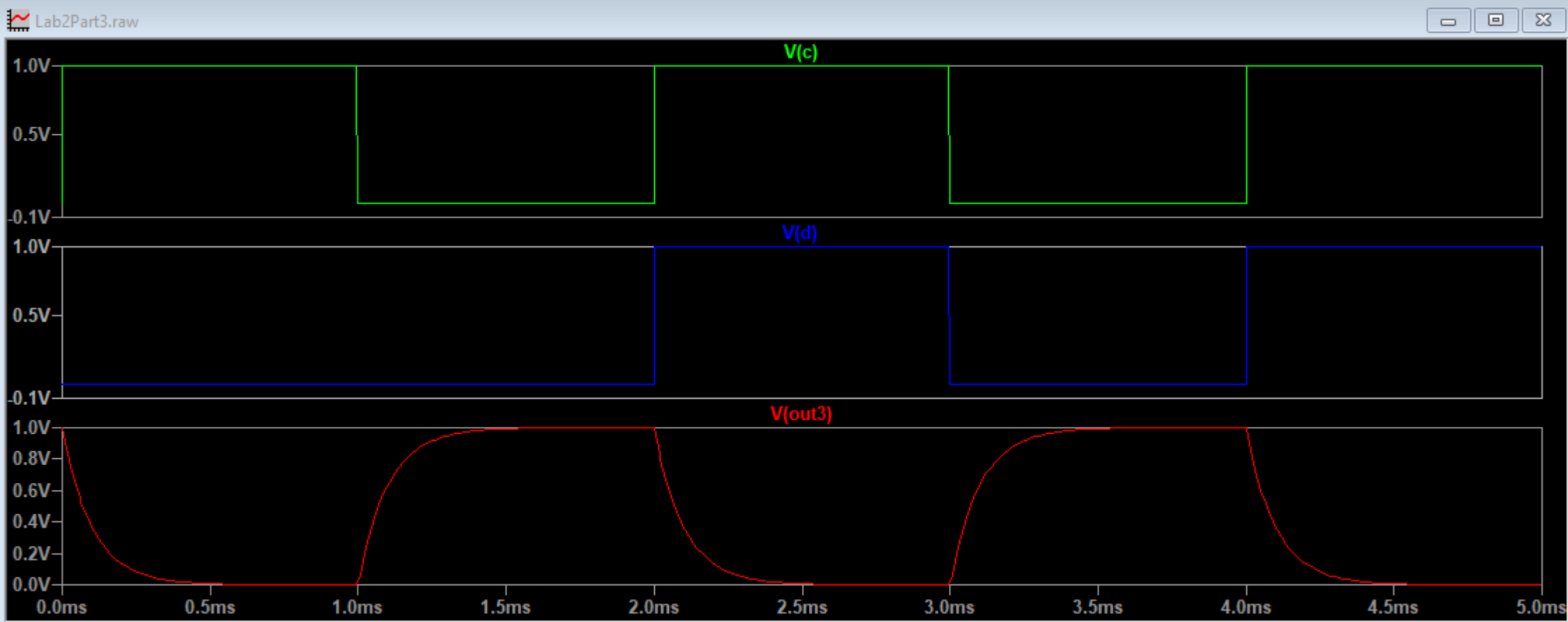



Lab2Part2.asc
Lab2Part2.raw
V(a)
1.0V
0.5V
-0.1V
V(b)
1.0V
0.5V
-0.1V
V(out2)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms


Lab2Part2.asc
Lab2Part2.raw
V(a)
1.0V
0.5V
-0.1V
V(b)
1.0V
0.5V
-0.1V
V(out2)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms


A1
.tran 0 5m
C
D
R1
1000
Out3
C1
100nf


Lab2Part3.raw
V(c)
1.0V
0.5V
-0.1V
V(d)
1.0V
0.5V
-0.1V
V(out3)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms


Lab2Part3.raw
V(c)
1.0V
0.5V
-0.1V
V(d)
1.0V
0.5V
-0.1V
V(out3)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms