Labs 10-12: Controller design

Abstract

Design, implement, and demonstrate an embedded system that controls dc motor speed and an up/down decade counter. Use the NUCLEO-L432KC board. Collect test data with WaveForms instruments.

Design specifications

See the table below for specification details. Some notes:

- The number *N* equals the number of letters in your family name.
- Requirement (a) means a keypad controller must work.
- Requirement (b) means programmable timer-based pwm must work, in addition to requirement (a).
- Requirement (c) means the motor drive amplifier must work, in addition to requirements (a) and (b).
- Requirement (d) means the counter timing and control are triggered by programmable timer interrupts.
- Requirement (e) means the analog-to-digital converter (ADC) is employed to measure a properly conditioned tachometer signal. Rather than selecting desired pwm duty cycle, the keypad selects a desired ADC count.
- Extra credit requires more effort in feedback controller design and/or tuning.

Item	Points	Description
a	3	Correctly decode all buttons of a 16-button keypad.
b	3	Produce an *N* kHz pulse-width-modulated (pwm) signal. 1. Any 10 different non-zero duty cycles may be chosen, in addition to 0% duty cycle. 2. Duty cycles are selected with keypad buttons 0-A. 3. Duty cycle must not be affected by the motor drive (c) or the counter (d)
c	3	Produce a dc motor drive controlled by the pwm signal (b). 1. Motor drive operates from 10-15 Vdc power supply. 2. Motor drive operation does not affect the pwm signal (b) or the counter (d).

d	3	Produce an up/down decade counter. 1. The counter period is *N*/5 s, and the error is less than 100 ppm (0.01%). 2. The counter value rolls over and repeats. 3. Button (*) is starts/stops the counter. 4. Button (#) changes the count direction (up/down). 5. Counter operation does not affect the pwm signal (b) or the motor drive (c).
e	3	Implement feedback control of the motor speed. 1. Desired motor speed is selected by keypad button press. 2. Provide at least four different non-zero desired speeds. 3. Steady-state speed error is less than 5% of desired speed 4. ADC sampling period equals counter period divided by 64.
xc	3	(Extra credit) All specifications (a-e) must work. 1. Steady-state speed error is less than 1% of desired speed, AND 2. Step response overshoot is less than 10% of desired speed change. Step response test is conducted anywhere in the range of 30-80% of full speed. For example, if the desired speed change is from 40% to 50% of full speed, then overshoot must be less than 1% of full speed.

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