EECS 645 Computer Architecture

Homework 5. Due March 3, 2020 at 4:00pm.

Extract the contents of the provided z80memhdl folder and place them in your existing z80hdl folder so that the components can refer to each other.

In this homework you will implement the following logic blocks using the provided templates, and test files. I recommend you implement them in the following order, and after verifying a module, I encourage you to use it where applicable in subsequent modules. Use the included tst file for each module to validate it.

DMux – see slides for nand representation
DMux8Way- 3 bit decoder
Mux8Way8
Bit – use a builtin DFF module, also need to have two out= statements (see slides)
Byte
DoubleReg
MEM8
MEM64
MEM512

Only use nand gates, DFF, or other modules you have built previously when implementing these.
Submit a zip file of your complete directory with all .hdl, .cmp, .out, .tst files for all modules from HW5, HW4, and HW3.

Some implementation hints:
To set a bit input low you can say a=false for example.
If you need to work with sub sets of a bus you can do things like a[0]=sel, a[1..3]=true, a[4..7]=false
A common example might be to use parts of a bus for one thing such as sel=address[3..5] and a different part elsewhere addr=address[0..2]
The simulator has issue with using an output internally at the same time, but you can have more than one out with label to work around it.