EECS 645 Computer Architecture

Homework 4. Due Feb 25, 2020 at 4:00pm.

Extract the contents of the provided z80aluhdl folder and place them in your existing z80hdl folder so that the components can refer to each other.

In this homework you will implement the following logic blocks using the provided templates, and test files. I recommend you implement them in the following order, and after verifying a module, I encourage you to use it where applicable in subsequent modules. Use the included tst file for each module to validate it.

Inc16 – a 16 bit incrementor.
AddSub8 – extend your Add8 to also perform subtraction.
Mux – a single bit 2 way mux
Mux8 – an eight bit 2 way mux
Mux4Way8 – and eight bit 4 way mux
ALU – a simple z80 ALU

Only use nand gates or other modules you have built previously when implementing these. Submit a zip file of your complete directory with all .hdl, .cmp, .out, .tst files for all modules from HW4 and HW3.

Some implementation hints:
For the AddSub implement the circuit as shown in the slides, ignoring the carry.
To set a bit input low you can say a=false for example.
If you need to work with sub sets of a bus you can do things like a[0]=sel, a[1..3]=true, a[4..7]=false