海奇半导体

B200

Brief Datasheet

HI-CHIP Corporation

B200

Brief Datasheet

CONTENTS

B200 Brief Data Sheet

1 What is B200

The B200 processor represents Hi-Chip Semiconductor's cost effective achievement in multimedia applications processors. The processor targets the needs of electronics market with LCD screens.

The B200 processor is a high-integration and cost effective SOC. It embedded one 32bit RISC CPU, a Crypto Engine , a multi-format full HD video decoder, a 2D-graphic accelerator, a high quality display engine, a flexible audio DMA engine , audio DAC and I2S /PCM interface. It also supports digital video input , RGB video output and a 8bit SAR ADC and etc.

The B200 supports external DDR2/DDR3, and packed with rich general-purpose peripherals such as USB OTG, SD/MMC, SPI, UART, I2C, IR and so on.

The B200 outperforms competitors in terms of its powerful performance, low power consumption and flexible scalability.

2 Features of B200

2.1 Key Specification

- 32-bit RISC CPU
- 16-bit DDR2 or DDR3
- Multi-format video decoder with high definition solutions, max 1920x1080p@60
- Advanced display engine with video rotation
- Audio DAC and I2S/PCM interface
- 8bit data video in
- 2-ports USB EHCI Host/Device, one can support OTG
- SD/MMC
- 8bit-SARADC

2.2 High-Performance CPU

- 32-bit single core RISC CPU
- Maximum frequency of 800Mhz, applications smoothly
- Independent 16KB I-cache, 16KB D-cache

2.3 Memory Sub-System

- This section consists of internal memory and external memory
- Boot ROM
- SDRAM
- SPI Nor/Nand Flash interface
- SD/MMC interface

2.3.1 Boot ROM

- embedded boot ROM
- On chip ROM boot loader
- Support system boot from SPI Nor/Nand Flash
- Support system code upgrade from UART/USB

2.3.2 SDRAM

- External 16bit DDR2/DDR3 SDRAM operation
- Compatible with JEDEC standard DDR3/DDR2 SDRAM
- Data rate up to 1066Mbps for DDR2 and up to 1333Mbps for DDR3
- Maximum 256MB capcacity
- Complete PHY initialization, training and control from various vendor

2.3.3 SPI Nor/Nand Flash interface

- Support 1-bit, 2bit, SPI flash
- Maximum frequency 50MHZ
- Maximum capacity of 32MB
- Support DMA and FIFO mode
- SPI MODE0, MODE3 supported.
- Support CRC calculation when reading data form FLASH in BYTE or DWORD format

2.3.4 SD/MMC interface

- Support SD/SDIO cards
- Support MMC and eMMC Cards
- Support one SD (version up to 2.0) or MMC (version up to eMMC 4.41)
- Support half-duplex serial and parallel data transfer for 1bit, 4bit data lines
- Maximum frequency 50MHZ
- Support hardware CRC generation and error detection

- Single or multiple block oriented data transfer, block and burst length programmable
- Support PIO and DMA read/write

2.4 Video Decoder

- H.264 BP/MP/HP@level 5.0, 1080p@60 fps
- H264 MVC, 1080p@60 fps
- MPEG1, 1080p@60 fps
- MPEG2 SP@ML, MP@HL, and 1080p@60 fps
- MPEG4 SP@level 0−3, ASP@level 0−5, GMC, 1080p@60 fps
- MPEG4 short header format (H.263 baseline), 1080p@60 fps
- DivX 3/4/5/6, 1080p@60 fps
- AVS baseline@level 6.0, AVS+(AVS-P16), and 1080p@60 fps
- VC-1 SP@ML, MP@HL, and AP@level 0−3, 1080p@60 fps
- JPEG hardware decoding, a maximum of 64 megapixels
- MJPEG baseline decoding

2.5 Jpeg Encoder

- Baseline ISO/IEC 10918-1 Jpeg compliant
- 8-bit/channel pixel depths
- Fixed Quantization and Huffman tables
- Fully programmable MCU(minimun coding unit)
- Hardware support for Restart markers insertion
- Input raw image
  - YCbCr 4:2:0
  - YCbCr 4:2:2
- Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
- Encoder image size up to 8192x8192(64million pixels) from 96x32
- Speed up to 720p@30

2.6 Video in

- BT.656 interface
- BT.601 interface with 8bit data width

- DVP interface with 8bit data width
- Speed up to 720p@60

2.7 2D-Graphic Acceleration

- Data format :
  - RGB888/ ARGB8888
  - RGB555/ ARGB1555
  - RGB444/ ARGB4444
  - RGB565
  - CLUT4/8, ACLUT88
- RLE8/16/32 decoder
- Color space convert
- Gamma correction, and contrast/luminance adjustment
- Bicubic filter to support image scaling
- Arbitrary degrees rotation
- Direct copy , color filling and pattern filling
- ROP acceleration
- Alpha blending modes including Java 2 Porter-Duff compositing blending
- DirectFB acceleration
- Color keying ,dither, pattern mask and window clipping
- Programmable scanning mode
- Linked-list operation

2.8 Display System

2.8.1 Display engine

- Output size up to 2048x2048
- Support up to 4 channel layers and programmable blending order
  - Main video layer
  - Auxilary picture layer
  - OSD layer 1
  - OSD layer 2
- All 4 layers have independent scaler
- Color conversion, brightness, contrast,saturation and hue adjustment and gamma correction

- Main video layer 90°, 180°, 270° rotation
- Main layer input data format
  - YUV 420 /YUV 422/ YUV 411
- Auxilary layer input data format
  - YUV 420 /YUV 422/ YUV 411
- OSD layers input data format
  - ARGB 8888/4444/1555
  - RGB888/RGB444/RGB565
  - CLUT2/CLUT4/CLUT8/ACLUT88

2.8.2 Display output interface

- Support RGB output interface
  - RGB888/RGB666 output
  - Support hsync mode and de mode
  - Support maximum resolution up to 1280x720p@60

2.9 Audio System

2.9.1 Audio Decoding /Encoding

- Software audio decoding formats
  - MPEG L1/L2
  - MP3
  - AAC_LC, HE_AAC, HE_AACV2
  - LPCM
  - APE
  - FLAC
  - OggVorbis
  - AMRNB
  - AMRWB
  - G.711 (u/a)
- Software audio encoding formats
  - AAC_LC, HE_AAC, HE_AACV2
  - AMR-NB
  - G.711 (u/a)

- MP3

2.9.2 Audio interface

- PWM DAC
  - PWM modulator stereo DAC output
    - Single ended output
    - 80±3db@A-weight
  - Support Earphone output with Titanium mode.
  - Audio Data adaptive synchronize
  - Programmable volume control
  - Pop up noise management
  - Embeded power saving
- SPDIF output
  - Support 1 set spdif output
  - Support sample rate from 8khz to 192khz
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer
- I2S output
  - Support 1 set I2S output
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Support master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
- I2S input
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Support master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)

2.10 SAR-ADC

- 8bit Successive Approximation Register (SAR) architecture
- 3.3V analog supply and 1.1V digital supply operation
- Single-ended analog input range: 0V to 2V
- Sampling frequency 6.25ksps/12.5ksps/25ksps/62.5ksps (programmable)
- 16x master clock frequency (to sample frequency ratio)
- Ultra low power consumption: 500uW @ 100Ksps
- Integral Nonlinearity: -/+1LSB
- Differential Nonlinearity: -/+0.5LSB
- SNR: 42dB
- SFDR: 42dB
- Wake up time: 100us

2.11 External Peripherals

2.11.1 USB2.0

- Contains 2 usb ports,port0 support OTG function
- Complies with the USB 2.0 standard for high-speed (480 Mbps)
- Support host or device function
- Support hi-,full- or low- speed device
- 5 additional transmit endpoint and 5 receive endpoint

2.11.2 UART

- Support up to 2 uart sets
- DMA-based or interrupt-based operation
- Compliant with industry-standard 16450 and 16550 uarts
- Support RS232 protocol
- Support 5bit,6bit,7bit,8bit serial data bits, an optional parity bit and 1, 1.5 or 2 stop bits
- Programmable parity(even , odd and no parity)
- Programmable clock divides for band clock generation
- Support clock frequency up to 2 MHZ

2.11.3 I2C

- Support up to 3 I2C sets
- Multi-master I2C operation
- Support 7bits and 10bits address mode

- programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
- Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

2.11.4 SPI

- Share pins with SPI flash pin
- Support serial-master mode with 1 or 2 data bits
- Maximum frequency 50MHZ
- Maximum capacity of 32MB
- Support DMA and FIFO mode
- SPI MODE0, MODE3 supported.
- Support CRC calculation when reading data form FLASH in BYTE or DWORD format

2.11.5 SDIO

- Share with SDIO memory interface
- Compatible with SDIO 2.0 protocol
- Maximum frequency 50MHZ
- 4 bits data bus width

2.11.6 TS

- One transport stream controller
- One external synchronous serial interface (SSI)
- Up to 100Mbps

2.11.7 IR receiver

- A flexible receiver for IR remote
- Programmable FIFO threshold

2.11.8 PWM

- Support up to 3 PWM channels with interrupt based operation
- Programmable pre-scaled operation to bus clock and then further scaled
- Embedded 32-bit timer/counter facility
- Support continuous mode or one-shot mode
- 0% to 100% adjustable duty cycle
- Up to 54MHZ output frequency

- Minimum resolution is 1/65536

2.11.9 GPIO

- 4 groups of GPIO (GPIOL,GPIOB,GPIOR,GPIOT), totally GPIO numbers base on different prodcuct & package.
- All of GPIOs can be used to generate interrupt
- All of GPIOs are always in input direction in default after power-on-reset

2.12 System component

2.12.1 Clock and Reset unit

- One oscillator with 27MHZ clock input and 4 embedded PLLs
- Support clock gating control for individual components
- Support global soft-reset control for whole SOC, also individual soft-reset for every components

2.12.2 Timer

- 8 on chip 32bits Timers in SOC with interrupt-based operation
- Provide two operation modes: free-running and user-defined count
- Support timer work state checkable
- Fixed 27MHz clock input

2.12.3 WatchDog

- 32 bits watchdog counter width
- Counter clock is from apb bus clock
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length

2.12.4 Interrupt Controller

- Support every interrupt sources input from different components.
- Every interrupt polarity and enable can by software programmable.

- Hardware not distinguished the interrupt source priority.

2.12.5 DMA Controller

- One set of scatter/Gather DMA
- 8 lists supported
- Start code search function supported

2.12.6 Crypto Engine

- Embeds AES, DES, SHA-1/SHA-256
- Support 128-bit, 192-bit and 256-bit key size for AES
- Support ECB, CBC,CTR,CTS mode for AES
- Support ECB,CBC,CTR mode for DES
- Support cpu mode and DMA mode

3 Block Diagram

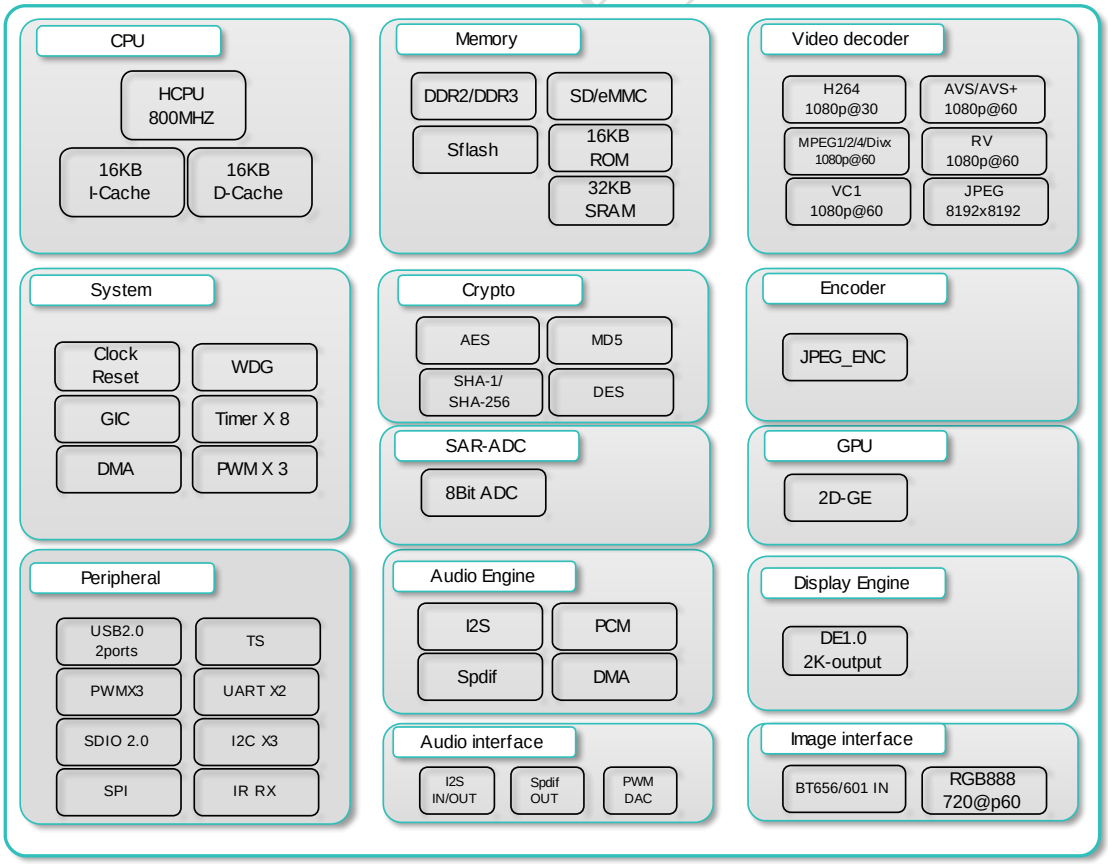


Table 3-1 Block Diagram

4 Pin Descriptions

4.1 Pin Characteristics

I -> input Following table list the characteristics of B200 pins from the following aspects:

- Pin# : Pin numbers associated with each signals.
- Pin Name : The name of the package pin.
- Signal Name : the signal name for that pin in the mode being used
- Function# : Function number
- Type : Denote the signal direction
  -
  - O->output
  - B->input/output
  - A->Analog
  - AI->Analog input
  - AO->Analog output
  - P->power
  - G->ground
- Pull Up/Down : denote the internal pull up or pull down resistor.
- Power : the voltage supply for the terminal's IO buffers

Pin#	Pin Name	Type	Power supply	Pull up/down	Function#	Signal name
1	XGPIO_L0	B	VDD_IO	U	0	GPIO_L0
		O	VDD_IO	U	6	PRGB_B1
		B	VDD_IO	U	8	I2C3_SCL
2	XGPIO_L1	B	VDD_IO	Z	0	GPIO_L1
		O	VDD_IO	Z	6	PRGB_B2
3	XGPIO_L2	B	VDD_IO	Z	0	GPIO_L2
		O	VDD_IO	Z	6	PRGB_B3
4	XGPIO_L3	B	VDD_IO	Z	0	GPIO_L3
		O	VDD_IO	Z	6	PRGB_B4
5	XGPIO_L4	B	VDD_IO	Z	0	GPIO_L4
		O	VDD_IO	Z	6	PRGB_B5
6	XGPIO_L5	B	VDD_IO	Z	0	GPIO_L5
		O	VDD_IO	Z	6	PRGB_B6
7	XGPIO_L6	B	VDD_IO	Z	0	GPIO_L6

		O	VDD_IO	Z	6	PRGB_B7
8	XGPIO_L7	B	VDD_IO	Z	0	GPIO_L7
		O	VDD_IO	Z	6	PRGB_CLK
9	XGPIO_L8	B	VDD_IO	Z	0	GPIO_L8
		O	VDD_IO	Z	6	PRGB_HSYNC
10	XGPIO_L9	B	VDD_IO	Z	0	GPIO_L9
		O	VDD_IO	Z	6	PRGB_VSYNC
11	XGPIO_L10	B	VDD_IO	U	0	GPIO_L10
		O	VDD_IO	U	1	PWM_0
		I	VDD_IO	U	3	IR
		O	VDD_IO	U	6	PRGB_DE
12	XGPIO_L11	B	VDD_IO	U	0	GPIO_L11
		O	VDD_IO	U	1	SF_CSJ0
13	XGPIO_L12	B	VDD_IO	Z	0	GPIO_L12
		O	VDD_IO	Z	1	SF_MISO
14	XGPIO_L13	B	VDD_IO	Z	0	GPIO_L13
		B	VDD_IO	Z	1	SF_MOSI
15	XGPIO_L14	B	VDD_IO	Z	0	GPIO_L14
		O	VDD_IO	Z	1	SF_CLK
16	XGPIO_L15	B	VDD_IO	U	0	GPIO_L15
		O	VDD_IO	U	1	SF_CSJ1
17	XGPIO_L16	B	VDD_IO	Z	0	GPIO_L16
		I	VDD_IO	Z	1	SSI_MISYNC
		B	VDD_IO	Z	4	SDIO_D1
		I	VDD_IO	Z	5	VIN_D0
		I	VDD_IO	Z	6	VIN_D7
		I	VDD_IO	Z	7	UART1_RX
18	XGPIO_L17	B	VDD_IO	Z	0	GPIO_L17
		I	VDD_IO	Z	1	SSI_MISYNC
		B	VDD_IO	Z	4	SDIO_D0
		I	VDD_IO	Z	5	VIN_D1
		I	VDD_IO	Z	6	VIN_D6
		O	VDD_IO	Z	7	UART1_TX
19	VDD_IO	P	NA	NA	NA	NA
20	XGPIO_L18	B	VDD_IO	Z	0	GPIO_L18
		I	VDD_IO	Z	1	SSI_MICLK
		B	VDD_IO	Z	4	SDIO_CLK
		I	VDD_IO	Z	5	VIN_D2
		I	VDD_IO	Z	6	VIN_D5
21	XGPIO_L19	B	VDD_IO	Z	0	GPIO_L19
		I	VDD_IO	Z	1	SSI_MID
		B	VDD_IO	Z	4	SDIO_CMD

		I	VDD_IO	Z	5	VIN_D3
		I	VDD_IO	Z	6	VIN_D4
22	XGPIO_L20	B	VDD_IO	U	0	GPIO_L20
		B	VDD_IO	U	3	I2C2_SDA
		B	VDD_IO	U	4	SDIO_D3
		I	VDD_IO	U	5	VIN_D4
		I	VDD_IO	U	6	VIN_D3
23	XGPIO_L21	B	VDD_IO	U	0	GPIO_L21
		B	VDD_IO	U	3	I2C2_SCL
		B	VDD_IO	U	4	SDIO_D2
		I	VDD_IO	U	5	VIN_D5
		I	VDD_IO	U	6	VIN_D2
24	XP_CRSTJ	I	VDD_IO	NA	NA	NA
25	XGPIO_L23	B	VDD_IO	U	0	GPIO_L23
		O	VDD_IO	U	1	PWM_0
		I	VDD_IO	U	2	I2S_DATAI
		O	VDD_IO	U	3	I2S_DATAO
		I	VDD_IO	U	4	IR
		I	VDD_IO	U	5	VIN_D6
		I	VDD_IO	U	6	VIN_D1
26	XGPIO_L24	B	VDD_IO	Z	0	GPIO_L24
		I	VDD_IO	Z	1	SSI_MISYNC
		B	VDD_IO	Z	2	I2S_LRCK
		B	VDD_IO	Z	3	I2S_MCLK
		I	VDD_IO	Z	5	VIN_D7
		I	VDD_IO	Z	6	VIN_D0
27	XGPIO_L25	B	VDD_IO	Z	0	GPIO_L25
		I	VDD_IO	Z	1	SSI_MIVLD
		B	VDD_IO	Z	2	I2S_BCLK
		B	VDD_IO	Z	3	I2S_BCLK
		O	VDD_IO	Z	4	SPDIF_O
		I	VDD_IO	Z	6	VIN_CLK
28	XGPIO_L26	B	VDD_IO	D	0	GPIO_L26
		I	VDD_IO	D	1	SSI_MICLK
		B	VDD_IO	D	2	I2S_MCLK
		B	VDD_IO	D	3	I2S_LRCK
		O	VDD_IO	D	4	SPDIF_O
		B	VDD_IO	D	5	HDMI_CEC
		O	VDD_IO	D	6	TVE_HSYNC
		I	VDD_IO	D	7	VIN_HSYNC
29	VDD_CORE	P	NA	NA	NA	NA
30	XGPIO_L27	B	VDD_IO	Z	0	GPIO_L27

		I	VDD_IO	Z	1	SSI_MID
		O	VDD_IO	Z	2	I2S_DATAO
		I	VDD_IO	Z	3	I2S_DATAI
		O	VDD_IO	Z	4	SPDIF_O
		I	VDD_IO	Z	5	HDMI_HTPG
		O	VDD_IO	Z	6	TVE_VSYNC
		I	VDD_IO	Z	7	VIN_VSYNC
31	XGPIO_L28	B	VDD_IO	U	0	GPIO_L28
		I	VDD_IO	U	2	UART1_RX
		B	VDD_IO	U	3	I2C1_SDA
32	XGPIO_L29	B	VDD_IO	U	0	GPIO_L29
		O	VDD_IO	U	2	UART1_TX
		B	VDD_IO	U	3	I2C1_SCL
33	ADAC_LP	AO	VDD_ADAC	NA	NA	NA
34	ADAC_VDDA	P	VDD_ADAC	NA	NA	NA
35	ADAC_RP	AO	VDD_ADAC	NA	NA	NA
36	VDD_IO	P	NA	NA	NA	NA
37	XGPIO_B2	B	VDD_IO	U	0	GPIO_B2
		O	VDD_IO	U	1	PWM_1
		B	VDD_IO	U	3	I2C2_SDA
		O	VDD_IO	U	4	SPDIF_O
		O	VDD_IO	U	5	PRGB_DE
		B	VDD_IO	U	7	I2S_LRCK
38	XGPIO_B3	B	VDD_IO	U	0	GPIO_B3
		O	VDD_IO	U	1	PWM_1
		B	VDD_IO	U	3	I2C2_SCL
		I	VDD_IO	U	4	IR
		O	VDD_IO	U	5	PRGB_R0
		B	VDD_IO	U	7	I2S_DATAI
39	VDD_CORE	P	NA	NA	NA	NA
40	D3_DQ9 /D2_DQ14	B	DDR_VDDQ	NA	NA	NA
41	D3_DQ11 /D2_DQ12	B	DDR_VDDQ	NA	NA	NA
42	D3_DM1 /D2_DQM1	O	DDR_VDDQ	NA	NA	NA
43	D3_DQ13 /D2_DQ9	B	DDR_VDDQ	NA	NA	NA
44	D3_DQ15 /D2_DQ11	B	DDR_VDDQ	NA	NA	NA
45	DDR_VDDQ	P	NA	NA	NA	NA
46	D3_DQS1	B	DDR_VDDQ	NA	NA	NA

	/D2_DQS1					
47	D3_DQSB1 /D2_DQSB1	B	DDR_VDDQ	NA	NA	NA
48	D3_DQ8 /D2_DQ15	B	DDR_VDDQ	NA	NA	NA
49	DDR_VDDQ	P	NA	NA	NA	NA
50	D3_DQ10 /D2_DQ8	B	DDR_VDDQ	NA	NA	NA
51	D3_DQ14 /D2_DQ10	B	DDR_VDDQ	NA	NA	NA
52	D3_DQ12 /D2_DQ13	B	DDR_VDDQ	NA	NA	NA
53	DDR_VDDQ	P	NA	NA	NA	NA
54	D3_DQ0 /D2_DQ6	B	DDR_VDDQ	NA	NA	NA
55	D3_DQ2 /D2_DQ1	B	DDR_VDDQ	NA	NA	NA
56	D3_DQS0 /D2_DQS0	B	DDR_VDDQ	NA	NA	NA
57	D3_DQSB0 /D2_DQSB0	B	DDR_VDDQ	NA	NA	NA
58	DDR_VDDC	P	NA	NA	NA	NA
59	D3_DM0 /D2_DQM0	O	DDR_VDDQ	NA	NA	NA
60	D3_DQ6 /D2_DQ4	B	DDR_VDDQ	NA	NA	NA
61	D3_DQ4 /D2_DQ3	B	DDR_VDDQ	NA	NA	NA
62	D3_DQ3 /D2_DQ7	B	DDR_VDDQ	NA	NA	NA
63	D3_DQ1 /D2_DQ0	B	DDR_VDDQ	NA	NA	NA
64	DDR_VDDQ	P	NA	NA	NA	NA
65	D3_DQ5 /D2_DQ2	B	DDR_VDDQ	NA	NA	NA
66	D3_DQ7 /D2_DQ5	B	DDR_VDDQ	NA	NA	NA
67	DDR_PLLVCCA	P	NA	NA	NA	NA
68	DDR_VDDQ	P	NA	NA	NA	NA
69	D3_CK /D2_CK	O	DDR_VDDQ	NA	NA	NA
70	D3_CKB /D2_CKB	O	DDR_VDDQ	NA	NA	NA

71	D3_B1 /D2_ODT	O	DDR_VDDQ	NA	NA	NA
72	D3_A12 /D2_RASB	O	DDR_VDDQ	NA	NA	NA
73	D3_A4 /D2_CASB	O	DDR_VDDQ	NA	NA	NA
74	D3_A6 /D2_A0	O	DDR_VDDQ	NA	NA	NA
75	D3_A8 /D2_A2	O	DDR_VDDQ	NA	NA	NA
76	D3_A1 /D2_A4	O	DDR_VDDQ	NA	NA	NA
77	D3_A11 /D2_A6	O	DDR_VDDQ	NA	NA	NA
78	DDR_VDDQ	P	NA	NA	NA	NA
79	D3_A10 /D2_A8	O	DDR_VDDQ	NA	NA	NA
80	D3_B2 /D2_A11	O	DDR_VDDQ	NA	NA	NA
81	D3_A0 /D2_WEB	O	DDR_VDDQ	NA	NA	NA
82	DDR_VDDC	P	DDR_VDDQ	NA	NA	NA
83	D3_A2 /D2_BA0	O	DDR_VDDQ	NA	NA	NA
84	D3_A9 /D2_BA1	O	DDR_VDDQ	NA	NA	NA
85	D3_A13 / NA	O	DDR_VDDQ	NA	NA	NA
86	D3_RESETN /NA	O	DDR_VDDQ	NA	NA	NA
87	DDR_VDDQ	P	NA	NA	NA	NA
88	D3_CKE /D2_CKE	O	DDR_VDDQ	NA	NA	NA
89	D3_A7 /D2_A1	O	DDR_VDDQ	NA	NA	NA
90	D3_A5 /D2_A10	O	DDR_VDDQ	NA	NA	NA
91	D3_A3 /D2_A5	O	DDR_VDDQ	NA	NA	NA
92	D3_B0 /D2_A3	O	DDR_VDDQ	NA	NA	NA
93	D3_WEB /D2_A9	O	DDR_VDDQ	NA	NA	NA

94	D3_CASB /D2_A7	O	DDR_VDDQ	NA	NA	NA
95	D3_ODT /D2_A12	O	DDR_VDDQ	NA	NA	NA
96	D3_RASB /D2_BA2	O	DDR_VDDQ	NA	NA	NA
97	XGPIO_R5	B	VDD_IO	U	0	GPIO_R5
		O	VDD_IO	U	1	PWM_2
		I	VDD_IO	U	2	UART2_RX
		B	VDD_IO	U	3	I2C2_SDA
		O	VDD_IO	U	5	PRGB_R5
98	VDD_IO	P	NA	NA	NA	NA
99	XGPIO_R8	B	VDD_IO	U	0	GPIO_R8
		O	VDD_IO	U	2	UART2_TX
		B	VDD_IO	U	3	I2C2_SCL
		O	VDD_IO	U	5	PRGB_G0
		O	VDD_IO	U	6	PRGB_R0
		O	VDD_IO	U	7	PRGB_G1
		O	VDD_IO	U	8	UART2_TX
100	XGPIO_T0	B	VDD_IO	U	0	GPIO_T0
		O	VDD_IO	U	3	TVE_HSYNC
		B	VDD_IO	U	4	SDIO_D1
		O	VDD_IO	U	5	PRGB_G1
		O	VDD_IO	U	6	PRGB_R1
		O	VDD_IO	U	7	PRGB_G3
		O	VDD_IO	U	8	UART2_RX
101	XGPIO_T1	B	VDD_IO	U	0	GPIO_T1
		O	VDD_IO	U	3	TVE_VSYNC
		B	VDD_IO	U	4	SDIO_D0
		O	VDD_IO	U	5	PRGB_G2
		O	VDD_IO	U	6	PRGB_R2
		O	VDD_IO	U	7	PRGB_G0
		O	VDD_IO	U	8	UART2_RX
102	XGPIO_T2	B	VDD_IO	U	0	GPIO_T2
		I	VDD_IO	U	2	UART2_RX
		B	VDD_IO	U	3	I2C3_SCL
		B	VDD_IO	U	4	SDIO_CLK
		O	VDD_IO	U	5	PRGB_G3
		O	VDD_IO	U	6	PRGB_R3
		O	VDD_IO	U	7	PRGB_G4
103	XGPIO_T3	B	VDD_IO	U	0	GPIO_T3
		O	VDD_IO	U	2	UART2_TX

		B	VDD_IO	U	3	I2C3_SDA
		B	VDD_IO	U	4	SDIO_CMD
		O	VDD_IO	U	5	PRGB_G4
		O	VDD_IO	U	6	PRGB_R4
		O	VDD_IO	U	7	PRGB_G2
104	XGPIO_T4	B	VDD_IO	Z	0	GPIO_T4
		I	VDD_IO	Z	1	SSI_MID
		B	VDD_IO	Z	4	SDIO_D3
		O	VDD_IO	Z	5	PRGB_G5
		O	VDD_IO	Z	6	PRGB_R5
		O	VDD_IO	Z	7	PRGB_G6
105	XGPIO_T5	B	VDD_IO	Z	0	GPIO_T5
		I	VDD_IO	Z	1	SSI_MICLK
		B	VDD_IO	Z	4	SDIO_D2
		O	VDD_IO	Z	5	PRGB_G6
		O	VDD_IO	Z	6	PRGB_R6
		O	VDD_IO	Z	7	PRGB_G5
106	XGPIO_T6	B	VDD_IO	U	0	GPIO_T6
		I	VDD_IO	U	1	SSI_MIVLD
		B	VDD_IO	U	3	I2C2_SCL
		O	VDD_IO	U	5	PRGB_G7
		O	VDD_IO	U	6	PRGB_R7
107	XGPIO_T7	B	VDD_IO	U	0	GPIO_T7
		I	VDD_IO	U	1	SSI_MISYNC
		B	VDD_IO	U	3	I2C2_SDA
		O	VDD_IO	U	5	PRGB_B0
		O	VDD_IO	U	6	PRGB_G0
		B	VDD_IO	U	8	I2C2_SDA
108	XGPIO_T8	B	VDD_IO	U	0	GPIO_T8
		I	VDD_IO	U	1	SSI_MID
		I	VDD_IO	U	2	I2S_DATAI
		I	VDD_IO	U	3	EJ_TRSTJ
		B	VDD_IO	U	4	SDIO_D1
		O	VDD_IO	U	5	PRGB_B1
		O	VDD_IO	U	6	PRGB_G1
		B	VDD_IO	U	8	I2C2_SCL
109	XGPIO_T9	B	VDD_IO	U	0	GPIO_T9
		I	VDD_IO	U	1	SSI_MICLK
		B	VDD_IO	U	2	I2S_LRCK
		I	VDD_IO	U	3	EJ_TDI
		B	VDD_IO	U	4	SDIO_D0
		O	VDD_IO	U	5	PRGB_B2

		O	VDD_IO	U	6	PRGB_G2
110	XGPIO_T10	B	VDD_IO	U	0	GPIO_T10
		I	VDD_IO	U	1	SSI_MIVLD
		B	VDD_IO	U	2	I2S_BCLK
		O	VDD_IO	U	3	EJ_TDO
		B	VDD_IO	U	4	SDIO_CLK
		O	VDD_IO	U	5	PRGB_B3
		O	VDD_IO	U	6	PRGB_G3
111	XGPIO_T11	B	VDD_IO	U	0	GPIO_T11
		I	VDD_IO	U	1	SSI_MISYNC
		B	VDD_IO	U	2	I2S_MCLK
		I	VDD_IO	U	3	EJ_TMS
		B	VDD_IO	U	4	SDIO_CMD
		O	VDD_IO	U	5	PRGB_B4
		O	VDD_IO	U	6	PRGB_G4
112	XGPIO_T12	B	VDD_IO	U	0	GPIO_T12
		O	VDD_IO	U	1	PWM_2
		O	VDD_IO	U	2	I2S_DATAO
		I	VDD_IO	U	3	EJ_TCLK
		B	VDD_IO	U	4	SDIO_D3
		O	VDD_IO	U	5	PRGB_B5
		O	VDD_IO	U	6	PRGB_G5
113	XGPIO_T13	B	VDD_IO	D	0	GPIO_T13
		O	VDD_IO	D	5	PRGB_B6
		O	VDD_IO	D	6	PRGB_G6
114	XGPIO_T14	B	VDD_IO	U	0	GPIO_T14
		I	VDD_IO	U	2	UART2_RX
		B	VDD_IO	U	3	I2C3_SDA
		O	VDD_IO	U	5	PRGB_B7
		O	VDD_IO	U	6	PRGB_G7
115	XGPIO_T15	B	VDD_IO	U	0	GPIO_T15
		O	VDD_IO	U	1	PWM_2
		O	VDD_IO	U	2	UART2_TX
		B	VDD_IO	U	3	I2C3_SCL
		O	VDD_IO	U	5	PRGB_CLK
		O	VDD_IO	U	6	PRGB_B0
		B	VDD_IO	U	8	I2C3_SDA
116	VDDC_PLL	P	NA	NA	NA	NA
117	XP_X27MOUT	AO	VDD_PLL	NA	NA	NA
118	XP_X27MIN	AI	VDD_PLL	NA	NA	NA
119	VDD_PLL	P	NA	NA	NA	NA
120	XADC8B_IN	AI	USB_VDD3P3	NA	NA	NA

121	USB_VDD3P3	P	NA	NA	NA	NA
122	USB1_PN	A	USB_VDD3P3	NA	NA	NA
123	USB1_PP	A	USB_VDD3P3	NA	NA	NA
124	USB_VDD1P1	P	NA	NA	NA	NA
125	USB0_PN	A	USB_VDD3P3	NA	NA	NA
126	USB0_PP	A	USB_VDD3P3	NA	NA	NA
127	USB0_VBUS	A	USB_VDD3P3	NA	NA	NA
128	USB0_ID	A	USB_VDD3P3	NA	NA	NA

Table 4-1 Pin Characteristics

4.2 Signal Descriptions

B200 contains many peripheral interfaces, following table shows detailed function description of every signal:

- Signal Name : the signal name of every signal
- Descriptions : the detailed function description of every signal
- Type : Denote the signal direction
  - I -> input
  - O->output
  - B->input/output
  - A->Analog
  - AI->Analog input
  - AO->Analog output
  - P->power
  - G->ground

Signal Name	Descriptions	Type
power		
VDD_IO	Digital IO Power	P
VDD_CORE	Digital Core Power	P
ADAC_VDDA	Audio DAC Power	P
DDR_VDDQ	DDR IO Power	P
DDR_VDDC	DDR Core Power	P
DDR_PLLVCCA	DDR PLL Power	P
VDD_PLL	PLL IO Power	P
VDDC_PLL	PLL Core Power	P
USB_VDD3P3	USB IO Power	P
USB_VDD1P1	USB Core Power	P
Oscillator		
XP_X27MOUT	Clock output of 27MHZ crystal	AO
XP_X27MIN	Clock input of 27MHZ crystal	AI

System Reset		
XP_CRSTJ	Reset signal, low active	I
EJTAG Debug		
EJ_TCLK	EJTAG clock signal	I
EJ_TRSTJ	EJTAG reset signal , low active	I
EJ_TMS	EJTAG mode select signal	I
EJ_TDI	EJTAG data input signal	I
EJ_TDO	EJTAG data output signal	O
DDR		
Dx_CK	Active high clock signal to DDR memory	O
Dx_CKB	Active low clock signal to DDR memory	O
Dx_CKE	Active high clock enable signal to DDR memory	O
Dx_RASB	Active low row address strobe to DDR memory	O
Dx_CASB	Active low column address strobe to DDR memory	O
Dx_WEB	Active low write enable strobe to DDR memory	O
Dx_ODT	On die termination output signal	O
Dx_RESETN	Reset signal to DDR memory	O
Dx_DM0	Active low data mask signal to DDR memory	O
Dx_DM1	Active low data mask signal to DDR memory	O
Dx_DQS0	Active high bidirectional data strobes to DDR memory	B
Dx_DQSB0	Active low bidirectional data strobes to DDR memory	B
Dx_DQS1	Active high bidirectional data strobes to DDR memory	B
Dx_DQSB1	Active low bidirectional data strobes to DDR memory	B
Dx_BA0	Bank address signal to DDR memory	O
Dx_BA1	Bank address signal to DDR memory	O
Dx_BA2	Bank address signal to DDR memory	O
Dx_Ai (i=0~13)	Address signal to DDR memory	O
Dx_DQi (i=0~15)	Bidirectional data signal to DDR memory	B
USB2.0		
USB0_PN	USB2.0 OTG Data Signal DM	AB
USB0_PP	USB2.0 OTG Data Signal DP	AB
USB0_VBUS	USB2.0 OTG 5V power supply	P
USB0_ID	USB2.0 OTG ID indicator	AI
USB1_PN	USB2.0 Data Signal DM	AB
USB1_PP	USB2.0 Data Signal DP	AB
SAR-ADC8B		
XADC8B_IN	SAR 8BT ADC INPUT	AI
ADAC		

ADAC_LP	Audio DAC left channel output	AO
ADAC_RP	Audio DAC right channel output	AO
SPI FLASH		
SF_CLK	SPI Serial clock	O
SF_CSJ0	SPI chip select signal 0 , low active	O
SF_CSJ1	SPI chip select signal 1 , low active	O
SF_MISO	SPI Serial data input	I
SF_MOSI	SPI Serial data output	O
SDIO		
SDIO_CLK	Clock signal for SDIO	O
SDIO_CMD	Command signal for SDIO	B
SDIO_D0	Data input and output for SDIO	B
SDIO_D1	Data input and output for SDIO	B
SDIO_D2	Data input and output for SDIO	B
SDIO_D3	Data input and output for SDIO	B
TSC		
SSI_MICLK	Transport stream clock	I
SSI_MISYNC	Transport stream sync	I
SSI_MIVLD	Transport stream data valid	I
SSI_MID	Transport stream input data	I
UART		
UART1_TX	UART 1 Data Transmit	O
UART1_RX	UART 1 Data Receive	I
UART2_TX	UART 2 Data Transmit	O
UART2_RX	UART 2 Data Receive	I
I2C		
I2C1_SCL	I2C 1 Clock Signal	B
I2C1_SDA	I2c 1 Data Signal	B
I2C2_SCL	I2C 2 Clock Signal	B
I2C2_SDA	I2c 2 Data Signal	B
I2C3_SCL	I2C 3 Clock Signal	B
I2C3_SDA	I2c 3 Data Signal	B
IR		
IR	IR receive data	I
PWM		
PWM_0	Pulse Width Modulation output	O
PWM_1	Pulse Width Modulation output	O
PWM_2	Pulse Width Modulation output	O
SPDIF		
SPDIF_O	SPDIF output signal	O
I2S		
I2S_MCLK	I2S source clock	B

I2S_BCLK	I2S serial clock	B
I2S_LRCK	I2S left & right channel signal	B
I2S_DATAI	I2S serial data input	I
I2S_DATAO	I2S serial data output	O
Video IN		
VIN_CLK	Video input clock signal	I
VIN_HSYNC	Video HSYNC input signal or Video Active input signal	I
VIN_VSYNC	Video VSYNC input signal	I
VIN_DATA7	Video input data bits	I
VIN_DATA6	Video input data bits	I
VIN_DATA5	Video input data bits	I
VIN_DATA4	Video input data bits	I
VIN_DATA3	Video input data bits	I
VIN_DATA2	Video input data bits	I
VIN_DATA1	Video input data bits	I
VIN_DATA0	Video input data bits	I
PRGB output		
PRGB_CLK	RGB clock signal	O
PRGB_DE	RGB data active signal	O
PRGB_HSYNC	RGB HSYNC signal	O
PRGB_VSYNC	RGB VSYNC signal	O
PRGB_R0~PRGB_R7	RGB red component data	O
PRGB_G0~PRGB_G7	RGB green component data	O
PRGB_B0~PRGB_B7	RGB blue component data	O

Table 4-2 Signal Descriptions

5 Electrical characteristics

5.1 DC characteristics

Table 5-1 summarizes the DC electrical characteristics with below condition as

- VDDP-VSSP = 3.3V ±5%
- Ta = 25°C
- Crystal frequency is XP_XIN = 27MHz

item	Descriptions	Condition	Min.	Typ.	Max.	Unit
VDD_IO	Digital IO Power		2.97	3.3	3.7	V

item	Descriptions	Condition	Min.	Typ.	Max.	Unit
VDD_CORE	Digital Core Power		1.05	1.1	1.21	V
VDD_VDDQ	DDR2 IO Power		1.62	1.8	1.98	V
VDD_VDDQ	DDR3 IO Power		1.35	1.5	1.65	V
VDD_VDDC	DDR Core Power		1.05	1.1	1.21	V
DDR_PLLVCCA	DDR PLL Power		2.97	3.3	3.7	V
VDD_PLL	PLL IO Power		2.97	3.3	3.7	V
VDDC_PLL	PLL Core Power		1.05	1.1	1.21	V
USB_VDD3P3	USB IO Power		2.97	3.3	3.7	V
USB_VDD1P1	USB Core Power		1.05	1.1	1.21	V
Idd_1.1V	Operating Supply Current, for all VDD=1.1V			270		mA
Idd_3.3V	Operating Supply Current, for all VDD=3.3V			30		mA
Idd_1.8V	Operating Supply Current, for all VDD=1.8V			260		mA
Pd	Power Dissipation	Include DDR		0.9		W
VOL	Output Voltage Low				0.4	V
VOH	Output Voltage High		2.4			V
VIH	Input Voltage High		2.7		5.0	V
VIL	Input Voltage Low		-0.3		0.7	V

Table 5-1 - DC Electrical Characteristics

5.2 Power up and Power down sequence

The power up and power down sequence needs to be followed to avoid power up crash and latch up during power down. The signals involved in this sequence are:

- VDDIO
- VDDCORE
- XP_CRST# (CPU reset signal)

Figure 5. illustrates the power up and power down timing sequence with the support of **Table 5-2**

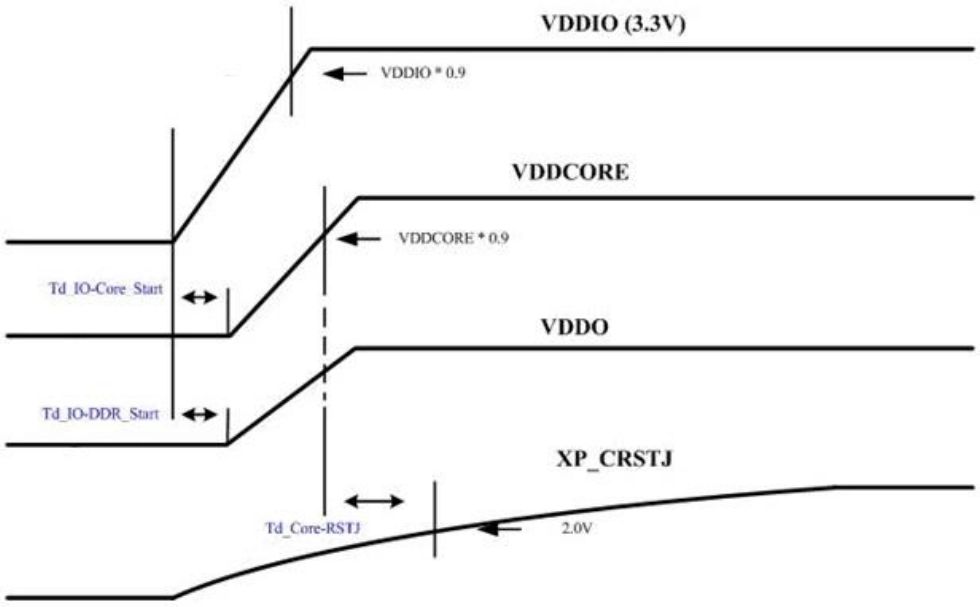


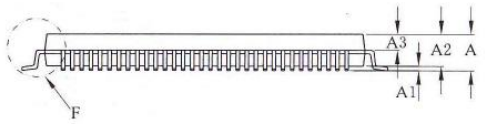
Figure 5.2 - Power up and Power down Sequence

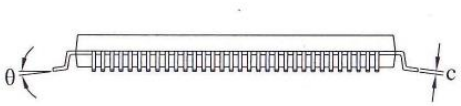
Name	Description	Value			Unit
		Min.	Typ.	Max.	
Td_IO-C_Start	Distance from IO power start rise to core power start rise	0		N/A	ms
Td_IO-DDR_Start	Distance from IO power start rise to DDR power start rise	0		N/A	ms
Td_Core-RSTJ	Distance from CPU core power stable to cold reset rise up to 2.0V	5			ms

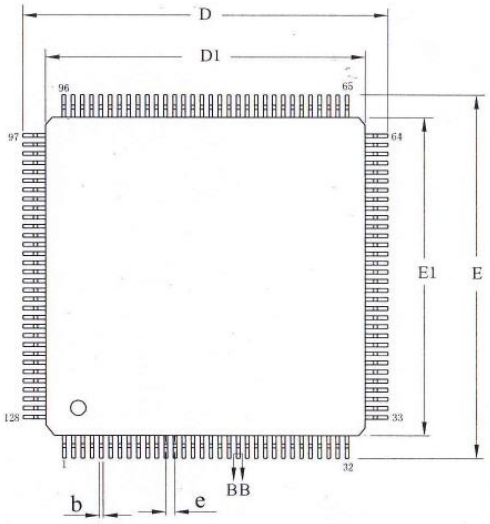
Table 5-2 - Power up and Power down Sequence Parameters

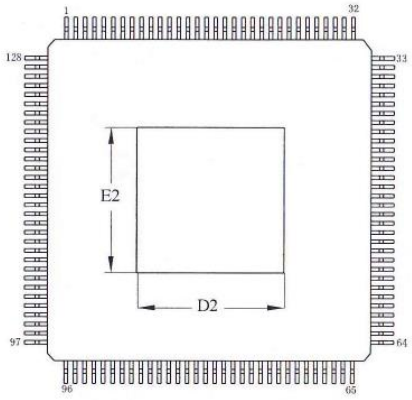
6 Package Characteristics

The package for B200 is eLQFP128 (14mmx14mmx1.4mm)

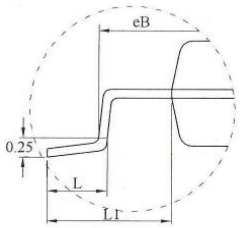




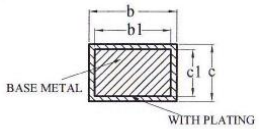




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	—	15.35
e	0.40BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°



DETAIL: F



SECTION B-B

L/F Size (mil) \ Size (mm)	D2	E2
218*218	4.95REF	4.95REF