2.2.2.1 The List of Inputs

16 bit integer input inputA (the first number in any addition, subtraction, multiplication, division, modulo operation)

16 bit integer input inputB (the second number in any operation)

4 bit integer input op_code (0000 means the operation to output is addition, 1000 means the operation to output is subtraction, 0100 means the operation to output is multiplication, 0010 means the operation to output is division, 0001 means the operation to output is modulo)

2.2.2.2 The List of Outputs

32 bit integer output R (result of the chosen operation, where all operations excluding multiplication use the most significant resulting bit and repeat it 16 times to properly cover the additional lines)

2 bit integer output E (the most significant bit is 1 when either division or modulo are chosen and inputB=0; the least significant bit is 1 when addition or subtraction are chosen and the overflow error is given by the AddSub module)

2.2.2.3 The List of Interfaces

The wires in inputB are ORed together to make a bit that is 1 if inputB is non-zero, then that bit connects to a NOT gate (thus the result is true if 0), which has its result connect to an AND gate where the second input is the result of the two least significant bits of the input op_code being ORed together (one of them will be true if either division or modulo is chosen); this AND gate then becomes the most significant bit of output E. Identifier for this operation is: “divZero”

The wires in op_code are connected to an OR gate, where the resulting bit connect to a not gate (thus 1 if addition is chosen), which itself then connects to an OR gate where the second

input is the most significant bit of op_code (which is 1 if subtraction is chosen), and that OR gate connects its result to an AND gate whose other input is the error result of the AddSub module, and the result of that AND gate becomes the least significant bit of output E. Identifier for this operation is: “overflow” (appears as an inline calculation after the “error” overflow goes from AddSub).

inputA is connected to the first input of the AddSub module. Identifier: “inputA”

inputB is connected to the second input of the AddSub module. Identifier: “inputB”

The most significant bit of op_code is connected to the mode bit of the AddSub module. Identifier: “mode”

inputA is connected to the first input of the multiply module. Identifier: “inputA”

inputB is connected to the second input of the multiply module. Identifier: “inputB”

inputA is connected to the first input of the divide module. Identifier: “inputA”

inputB is connected to the second input of the divide module. Identifier: “inputB”

inputA is connected to the first input of the modulo module. Identifier: “inputA”

inputB is connected to the second input of the modulo module. Identifier: “inputB”

The most significant bit of the result of the AddSub module is copied onto 16 more wires to make the output of AddSub be 32 bits. Identifier: n/a (happens all within module)

The most significant bit of the result of the divide module is copied onto 16 more wires to make the output of divide be 32 bits. Identifier: n/a (happens all within module)

The most significant bit of the result of the modulo module is copied onto 16 more wires to make the output of modulo be 32 bits. Identifier: n/a (happens all within module)

The altered result of the AddSub module (above) is copied onto both the 0000 (0 base 10) and 1000 (8 base 10) locations of the multiplexor. Identifier: “sum”

The result of the multiply module is copied onto the 0100 (4 base 10) location of the multiplexor. Identifier: “res”

The altered result of the divide module (above) is copied onto the 0010 (2 base 10) location of the multiplexor. Identifier: “resDiv”

The altered result of the modulo module (above) is copied onto the 0001 (1 base 10) location of the multiplexor. Identifier: “resMod”

op_code connects to the 4 to 16 (one-hot) decoder. Identifier: “encode”

The decoder connects its 16 bit result to the control of the multiplexor. Identifier: “decode”

The multiplexor connects the result allowed to pass through it to output R. Identifier: “R”

2.2.2.4 The List of Parts

divZero (OR gate, NOT gate, AND gate, second OR gate)

overflow (OR gate, NOT gate, second OR gate, AND gate)

AddSub (the adder-subtractor module)

multiply (the multiplication module)

divide (the division module)

modulo (the modulo module)

Dec4x16 (the 4 to 16 one-hot decoder)

Mux (the 16 choice by 32 bit input with 32 bit output multiplexor)

2.2.2.5 The Top Level circuit diagram