CS 4341 Fall 2021

Project, Part 2 Worklog

Work Log with Peer Participation

The Journal:

Date	**Task**	**Who**
October 6	started working on AddSub	Srivatsan Srirangam
October 8	worked on the list of inputs/outputs/interfaces/circuit diagram	Evan Nibbe
October 9	worked on the circuit diagram, began updating project part 1, and started working on verilog code	Evan Nibbe
October 10	Managed to get Add and sub working on verilog	Evan Nibbe
October 11	began working on the multiplier code/made updates to project part1	Edilberto Carrizales, Evan Nibbe
October 11	Created divide and modulo modules, sent via WhatsApp	Srivatsan Srirangam
October 11	Debugging issue with multiplier shifting	Evan Nibbe, Edilberto Carrizales
October 11	Solved multiplier issue and began working on the multiplexor module	Evan Nibbe

October 13	Debugging verilog subtraction issue/formatted the verilog code output	Edilberto Carrizales
October 13	Solved problem with negative number subtraction	Evan Nibbe
October 13	Debugging problem with multiplexer and large numbers	Evan Nibbe, Edilberto Carrizales
October 13	Updated the circuit diagram	Evan Nibbe

Affirmation:

Evan had addition and subtraction working on verilog on October 10
Edilberto had addition and subtraction working on verilog on October 11
Evan had the full verilog code running on October 13th
Edilberto had the full verilog code running on October 13th.
Srivatsan Srirangam had the full verilog code running on October 13th