Name: Ruoyan Wu RCS ID: wwr7 @rpi.edu

# ⊗ ⊗ CSCI 2500 — Computer Organization ⊗ ⊗
## Fall 2018 Quiz 6 (November 30, 2018)

Please silence and put away all laptops, notes, books, phones, electronic devices, etc. This quiz is designed to take 25 minutes; therefore, for 50% extra time, the expected time is 38 minutes and 100% extra time is 50 minutes. Questions will not be answered except when there is a glaring mistake or ambiguity in a question. Please do your best to interpret and answer each question.

1. **(24 POINTS)** We've focused quite a bit on the five-stage pipeline, which includes the `IF`, `ID`, `EX`, `MEM`, and `WB` stages. Using the notation of Homework 5 and the Project, show all cycles for all instructions of the following code snippet when there is no forwarding. This is equivalent to showing the output from the last iteration of Homework 5 or the Project.

```
add $a0,$s0,$s0
lw $s0,64($a0)
add $a0,$s0,$s0
```

| Instruction | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| add $a0, $s0, $s0 | IF | ID | EX | MEM | WB | | | | | | | | |
| nop | | IF | ID | * | * | * | | | | | | | |
| nop | | IF | ID | * | * | * | | | | | | | |
| lw $s0, 64($a0) | | IF | ID | ID | ID | EX | MEM | WB | | | | | |
| nop | | | IF | IF | IF | ID | * | * | * | | | | |
| nop | | | IF | IF | IF | ID | * | * | * | | | | |
| add $a0, $s0, $s0 | | | IF | IF | IF | ID | ID | ID | EX | MEM | WB | | |
| | | | | | | | | | | | | | |

2. **(20 POINTS)** Assuming there is no forwarding, consider the instructions below:

```
lw $t0,0($s0)
add $t0,$t0,$s0
sw $t0,0($s0)
lw $t1,4($s0)
add $t1,$t1,$s1
sw $t1,4($s0)
```

```
lw $t0, 0($s0)
lw $t1, 4($s1)
add $t0, $t0, $s0
add $t1, $t1, $s1
sw $t0, 0($s0)
sw $t1, 4($s0)
```

In the space to the above-right, show a valid reordering of instructions that optimally reduces the number of hazards.

3. **(12 POINTS)** Again for a five-stage pipeline, consider a modified implementation that combines the IF and ID stages into a single pipeline stage labeled IFD that takes one-and-a-half clock cycles (i.e., $1.5 \times T_c$). Describe in one or two sentences how this will impact pipeline speedup.

Combines the IF and ID stages into a single pipeline stage. Will shorten the cycle and faster the pipeline.

4. **(12 POINTS)** Consider the following three branch prediction schemes: (1) predict not taken; (2) predict taken; and (3) dynamic prediction with an accuracy of 90%. Assume that each scheme has zero penalty when the prediction is correct and a 2-cycle penalty when the prediction is incorrect.

   (a) Which scheme is the best choice for a branch that is taken with 95% frequency?

   (1) predict not taken.

   (b) Which scheme is the best choice for a branch that is taken with 70% frequency?

   (3) dynamic prediction with an accuracy of 90%

5. **(16 POINTS)** Given a 32-bit architecture with a 5-bit index, consider an 8-way associative cache with a 2-word block size. What is the tag and index for address `0xbad1beef`? Present each answer in hexadecimal.

tag = address bit length − exponent of index − exponent of offset

= 32 − 5 − 16 = 11

index = 5

2 words = $2^1$

6. **(16 POINTS)** Consider a scenario in which die size constraints limited CPU designers to only 16K bits (i.e., 16,384 bits, not bytes) of space left for the on-chip cache. Given that you want the cache to be 4-way associative with a 4-word block size (and the machine word size is 32 bits), what is the maximum number of entries this cache can have? In other words, how large (in bits) can the index field be? Be sure to account for the tag and valid bits.

16K bits = $2^{14}$ words = 4096 words $\Rightarrow 2^{12} - 2^2 = 2^{10}$ blocks

4 words = $2^2$

tag = 32 − 10 − 2 − 4 bits = 16 bits

index = 8