CE2210, Sec. 3
Homework 5

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1. The Set and Reset signals shown below are applied to a NOR-based SR latch. Draw the output waveform $Q(t)$. Assume $Q(t)$ is initially 1.

2. The signals shown below are applied to a clocked NOR-based SR latch. Draw the output waveform. Assume $Q(t)$ is initially 1.

3. The data signal $D(t)$ shown below is applied to the input of a positive edge-triggered DFF. Draw the output $Q(t)$ for the device.

4. Redo the previous problem for the case where $D(t)$ is applied to the input of a negative edge-triggered DFF.

5. Consider the NAND-based SR latch. What are the outputs, Q and $\bar{Q}$, when both $S = 0$ and $R = 0$? Why is this "not used" case?

   When $S = 0$ and $R = 0$ the relationship between Q and $\bar{Q}$ would be wrong because they both would be 1.

6. An 8-bit shift register has the binary equivalent of the decimal number 46 stored in it. What are the base-10 equivalent contents of the register after the following operations have been performed?

   $46_{10} = 0010\ 1110_2$

   (a) SHR 1 = $0001\ 0111_2$
   (b) SHL 1 = $0101\ 1100_2$
   (c) SHR 2 = $0000\ 1011_2$
   (d) ROR 2 = $1000\ 1011_2$