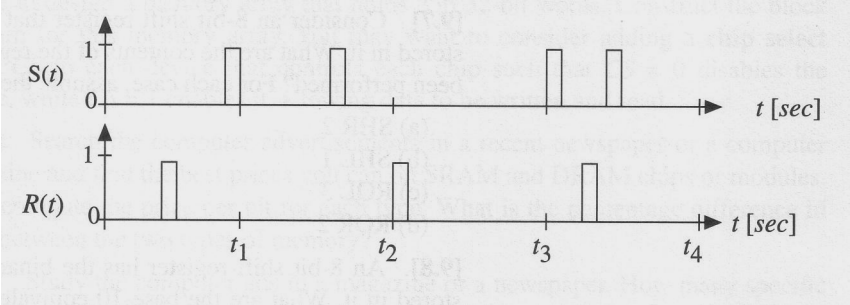
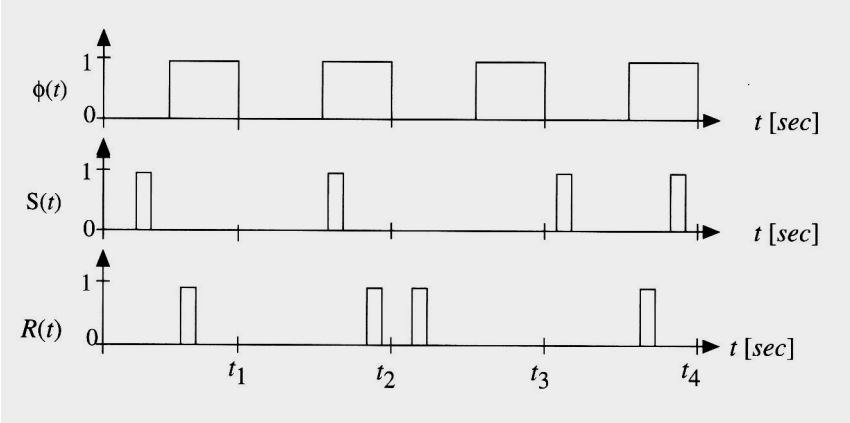
CpE2210 Homework Assignment #5 Maximum – 100pts

HW#5 is due at the beginning of class on Friday, Apr 12, 2019. You must always show or explain your work in a neat and orderly format. You are encouraged to discuss ideas with other students and consult references but your work must be your own.

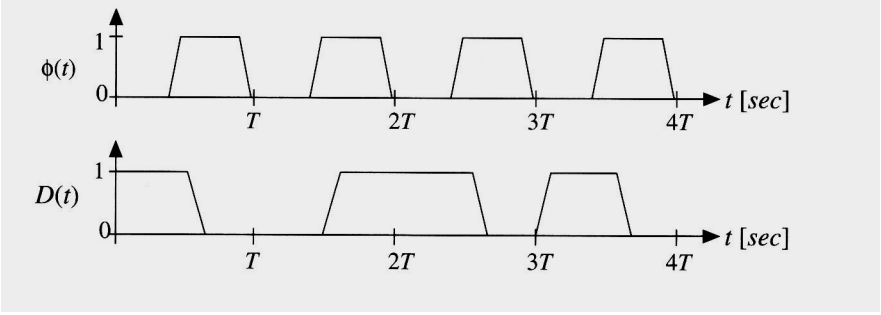
1. The Set and Reset signals shown below are applied to a NOR-based SR latch. Draw the output waveform Q(t). Assume Q(t) is initially 1. (Ignore all timing delays) [20pts]



2. The signals shown below are applied to a clocked NOR-based SR latch. Draw the output waveform. Assume Q(t) is initially 1. (Ignore all timing delays) [20pts]



3. The data signal D(t) shown below is applied to the input of a positive edge-triggered DFF. Draw the output Q(t) for the device. (Ignore all timing delays) [15pts]



4. Redo the previous problem for the case where D(t) is applied to the input of a negative edge-triggered DFF. [15pts]

5. Consider the NAND-based SR latch. What are the outputs, Q and $\overline{Q}$, when both S = 0 and R = 0? Why is this "not used" case? [15pts]

6. An 8-bit shift register has the binary equivalent of the decimal number 46 stored in it. What are the base-10 equivalent contents of the register after the following operations have been performed? For each case, assume the same initial state given. [15pts]

(a) SHR 1
(b) SHL 1
(c) SHR 2
(d) ROR 2