C-238, Hall-32
Yuquan Campus, Zhejiang University
Hangzhou, Zhejiang, China
yifanbao@zju.edu.cn | yfbaohangzhou@gmail.com
Webpage : https://evanfanbao.github.io
Github : https://github.com/evanfanbao
+86-188-8891-8270

Yifan Bao

Junior Undergraduate, Computer Science, Zhejiang University

Education

Chu Kochen Honors College, Zhejiang University, Zhejiang, China
Bachelor of Technology, Computer Science and Technology, *Jul' 18 - Jul' 22 (Expected)*
GPA: 3.89/4(89.18/100) (Overall)

Research Interests

Machine Learning, Computer Vision,
Programming Language, Side Channel Attacks

Awards & Achievements

Awarded the **2019-2020 third-class scholarship** of Zhejiang University
Awarded the **2018-2019 third-class scholarship** of Zhejiang University
Secured an **excellent conclusion** of **Student Research Training Program** of Zhejiang University, 2018-2019
Secured the **thrid prize** in University Students' Physics (Theory) Innovation Competition of Zhejiang Province, 2019.
Awarded the **Excellent volunteer** of fifth China College Students' 'Internet+' Innovation and Entrepreneurship Competition, 2019
Secured an **excellent conclusion** of **Student Quality Training Project** of Zhejiang University, 2018

Research Projects

Side Channel Attack on AI chips

Supervisor : Prof. Fan(Terry) Zhang *Mar '19 - May '20*

- Side Channel Attack(SCA) is an attack technique based on the **leakage of information** gained from computer system.
- Using power analysis(one category of SCA) to reverse engineer part of parameters and hyper-parameters of feedforward neural network designed for cat recognition task running on Xilink Zynq-7000S FPGA board.
- Using power analysis to reverse engineer the input binary image of convolutional neural network running designed for MNIST handwritten digit recognition task on Xilink zynq-7000s FPGA board.
- Designing protective strategies for the two experimental neural networks against potential attacks. Specifically, random masking and random shuffling.
- For more details, please drop me an email. I am more than thrilled to explain the awesome results I have got.

Clothing parsing algorithm design for virtual fitting

Supervisor : Prof. Mingli Song *July '20 - Oct '20*

- Serving as a research intern in Computer Vision and Video Analysis Laboratory Computer Vision and Video Analysis Laboratory, Alibaba-Zhejiang University Joint Research Institute of Frontier Technologies(AZFT).
- Customizing, modifying, integrating and improving the existing segmentation algorithms including Deeplab-v3+, CascadePSP, and PointRend for clothing parsing with Zeekit clothing dataset provided by Alibaba.

Datafree amalgamation for object detection

Supervisor : Prof. Mingli Song *Feb '21 - Present*

- Surveying object detection, knowledge distillation and knowledge amalgamation.
- Reimplementing DETR(DEtection TRansformer) in paper End-to-End Object Detection with Transformers

Course Projects

Mini-SQL in C++
Course : Database System | *Supervisor : Prof. Jianling Sun* *Mar '20 - Jun '20*

- Built a simple local relational database.
- Implemented features such as *creating, inserting, deleting, and indexing(using self-implemented B+ tree).*
- Data types supported: *int, float, and char(n).*

Skip List implementation and analysis
Course: Advanced Data structure and Algorithm Analysis | *Supervisor : Assoc Prof. Yang Yang*
Mar '20 - Jun '20

- A skip list is a data structure that is used for storing a sorted list of items with the help of hierarchy of linked lists that connect increasingly sparse subsequences of the items.
- Implemented the skip list data structure.
- Tested the actual performance of self-implemented skip list and compared it with the ideal one.
- Tested skip list performance under different going up probability and wrote a testing report.
- Github Link

STL allocator and memory pool
Course: Object Oriented Programming | *Supervisor:Weiwei XU* *Mar '20 - Jun '20*

- An allocator is used by standard library containers as a template parameter.
- Designed a memory pool to speed up the dynamic allocation of a large number of small blocks, and to reduce memory fragmentation.
- Replaced the default allocator with a new one that optimizes the memory allocation speed using memory pool, supporting arbitrary memory size allocation request.
- Github Link

Pipelined CPU for MIPS assembly language
Course : Computer Architecture | *Supervisor : Prof. Shuibing He* *Sept '20 - Jan '21*

- Implemented a pipelined CPU in Verilog based on MIPS R10K architecture with Xilink Kintex 7 FPGA board
- Implemented memory hierarchy(a.k.a, cache design compatible with the CPU and memory)
- Implement stall, forwarding, multiple instruction issue and commit, precise interrupts and branch-misprediction rollback.
- Github Link

Computer Skills

Languages: Java(Proficient), Python(Advanced), C/C++(Advanced), Shell(Familiar), LaTeX
Research Tools: PyTorch(Competent)

Extra Interests

Hobbies: Competitive Programming, Jogging(Marathon), Pingpong, Swimming, Mountain Climbing, Photography,