

## ECE486/586 Homework No. 3

Due date: 05/14/2015

### Problem No. 1 (12 points)

We begin with a processor implemented in single-cycle implementation. When we attempt to split the processor functionality into multiple pipeline stages, the different stages do not require exactly the same amount of time. Assume that the original single-cycle processor had a clock period of 7 ns. After the stages were split, the measured times were: IF 1.2 ns; ID 1.8 ns; EX 1.4 ns; MEM 1.8 ns, WB 0.8 ns. The pipeline register delay is 0.2 ns.

- (a) **(4 points)** What is the clock rate for the 5-stage pipelined processor?
- (b) **(4 points)** Assume that the pipelined processor needs to incur a 2-cycle stall once every 6 instructions. What is the CPI for the pipelined processor?
- (c) **(4 points)** What is the speedup of the pipelined processor over the original single-cycle processor?

### Problem No. 2 (24 points)

Consider the following instruction sequence executing on the 5-stage MIPS pipeline.

```
LOAD  R1, #12(R2)
ADD   R2, R1, R3
SUB   R3, R2, R4
STORE R5, #16(R1)
```

- (a) **(6 points)** Identify all data dependences (by instruction pair and register involved) and their type (RAW, WAR or WAW):

1st Instruction	2 <sup>nd</sup> Instruction	Register	Type of Dependence

- (b) **(7 points)** Draw a pipeline execution diagram (similar to the bottom half of Figure C.10) for the above instruction sequence, showing the flow of instructions through the pipeline during each clock cycle. Indicate any necessary stalls on the pipeline diagram.
- (c) **(7 points)** Now, assume that all possible forwarding paths have been added to the pipeline. Redraw the pipeline execution diagram, indicating operand forwarding by arrows.
- (d) **(4 points)** Compared with non-pipelined execution, how much speedup is achieved by the pipelined processor: (i) without forwarding, and (ii) with forwarding?

### **Problem No. 3 (10 points)**

In this problem, we will explore how deepening the pipeline affects performance in two ways: faster clock cycle and increased stalls due to control hazards. Consider two pipelined processors: the first is a 5-stage pipeline with a 2 ns clock cycle and the second is a 12-stage pipeline with a 1 ns clock cycle. Assume that branches constitute 15% of the instructions and the branch misprediction rate for both processors is 10%. The branch misprediction penalty is 2 cycles for the 5-stage processor and 5 cycles for the 12-stage processor. Assuming that branch mispredictions are the only source of pipeline stalls, what is the speedup of the 12-stage pipeline over the 5-stage pipeline?

### **Problem No. 4 (22 points)**

In this problem, we will explore a pipeline for a register-memory architecture. The architecture has two instruction formats: a register-register format and a register-memory format. There is a single-memory addressing mode (offset + base register).

Arithmetic operations can use any of the following two formats:

ALUop Rdest, Rsrc1, Rsrc2                      # register-register format

or

ALUop Rdest, MEM                                # register-memory format

where the ALUop is one of the following: *Add*, *Subtract*, *And*, *Or*. Rsrc1, Rsrc2 and Rdest are registers. MEM is a base register and offset pair. When a memory operand is used in an ALUop, Rdest serves as both a destination and source register. For example, ADD R1, #8(R2) implies  $R1 \leftarrow R1 + \text{MEM}[8 + R2]$ .

*Load* and *Store* instructions use only the register-memory format. *Branches* use a full compare of two registers and are PC relative.

Assume that this machine is pipelined so that a new instruction can be started every clock cycle in the absence of any stalls. The resulting pipeline structure is as follows:

Instruction	Cycle										
	1	2	3	4	5	6	7	8	9	10	11
1	IF	RF	ALU1	MEM	ALU2	WB					
2		IF	RF	ALU1	MEM	ALU2	WB				
3			IF	RF	ALU1	MEM	ALU2	WB			
4				IF	RF	ALU1	MEM	ALU2	WB		
5					IF	RF	ALU1	MEM	ALU2	WB	
6						IF	RF	ALU1	MEM	ALU2	WB

The first ALU stage (ALU1) is used for effective address calculation for memory accesses and branches. The second ALU stage (ALU2) is used for arithmetic operations and branch comparison. RF stage includes both instruction decoding and source register reads. Also assume that when a register read and

register write of the same register occur in the same clock cycle, write data is written in the first half cycle and the new contents of the register can be read in the second half of the cycle.

- (a) **(4 points)** Find the number of adders needed to avoid any structural hazards. Show a combination of instructions and pipe stages that justifies your answer. You need to give only one combination that maximizes the adder count.
- (b) **(9 points)** Show the pipeline execution diagram for the following instruction sequence: Identify any hazards or stalls, indicating the reason for each, and the number of stall cycles required. Assume that no forwarding/bypassing is implemented.

LOAD R1, #4(R2)  
ADD R1, #8(R3)  
STORE R4, #16(R5)  
SUB R2, R4, R5  
AND R6, R1, R2

- (c) **(9 points)** Describe any forwarding paths that would reduce or eliminate any stalls present above. Draw the pipeline execution diagram after the forwarding paths have been added to the pipeline. Indicate which stages forward to which stages and the impact on the number of stall cycles compared with the non-forwarding pipeline.

### **Problem No. 5 (8 points)**

Consider a 5-stage MIPS pipeline running at a clock speed of 2.4 GHz. Assume that load instructions constitute 25% of the dynamic instruction count and 30% of all the load instructions are immediately followed by dependent instructions. Also, assume that the pipeline employs full forwarding hardware and a branch predictor with 100% branch prediction accuracy. Calculate the instruction throughput in terms of billions of instructions per second.

### **Problem No. 6 (14 points)**

Read the following paper posted on the course website: *D. Papworth, "Tuning the Pentium Pro Microarchitecture", IEEE MICRO, April 1996*. Then, answer the following questions:

- (a) **(2 points)** According to the author, to justify its development a major new microarchitecture must improve performance by how much over the previous microarchitecture?
  - i. 1.2x to 1.5x
  - ii. 1.5x to 2.0x
  - iii. 2.0x to 2.5x
  - iv. More than 2.5x
- (b) **(2 points)** The graph of "delivered performance vs. clock frequency" was:
  - i. A smooth linear progression
  - ii. Parabolic with performance improving non-linearly and then gradually worsening
  - iii. A random walk
  - iv. Nearly smooth and linear with some dips
  - v. None of the above

- (c) **(2 points)** Which of the following constraints does the author cite as a challenge for the Pentium Pro design?
- i. Lack of design time
  - ii. Insufficient design resources
  - iii. Inability to control the software environment
  - iv. Reliability
  - v. Power consumption
- (d) **(3 points)** Why did the Pentium Pro designers build a performance simulator as one of their first activities during the design evolution process?
- (e) **(5 points)** Identify two trade-offs made by the design team that increased CPI (cycles per instruction). Why were these trade-offs made?