Exercise 2

1. Consider the circuit of Fig.1.1.

a) Using the simple model with $V_{Don} = 0.7\text{V}$, solve for I_D;

b) Find I_D and V_D using the ideal diode equation. Use $I_S = 10^{-14}$ A and T=300 K.

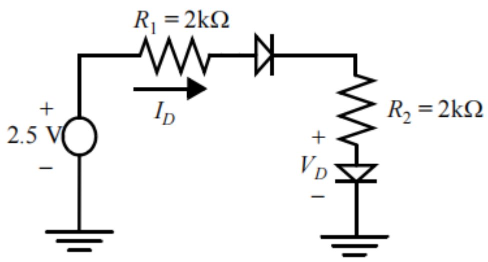

Fig.1.1

2. For the circuit in Fig.1.2, V_s=3.3 V. Assume $A_D = 12\ \mu\text{m}^2$, $\varphi_0 = 0.65$ V, and m= 0.5, $N_A = 2.5\times10^{16}\ \text{cm}^{-3}$, $N_D = 5\times10^{15}\ \text{cm}^{-3}$ and $\varepsilon_{si} = 11.7\varepsilon_0, \varepsilon_0 = 8.85\times10^{-12}F/m.$

a) Is the diode forward- or reverse-biased?

b) Find I_D and V_D;

c) Find the depletion region width, W_j, of the diode;

d) Use the parallel-plate model to find the junction capacitance, C_j;

e) Set V_s = 1.5 V. Again using the parallel-plate model, explain qualitatively why C_j increases.

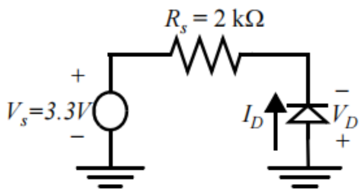

Fig.1.2

3. Fig.1.3 shows NMOS and PMOS devices with drains, source, and gate ports annotated. Determine the operation region (saturation, linear, or cutoff) and the drain current I_D for each of the biasing configurations given in table. Assume the model parameters from Table.1.1, V_{BS}=0 and W/L = 1, L=1μm fill the table

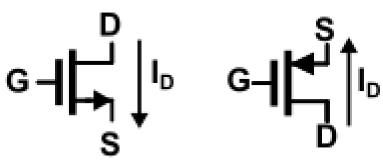

Fig.1.3

	V_{GS}(V)	V_{DS}(V)	Operation region	I_D (μA)
NMOS	2.5	2.5		
	3.3	2.2		
	0.6	0.1		
PMOS	-0.5	-1.25		
	-2.5	-1.8		
	-2.5	-0.7		

4. An NMOS device is plugged into the test configuration shown below in Fig .1.4 The input V_{in} is 2V. The current source draws a constant current of 50 μA. R is a variable resistor between 10kΩ and 30 kΩ. Transistor M1 has following transistor parameters: k'= 110μA/V^2, V_T = 0.7V, and V_{DSAT} = 0.6V, and has a W/L = 2.5μ/0.25. For simplicity, the body effect and channel length modulation can be neglected, i.e λ=0, γ=0.

a) When R =10kΩ find the operation region, V_D and V_S.

b) For the case of R = 10kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively.

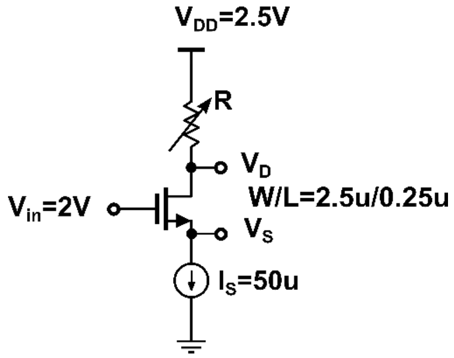

Fig.1.4

Thinking Questions(optional)

5. Show that two MOS transistors connected in parallel with channel widths of W_1 and W_2 and identical channel lengths of L can be modeled as one equivalent MOS transistor whose width is W_1+W_2 and whose length is L, as shown in Fig.1.5 Assume the transistors are identical except for their channel widths.

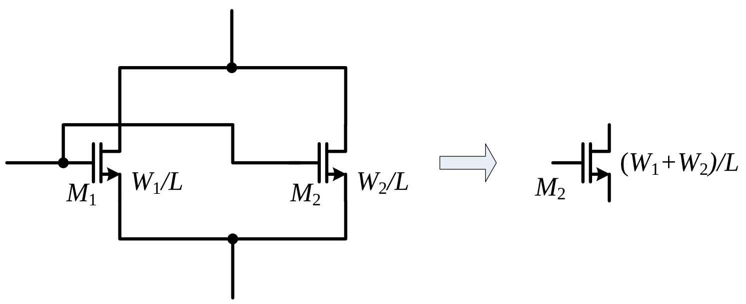

Fig.1.5

6. Show that two MOS transistors connected in series with channel lengths of L_1 and L_2 and identical channel widths of W can be modeled as one equivalent MOS transistor whose width is W and whose length is L_1+L_2, as shown in Fig. 1.6. Assume the transistors are identical except for their channel lengths. Ignore the body effect and channel-length modulation.

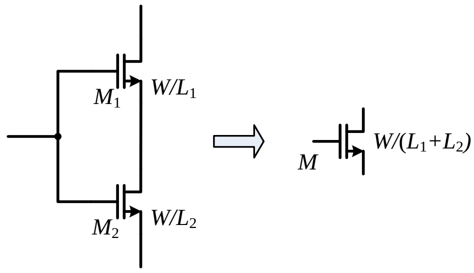

Fig.1.6

Table.1.1

Parameter Symbol	**Parameter Description**	**Typical Parameter Value**		**Units**
		n-Channel	**p-Channel**	
V_{T0}	Threshold voltage ($V_{BS}=0$)	0.7	−0.7	V
K'	Transconductance parameter (in saturation)	110.0	50.0	μA/V^2
γ	Bulk threshold parameter	0.4	0.57	$V^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1μm) 0.01 (L=2μm)	0.05 (L=1μm) 0.01 (L=2μm)	V^{-1}
$2\|\Phi_F\|$	Surface potential at strong inversion	0.7	0.8	V

$*K' = \frac{1}{2}\mu C_{ox}$