Exercise 7

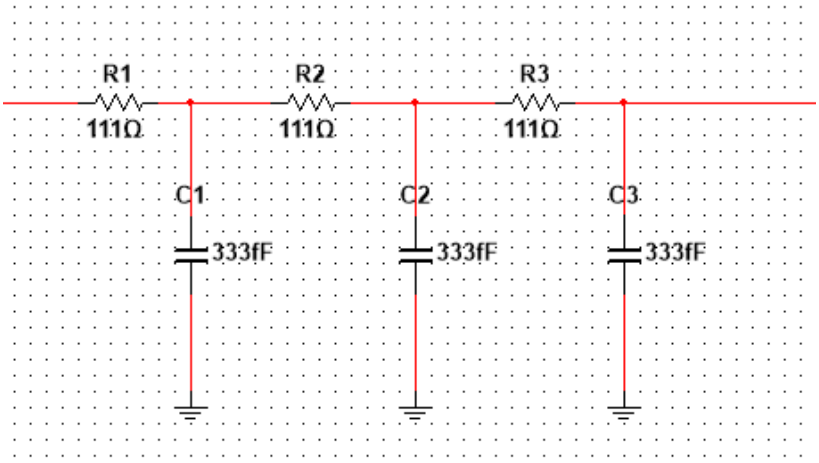
7-1 Consider a 5 mm-long, 4 λ-wide metal2 wire in a 0.6 μm process. The sheet resistance is 0.08 Ω/□ and the capacitance is 0.2 fF/μm. Construct 3-segment L-model and 3-segment π-model for the wire. (Please present models and calculate delay).

Answer

$$R = R_{\square}\frac{l}{w}$$

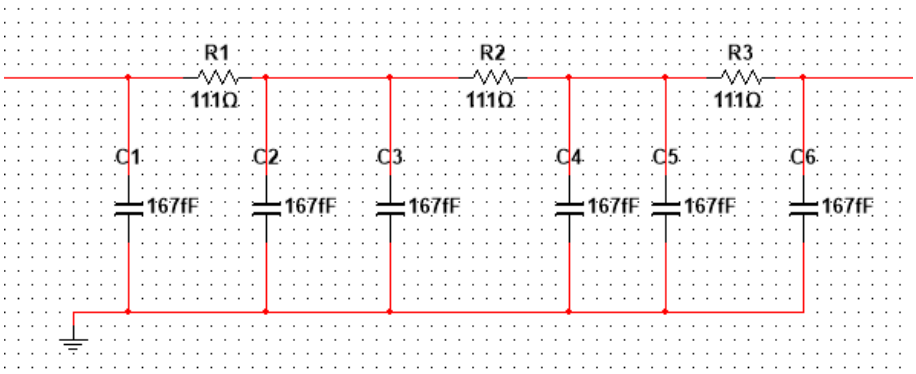
The wire width is 1.2μm so the wire is 5000μm/1.2μm= 4167 squares in length

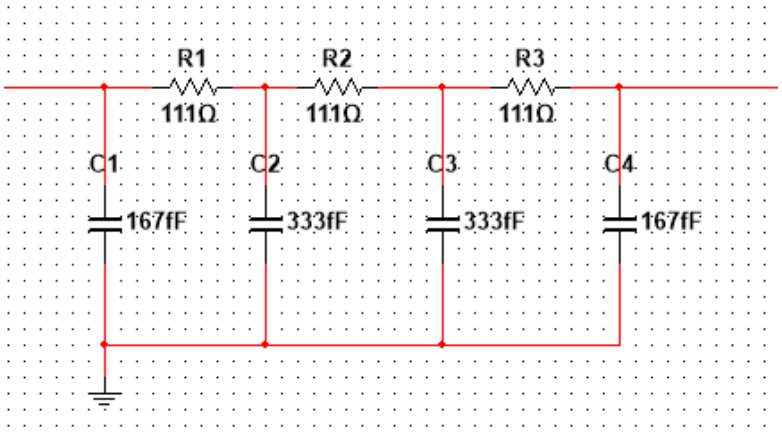
So, the total resistance is (0.08 $\Omega/$ sq) $\times$ 4167 sq) = 333 Ω The total capacitance is (0.2 fF/μm)$\times$5000μm) = 1 pF



3-segment L-model

$\tau = C_1R_1 + C_2(R_1 + R_2) + C_3(R_1 + R_2 + R_3) = 2.22 \times 10^{-10}s$





3-segment $\boldsymbol{\pi}$-model

$$\tau = C_2R_1 + C_3(R_1 + R_2) + C_4(R_1 + R_2 + R_3) = 1.67 \times 10^{-10}s$$

7-2 Assume an inverter is designed with a PMOS/NMOS ratio of 3.6 and the NMOS transistor is minimum size. (W = 0.375μm, L = 0.25μm, W/L =1.5). VM=1.25V, VDD=2.5V. Please describe the voltage transfer characteristic and noise margins of CMOS inverter. (use V_{IL}, V_{IH}, NM_H, NM_L and g). The parameters shown in table 7.1.

Table7.1

	V_{T0} (V)	γ ($V^{1/2}$)	V_{DSAT} (V)	K ($\mu A/V^2$)	λ (V^{-1})
NMOS	0.7	0.45	0.83	134	0.1
PMOS	-0.8	-0.4	-1	-50	-0.2

Answer

$$I_D(V_M) = K_N(\frac{W}{L})_N(V_{GS} - V_{THN})^2(1 + \lambda_n V_M) = 68.4 \times 10^{-6}A$$

$$\mathrm{g} = \frac{-1}{I_D(V_M)} \times \frac{k_n \frac{w}{l}_n V_{DSATn} + k_p \frac{w}{l}_p V_{DSATp}}{\lambda_n - \lambda_p} = -24.93$$

$$V_{IH} = V_M - \frac{V_M}{g} = 1.3$$

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g} = 1.2$$

$$NM_H = V_{DD} - V_{IH} = 1.2 \qquad NM_L = V_{IL} = 1.2$$