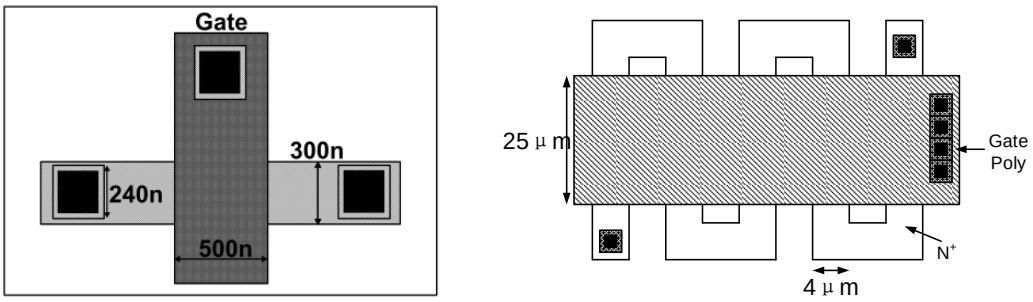
Exercise 1

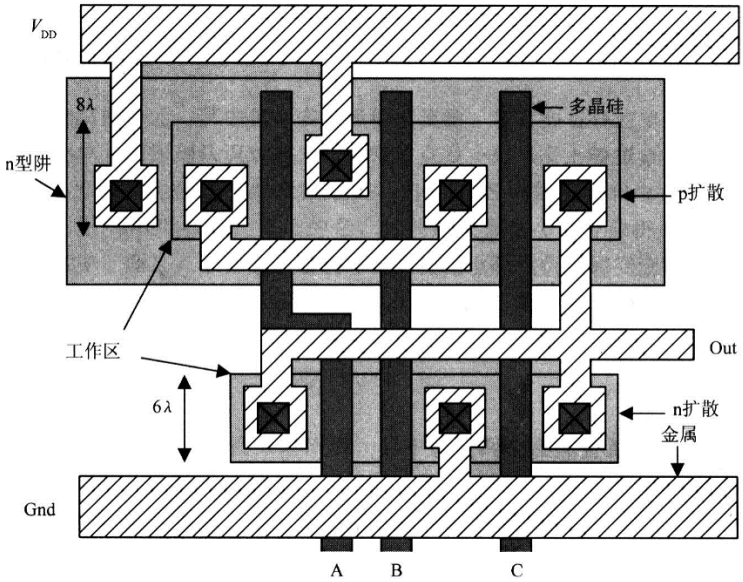
1. Two layouts of n-channel MOSFET are shown in Fig.3.1. What is the width and length of the two devices?



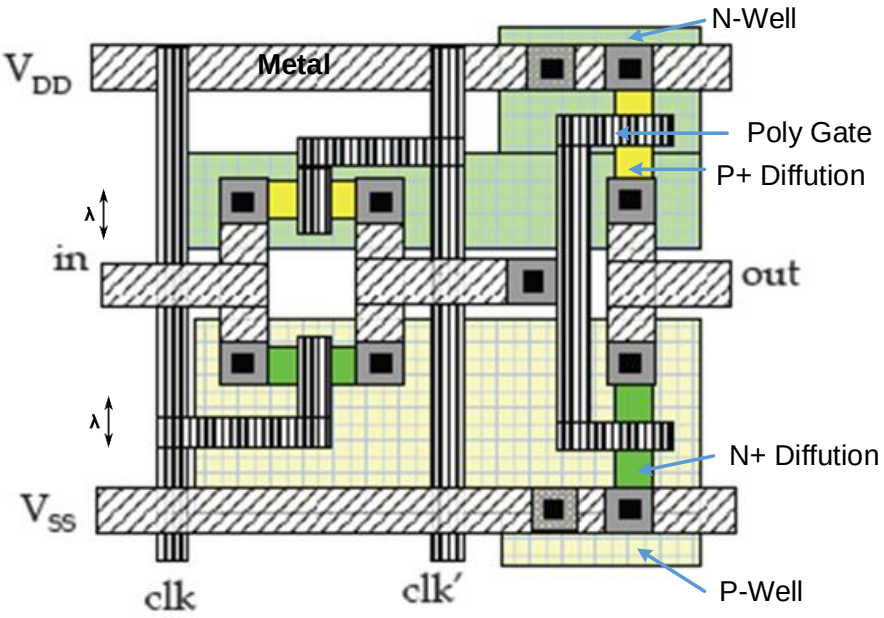
(a) (b)

Fig.3.1

2. The layouts of a circuit are shown in Fig.3.2. Give the corresponding schematics and its function, and mark the *W*/*L* sizes of each transistor. Assume $L=2\lambda$, $\lambda=0.4\mu m$.



(a) p-sub, n-well technology



(b) dual-well technology, and $clk' = \overline{clk}$

Fig.3.2

3. Layout of a different pair with PMOS current source loads in p-sub N-well technology is shown as Fig.3.3. Give the corresponding schematics and mark the W/L sizes of each transistor. Assume λ=0.4μm.

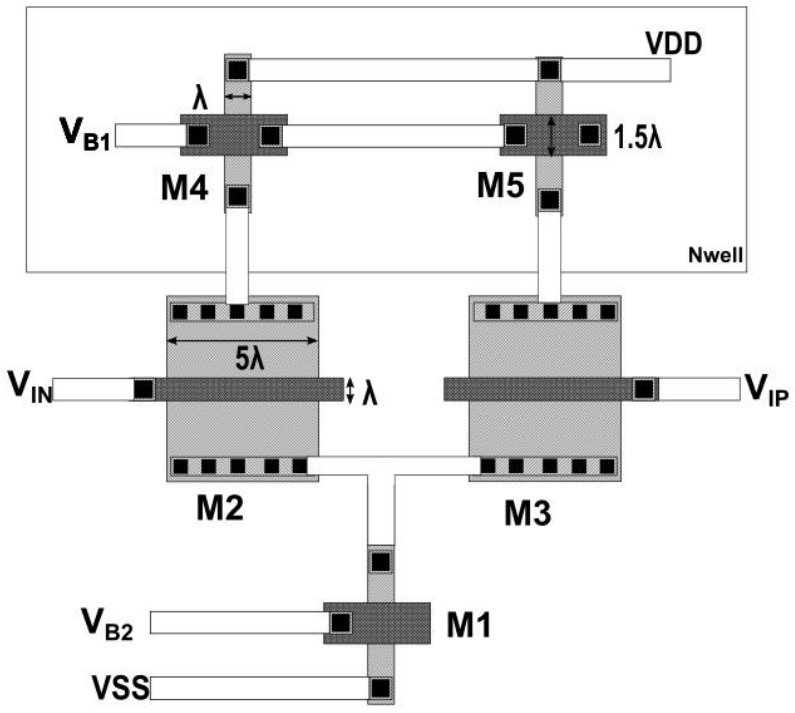


Fig.3.3