



Exercise 3

3-1. Two layouts of n-channel MOSFET are shown in Fig.3.1. What is the width and length of the two devices?

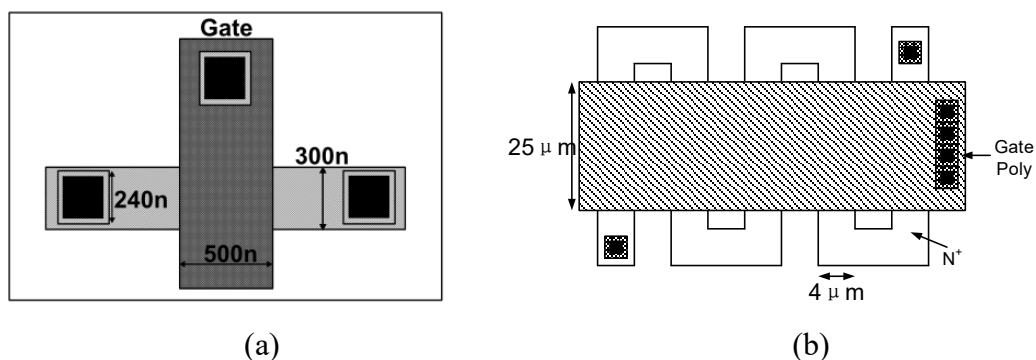
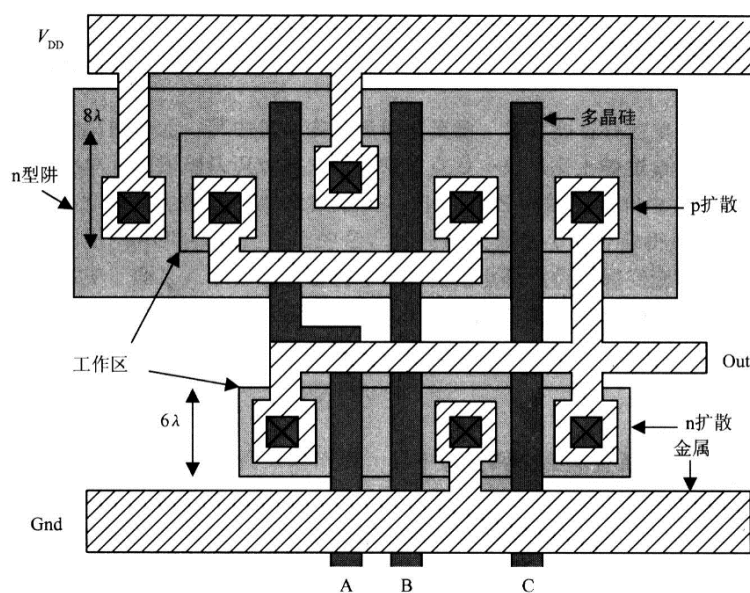


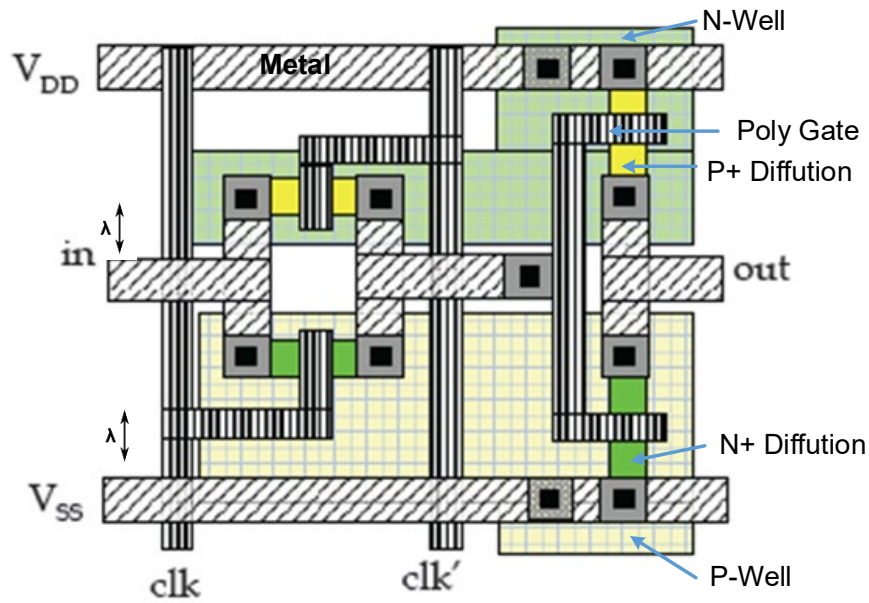
Fig.3. 1

Answer:

- (a) Length=500n; Width=300n
(b) Length=5 × 25μm = 125μm; Width=4μm

3-2. The layouts of a circuit are shown in Fig.3.2. Give the corresponding schematics and itsfunction, and mark the W/L sizes of each transistor. Assume $L=2\lambda$, $\lambda=0.4\mu\text{m}$.



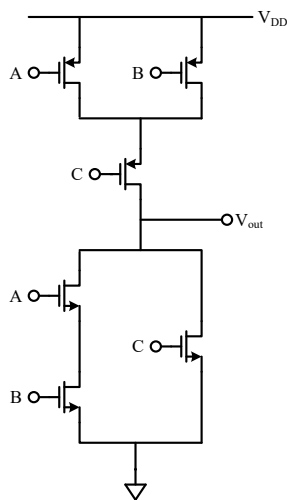


(b) dual-well technology, and $clk' = \overline{clk}$

Fig.3. 2

Answer:

(a)



$$\text{Out} = \overline{AB + C}$$

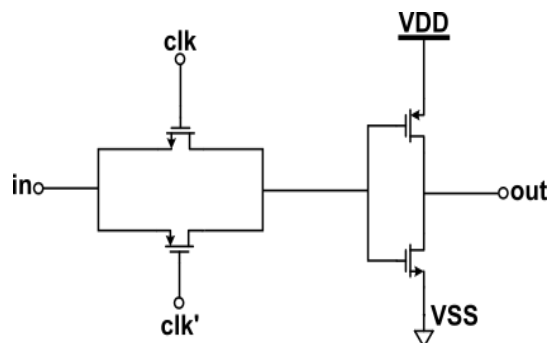
W/L of N-MOSFET:

$$\frac{6\lambda}{2\lambda} = \frac{6 \times 0.4}{2 \times 0.4} = \frac{2.4}{0.8}$$

W/L of P-MOSFET:

$$\frac{8\lambda}{2\lambda} = \frac{8 \times 0.4}{2 \times 0.4} = \frac{3.2}{0.8}$$

(b)



CLK high: $\text{Out} = \overline{IN}$

CLK low: $\text{Out} = 0$

W/L of N-MOSFET:

$$\frac{\lambda}{2\lambda} = \frac{0.4}{2 \times 0.4} = \frac{0.4}{0.8}$$

W/L of P-MOSFET:

$$\frac{\lambda}{2\lambda} = \frac{0.4}{2 \times 0.4} = \frac{0.4}{0.8}$$

3-3. Layout of a differential pair with PMOS current source loads in p-sub N-well technology is shown as Fig.3.3. Give the corresponding schematics and mark the W/L sizes of each transistor. Assume $\lambda=0.4\mu\text{m}$.

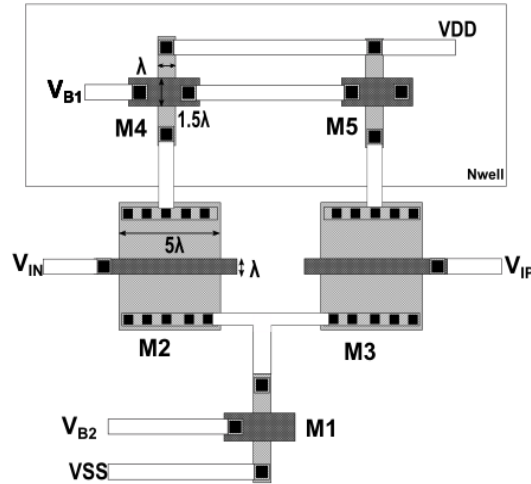
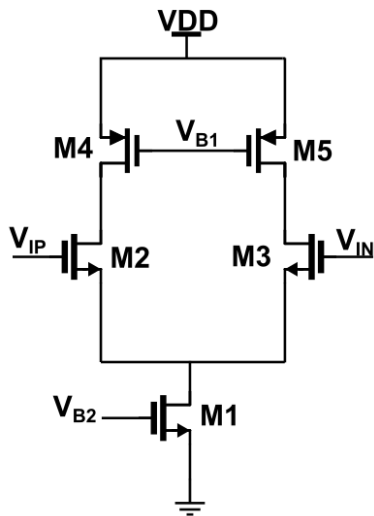


Fig.3.3

Answer:



$$\begin{aligned} M1=M4=M5 \quad \frac{W}{L} &= \frac{\lambda}{1.5\lambda} \\ M2=M3 \quad \frac{W}{L} &= \frac{5\lambda}{\lambda} \end{aligned}$$