Exercise 7

7-1 Consider a 5 mm-long, 4 λ-wide metal2 wire in a 0.6 μm process. The sheet resistance is 0.08 Ω/□ and the capacitance is 0.2 fF/μm. Construct 3-segment L-model and 3-segment π-model for the wire. (Please present models and calculate delay).

7-2 Assume an inverter is designed with a PMOS/NMOS ratio of 3.6 and the NMOS transistor is minimum size. (W = 0.375μm, L = 0.25μm, W/L =1.5). VM=1.25V, VDD=2.5V. Please describe the voltage transfer characteristic and noise margins of CMOS inverter. (use V_{IL}, V_{IH}, NM_H, $NM_L$and g). The parameters shown in table 7.1.

Table7.1

	V_{T0} (V)	γ ($V^{1/2}$)	V_{DSAT} (V)	K (μA/V^2)	λ (V^{-1})
NMOS	0.7	0.45	0.83	134	0.1
PMOS	-0.8	-0.4	-1	50	0.2