WM8994

Multi-Channel Audio Hub CODEC for Smartphones

DESCRIPTION

The WM8994 is a highly integrated ultra-low power hi-fi CODEC designed for smartphones and other portable devices rich in multimedia features.

An integrated stereo class D/AB speaker driver and class W headphone driver minimize power consumption during audio playback.

The device requires only two voltage supplies, with all other internal supply rails generated from integrated LDOs.

Stereo full duplex asynchronous sample rate conversion and multi-channel digital mixing combined with powerful analogue mixing allow the device to support a huge range of different architectures and use cases.

A fully programmable parametric EQ provides speaker compensation and a dynamic range controller can be used in the ADC or DAC paths for maintaining a constant signal level, maximizing loudness and protecting speakers against overloading and clipping.

A smart digital microphone interface provides power regulation, a low jitter clock output and decimation filters for up to four digital microphones. A MIC activity detect with interrupt is available.

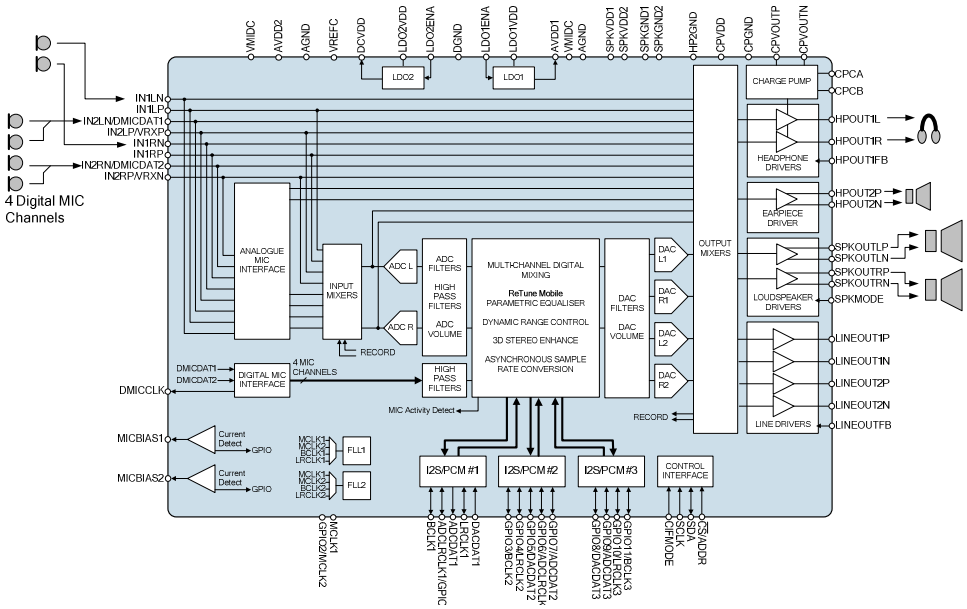
Active ground loop noise rejection and DC offset correction help prevent pop noise and suppress ground noise on the headphone outputs.

FEATURES

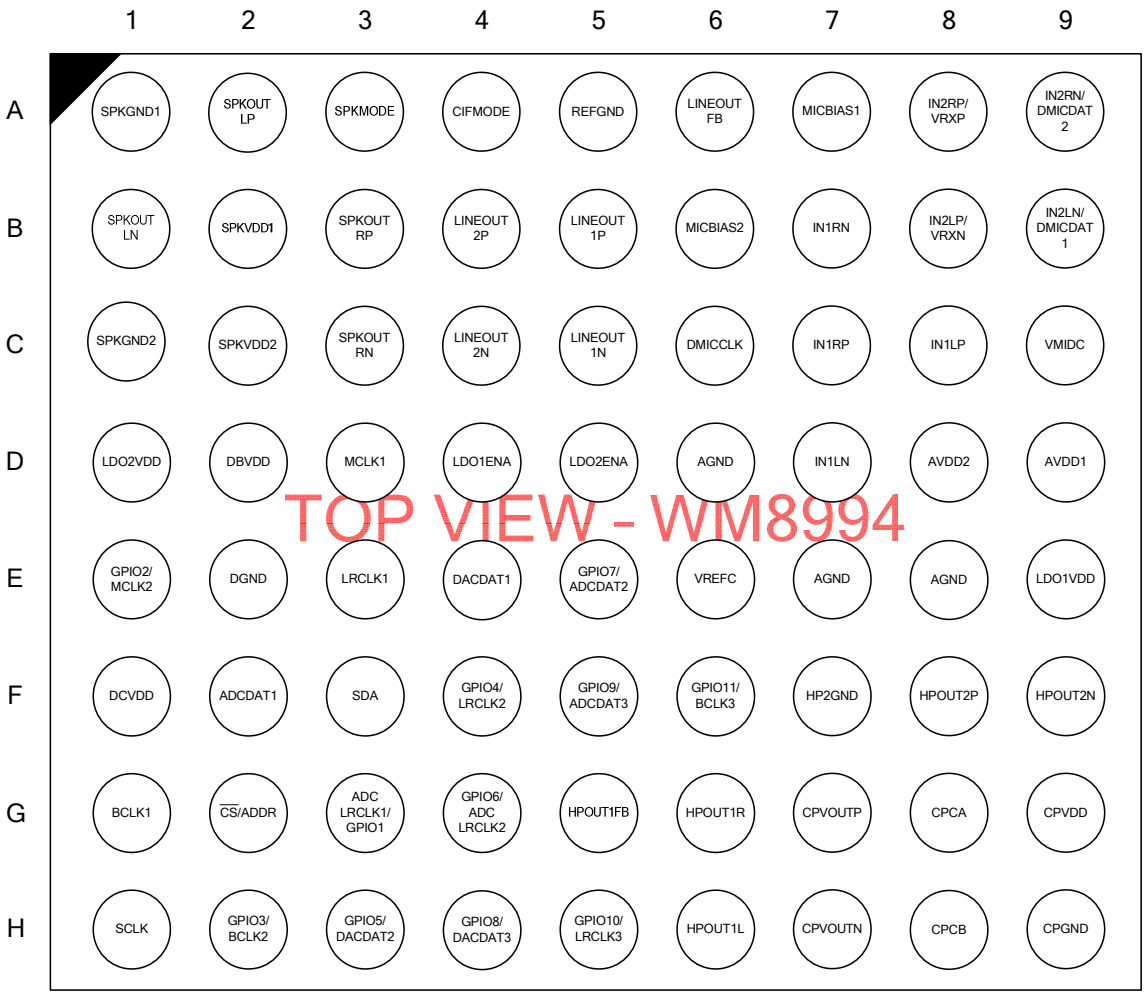
- Hi-Fi 24-bit 4-channel DAC and 2-channel ADC
- 100dB SNR during DAC playback ('A' weighted)
- Smart MIC interface
  - Power, clocking and data input for up to four digital MICs
  - High performance analogue MIC interface
  - MIC activity monitor & interrupt allows processor to sleep
- 1W stereo / 2W mono class D/AB speaker driver
- Capless Class W headphone drivers
  - Integrated charge pump
  - 5.3mW total power for DAC playback to headphones
- 4 Line outputs (single-ended or differential)
- BTL Earpiece driver
- Digital audio interfaces for multi-processor architecture
  - Asynchronous stereo duplex sample rate conversion
  - Powerful mixing and digital loopback functions
- ReTune™ Mobile 5-band, 6-channel parametric EQ
- Programmable dynamic range controller
- Dual FLL provides all necessary clocks
  - Self-clocking modes allow processor to sleep
  - All standard sample rates from 8kHz to 96kHz
- Active noise reduction circuits
  - DC offset correction removes pops and clicks
  - Ground loop noise cancellation
- Integrated LDO regulators
- 72-ball W-CSP package (4.511 x 4.023 x 0.7mm)

APPLICATIONS

- Smartphones and music phones
- Portable navigation
- Tablets
- eBooks
- Portable Media Players



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8994ECS/R	-40°C to +85°C	72-ball W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	SPKGND1	Supply	Ground for speaker driver (Return path for SPKVDD1)
A2	SPKOUTLP	Analogue Output	Left speaker positive output
A3	SPKMODE	Digital Input	2W Mono/1W Stereo speaker mode select
A4	CIFMODE	Digital Input	Selects 2-wire or 3/4-wire control interface mode
A5	REFGND	Supply	Analogue ground
A6	LINEOUTFB	Analogue Input	Line output ground loop noise rejection feedback
A7	MICBIAS1	Analogue Output	Microphone bias 1
A8	IN2RP/VRXP	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential positive input (RXVOICE +)
A9	IN2RN/ DMICDAT2	Analogue Input / Digital Input	Right channel line input / Right channel negative differential MIC input /
B1	SPKOUTLN	Analogue Output	Left speaker negative output
B2	SPKVDD1	Supply	Supply for speaker driver 1 (Left channel)
B3	SPKOUTRP	Analogue Output	Right speaker positive output
B4	LINEOUT2P	Analogue Output	Positive mono line output / Positive left line output
B5	LINEOUT1P	Analogue Output	Positive mono line output / Positive left line output
B6	MICBIAS2	Analogue Output	Microphone bias 2
B7	IN1RN	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input
B8	IN2LP/VRXN	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential negative input (RXVOICE -)
B9	IN2LN/ DMICDAT1	Analogue Input / Digital Input	Left channel line input / Left channel negative differential MIC input / Digital MIC data input 1
C1	SPKGND2	Supply	Ground for speaker driver (Return path for SPKVDD2)
C2	SPKVDD2	Supply	Supply for speaker driver 2 (Right channel)
C3	SPKOUTRN	Analogue Output	Right speaker negative output
C4	LINEOUT2N	Analogue Output	Negative mono line output / Positive left or right line output
C5	LINEOUT1N	Analogue Output	Negative mono line output / Positive left or right line output
C6	DMICCLK	Digital Output	Digital MIC clock output
C7	IN1RP	Analogue Input	Right channel line input / Right channel positive differential MIC input
C8	IN1LP	Analogue Input	Left channel line input / Left channel positive differential MIC input
C9	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
D1	LDO2VDD	Supply	Supply for LDO2
D2	DBVDD	Supply	Digital buffer (I/O) supply
D3	MCLK1	Digital Input	Master clock 1
D4	LDO1ENA	Digital Input	Enable pin for LDO1
D5	LDO2ENA	Digital Input	Enable pin for LDO2
D6	AGND	Supply	Analogue ground (Return path for AVDD1)
D7	IN1LN	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
D8	AVDD2	Supply	Bandgap reference, analogue class D and FLL supply
D9	AVDD1	Supply / Analogue Output	Analogue core supply / LDO1 Output
E1	GPIO2/ MCLK2	Digital Input	General Purpose pin GPI 2 / Master clock 2
E2	DGND	Supply	Digital ground (Return path for DCVDD and DBVDD)
E3	LRCLK1	Digital Input / Output	Audio interface 1 left / right clock

PIN NO	NAME	TYPE	DESCRIPTION
E4	DACDAT1	Digital Input	Audio interface 1 DAC digital audio data
E5	GPIO7/ ADCDAT2	Digital Input / Output	General Purpose pin GPIO 7 / Audio interface 2 ADC digital audio data
E6	VREFC	Analogue Output	Bandgap reference decoupling capacitor
E7	AGND	Supply	Analogue ground (Return path for AVDD1)
E8	AGND	Supply	Analogue ground (Return path for AVDD1)
E9	LDO1VDD	Supply	Supply for LDO1
F1	DCVDD	Supply / Analogue Output	Digital core supply / LDO2 output
F2	ADCDAT1	Digital Output	Audio interface 1 ADC digital audio data
F3	SDA	Digital Input / Output	Control interface data input and output / 2-wire acknowledge output
F4	GPIO4/ LRCLK2	Digital Input / Output	General Purpose pin GPIO 4 / Audio interface 2 left / right clock
F5	GPIO9/ ADCDAT3	Digital Input / Output	General Purpose pin GPIO 9 / Audio interface 3 ADC digital audio data
F6	GPIO11/ BCLK3	Digital Input / Output	General Purpose pin GPIO 11 / Audio interface 3 bit clock
F7	HP2GND	Supply	Analogue ground
F8	HPOUT2P	Analogue Output	Earpiece speaker non-inverted output
F9	HPOUT2N	Analogue Output	Earpiece speaker inverted output
G1	BCLK1	Digital Input / Output	Audio interface 1 bit clock
G2	$\overline{CS}$/ADDR	Digital Input	3-/4-wire (SPI) chip select or 2-wire (I2C) address select
G3	ADCLRCLK1/ GPIO1	Digital Input / Output	Audio interface 1 ADC left / right clock / General Purpose pin GPIO 1/ Control interface data output
G4	GPIO6/ ADCLRCLK2	Digital Input / Output	General Purpose pin GPIO 6 / Audio interface 2 ADC left / right clock
G5	HPOUT1FB	Analogue Input	HPOUT1L and HPOUT1R ground loop noise rejection feedback
G6	HPOUT1R	Analogue Output	Right headphone output
G7	CPVOUTP	Analogue Output	Charge pump positive supply decoupling pin (HPOUT1L, HPOUT1R)
G8	CPCA	Analogue Output	Charge pump fly-back capacitor pin
G9	CPVDD	Supply	Charge pump supply
H1	SCLK	Digital Input	Control interface clock input
H2	GPIO3/ BCLK2	Digital Input / Output	General Purpose pin GPIO 3 / Audio interface 2 bit clock
H3	GPIO5/ DACDAT2	Digital Input / Output	General Purpose pin GPIO 5 / Audio interface 2 DAC digital audio data
H4	GPIO8/ DACDAT3	Digital Input / Output	General Purpose pin GPIO 8 / Audio interface 3 DAC digital audio data
H5	GPIO10/ LRCLK3	Digital Input / Output	General Purpose pin GPIO 10 / Audio interface 3 left / right clock
H6	HPOUT1L	Analogue Output	Left headphone output
H7	CPVOUTN	Analogue Output	Charge pump negative supply decoupling pin (HPOUT1L, HPOUT1R)
H8	CPCB	Analogue Output	Charge pump fly-back capacitor pin
H9	CPGND	Supply	Charge pump ground (Return path for CPVDD)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (AVDD1, DBVDD)	-0.3V	+4.5V
Supply voltages (AVDD2, DCVDD, LDO2VDD)	-0.3V	+2.5V
Supply voltages (CPVDD)	-0.3V	+2.2V
Supply voltages (SPKVDD1, SPKVDD2, LDO1VDD)	-0.3V	+7.0V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD1 +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	0.95	1.0	2.0	V
Digital supply range (I/O)	DBVDD	1.62	1.8	3.6	V
Analogue supply 1 range	AVDD1	2.4	3.0	3.3	V
Analogue supply 2 range	AVDD2	1.71	1.8	2.0	V
Charge Pump supply range	CPVDD	1.71	1.8	2.0	V
Speaker supply range	SPKVDD1, SPKVDD2	2.7	5.0	5.5	V
LDO1 supply range	LDO1VDD	2.7	5.0	5.5	V
LDO2 supply range	LDO2VDD	1.71	1.8	2.0	V
Ground	DGND, AGND, CPGND, SPKGND1, SPKGND2, REFGND, HP2GND		0		V
Power supply rise time (notes 6, 7 and 8)	All supplies	1			µs

Notes:

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.
2. There is no power sequencing requirement; the supplies may be enabled in any order.
3. AVDD1 must be less than or equal to SPKVDD1 and SPKVDD2.
4. When AVDD1 is supplied externally (not from LDO1), the LDO1VDD voltage must be greater than or equal to AVDD1
5. When DCVDD is supplied externally (not from LDO2), the LDO2VDD voltage must be greater than or equal to DCVDD
6. DCVDD and AVDD1 minimum rise times do not apply when these domains are powered using the internal LDOs.
7. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Wolfson strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed (see “Applications Information” section).
8. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

DEVICE DESCRIPTION

The WM8994 is a low power, high quality audio codec designed to interface with a wide range of processors and analogue components. A high level of mixed-signal integration in a very small footprint makes it ideal for portable applications such as mobile phones.

The analogue circuits of the WM8994 are almost entirely backwards-compatible with the WM8993 with the exception of two additional DAC channels, a dual FLL and two integrated LDO regulators.

Three sets of audio interface pins are available in order to provide independent and fully asynchronous connections to multiple processors, typically an application processor, baseband processor and wireless transceiver. Any two of these interfaces can operate totally independently and asynchronously while the third interface can be synchronised to either of the other two and can also provide ultra low power loopback modes to support, for example, wireless headset voice calls.

Four digital microphone input channels are available to support advanced multi-microphone applications such as noise cancellation. An integrated microphone activity monitor is available to enable the processor to sleep during periods of microphone inactivity, saving power.

Four DAC channels are available to support use cases requiring up to four simultaneous digital audio streams to the output drivers.

Eight highly flexible analogue inputs allow interfacing to up to four microphone inputs (single-ended or differential), plus multiple stereo or mono line inputs. Connections to an external voice CODEC, FM radio, line input, handset MIC and headset MIC are all fully supported. Signal routing to the output mixers and within the CODEC has been designed for maximum flexibility to support a wide variety of usage modes. A 'Direct Voice' path from a voice CODEC directly to the Speaker or Earpiece output drivers is included.

Nine analogue output drivers are integrated, including a stereo pair of high power, high quality Class D/AB switchable speaker drivers; these can support 1W each in stereo mode, or can be coupled to support a 2W mono speaker output. A mono earpiece driver is provided, providing output from the output mixers or from the low-power differential 'Direct Voice' path.

One pair of ground-reference headphone outputs is provided; these are powered from an integrated Charge Pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. A DC Servo circuit is available for DC offset correction, thereby suppressing pops and reducing power consumption. Four line outputs are provided, with multiple configuration options including 4 x single-ended output or 2 x differential outputs. The line outputs are suitable for output to a voice CODEC, an external speaker driver or line output connector. Ground loop feedback is available on the headphone outputs and the line outputs, providing rejection of noise on the ground connections. All outputs have integrated pop and click suppression features.

Internal differential signal routing and amplifier configurations have been optimised to provide the highest performance and lowest possible power consumption for a wide range of usage scenarios, including voice calls and music playback. The speaker drivers offer low leakage and high PSRR; this enables direct connection to a Lithium battery. The speaker drivers provide eight levels of AC and DC gain to allow output signal levels to be maximised for many commonly-used SPKVDD/AVDD1 combinations.

The ADCs and DACs are of hi-fi quality, using a 24-bit low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed sample rates, whilst an integrated ultra-low power dual FLL provides additional flexibility. A high pass filter is available in all ADC and digital MIC paths for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise. A digital mixing path from the ADC or digital MICs to the DAC provides a sidetone of enhanced quality during voice calls. DAC soft mute and un-mute is available for pop-free music playback.

The integrated Dynamic Range Controllers (DRC) and ReTune™ Mobile 5-band parametric equaliser (EQ) provide further processing capability of the digital audio paths. The DRC provides compression and signal level control to improve the handling of unpredictable signal levels. 'Anti-clip' and 'quick release' algorithms improve intelligibility in the presence of transients and impulsive noises. The EQ provides the capability to tailor the audio path according to the frequency characteristics of an earpiece or loudspeaker, and/or according to user preferences.

The WM8994 has highly flexible digital audio interfaces, supporting a number of protocols, including I^2S, DSP, MSB-first left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power. The four digital MIC and ADC channels and four DAC channels are available via four TDM channels on Digital Audio Interface 1 (AIF1).

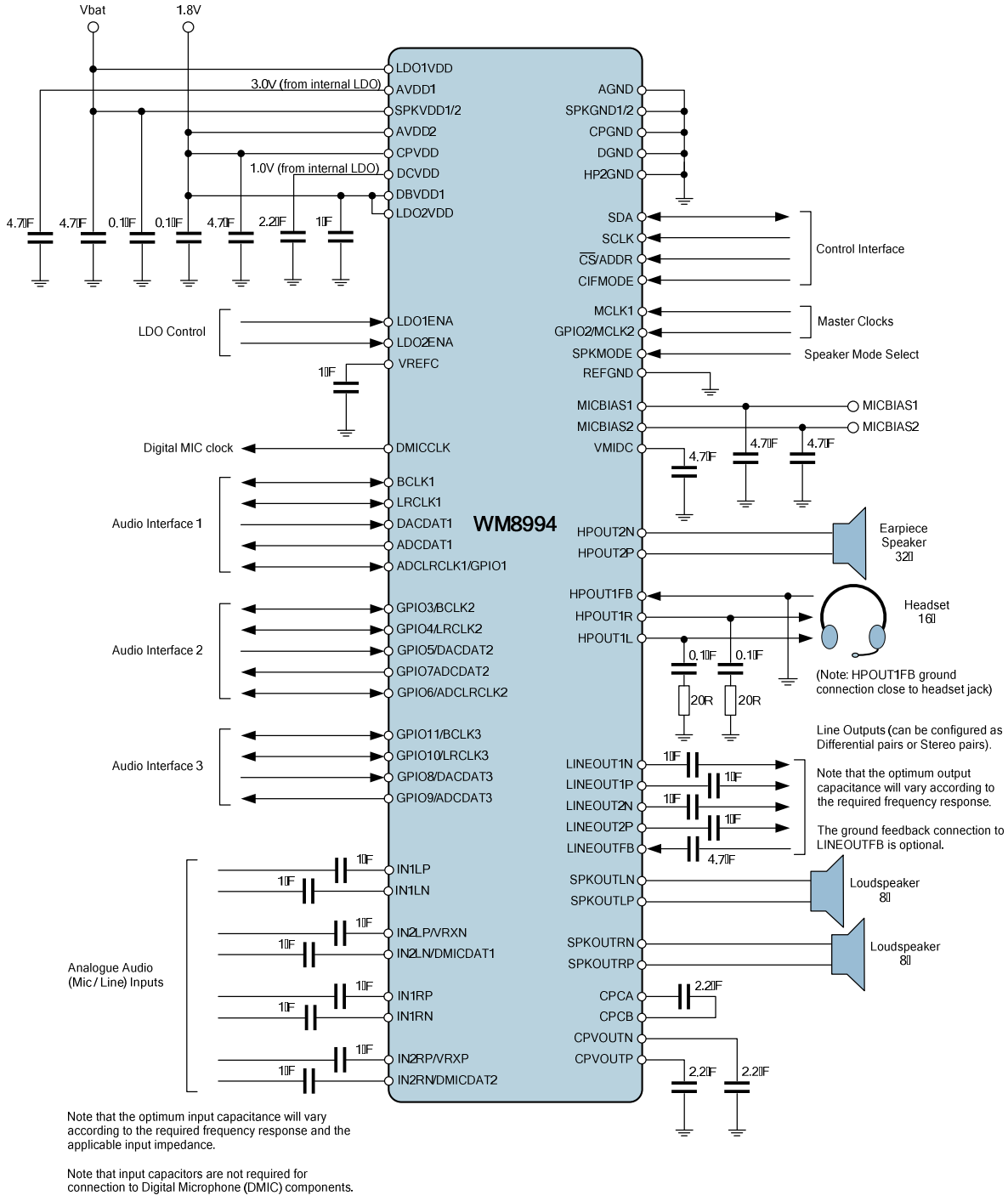
A powerful digital mixing core allows data from each TDM channel of each audio interface and from the ADCs and digital MICs to be mixed and re-routed back to a different audio interface and to the 4 DAC output channels. The digital mixing core can operate synchronously with either Audio Interface 1 or Audio Interface 2, with asynchronous stereo full duplex sample rate conversion performed on the other audio interface as required.

The system clock (SYSCLK) provides clocking for the ADCs, DACs, DSP core, digital audio interface and other circuits. SYSCLK can be derived directly from one of the MCLK1 or MCLK2 pins or via one of two integrated FLLs, providing flexibility to support a wide range of clocking schemes. Typical portable system MCLK frequencies, and sample rates from 8kHz to 96kHz are all supported. Automatic configuration of the clocking circuits is available, derived from the sample rate and from the MCLK / SYSCLK ratio.

The WM8994 uses a standard 2, 3 or 4-wire control interface, providing full software control of all features, together with device register readback. An integrated Control Write Sequencer enables automatic scheduling of control sequences; commonly-used signal configurations may be selected using ready-programmed sequences, including time-optimised control of the WM8994 pop suppression features. It is an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Versatile GPIO functionality is provided, with support for button/accessory detect inputs, or for clock, system status, or programmable logic level output for control of additional external circuitry. Interrupt logic, status readback and de-bouncing options are supported within this functionality.

RECOMMENDED EXTERNAL COMPONENTS

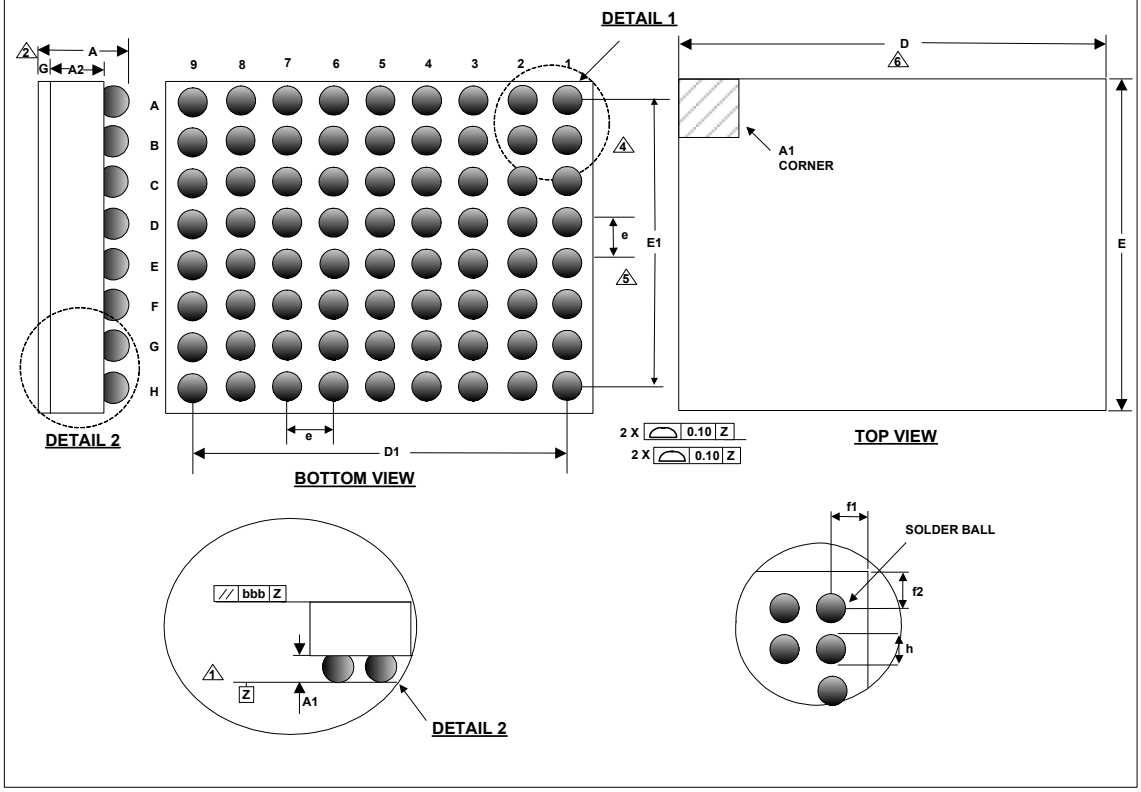


Note that the optimum input capacitance will vary according to the required frequency response and the applicable input impedance.

Note that input capacitors are not required for connection to Digital Microphone (DMIC) components.

PACKAGE DIMENSIONS

B: 72 BALL W-CSP PACKAGE 4.511 x 4.023 x 0.7 mm BODY, 0.50 mm BALL PITCH **DM068.C**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.615	0.7	0.785	
A1	0.219	0.244	0.269	
A2	0.361	0.386	0.411	
D	4.471	4.511	4.551	
D1		4.00 BSC		
E	3.983	4.023	4.063	
E1		3.50 BSC		
e		0.50 BSC		5
f1		0.2555 BSC		8
f2		0.2615 BSC		9
g	0.035	0.070	0.105	
h		0.314 BSC		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.
8. f1 = NOMINAL DISTANCE OF BALL CENTRE TO DIE EDGE X AXIS (AS PER POD) – APPLICABLE TO ALL CORNERS OF DIE.
9. f2 = NOMINAL DISTANCE OF DIE CENTRE TO DIE EDGE IN Y AXIS (AS PER POD) – APPLICABLE TO ALL CORNERS OF DIE.

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ADDRESS:

Wolfson Microelectronics plc

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com