Digital VLSI Implementation of Leaky Integrate and Fire (LIF) with Spike-rate Adaptation (SRA) Neuron Model

Abstract— **This report summarizes the steps and results of the VLSI implementation of LIF-SRA neuron model, including software simulation using Matlab, hardware simulation using Verilog, synthesis and place and route.**

I. INTRODUCTION

Extensive work has been done on developing models to mimic the spiking behavior of neurons. Models have different implementation costs reflected by their floating point operation per second (FLOPS), and the behaviors of neurons that models can mimic are also different. In his paper, Izhikevich summarized a series of neuron models and the features that each model can express [1]. In this project, we will try to reproduce the features of the LIF-SRA model, and implement the neuron model in digital VLSI.

II. MODEL AND BIOLOGICAL REPRESENTATIONS

A. Mathematical Model of Leaky Integrate and Fire (LIF) with Spike-rate Adaptation (SRA) neuron

The model can be described by two 1D differential equations and an update rule when the membrane potential reaches the threshold voltage:

$$v' = I + a - bv + g(d - v)$$

$$g' = \frac{-g}{\tau}$$

The update rule when $v > v_{th}$:

$$\begin{cases} v = c \\ g = g + e \end{cases}$$

Input variable I is the stimulus, and a, b, c, d, e are all constant parameters. Function g is the update function and time constant τ describes the decay rate of g.

B. Biological Representation of the Model

v describes the membrane potential of the neuron. The typical value is -70 mV at rest, which is also the voltage at the start of the simulation. Input I is the positive stimulus current which can vary with time. a is a constant term describing the constant voltage change of the membrane, and b is the positive leaking term describing the increase of membrane potential due to the leaking current as a function of v. Constant c is also called the reset voltage, which is normally at -80mV. Constant v_{th} is the threshold voltage where the neuron fires, which is at -55 mV. Function g is a positive function modeling the conductance of K+ activation gate, which is initially at 0, and τ describes the speed of decay of the conductance. Constant d is the Nernst potential of K+ which is at -90 mV, and constant e is added to g each time the neuron fires, creating an outward current which reduces membrane potential and slows down the rate of tonic spiking.

C. Effect of Changing Parameters

Changing the parameter a would directly change the constant increase/decrease of the membrane voltage when there is no external stimulus. Increasing b would increase the leaking current which increases the spike rate. Increasing e will increase the effect of spike-rate adaptation and increasing time constant τ will also slow down the decay of g and increase the effect of spike-rate adaptation. Other parameters correspond to actual biological constants which normally we do not change.

III. NEURAL-COMPUTATIONAL FEATURES

There are total of five neural-computational features that can be expressed using the LIF with SRA model:

A. Tonic Spiking

When receiving constant stimulus current I and set parameter e to a low value, the neuron spikes at a constant frequency. The higher the current, the higher the frequency.
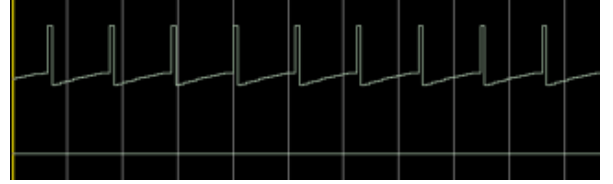
Simulated tonic spiking behavior of the neuron

B. Spike Frequency Adaptation

Keep the stimulus current constant as before, the spike frequency adaptation can be achieved by increasing the value of e and τ. With larger values of e and τ, the frequency decreases faster in constant stimulus.
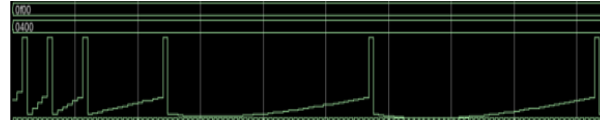
Spike frequency adaptation behavior of the neuron

C. Class 1 Excitable

Class 1 excitable can be achieved using a ramp input of stimulus current. The spike frequency will increase as the input current increases.
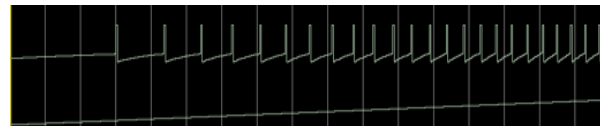
Class 1 excitable behavior of the neuron

D. Integrator

Two closer input pulses can be integrated into an action potential, but two far away pulses will not. This feature can be seen by inputting pulse stimulus.

Integrator behavior of the neuron

E. Depolarization after potential

Depolarization after potential can be easily simulated by just inputting one pulse stimulus. It can be seen from the graph that the membrane potential increases (depolarization) again after the hyperpolarization after action potential.
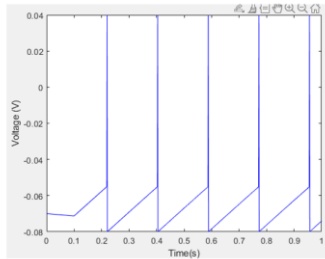

Depolarization after potential behavior of the neuron

IV. NEURAL-COMPUTATIONAL FEATURES IN MATHEMATICAL MODELS IN MATLAB

All the above simulations are performed in QuestaSim using a Verilog implementation of the LIF-SRA model. Then, we implemented the model again mathematically in Matlab to verify the behaviors.
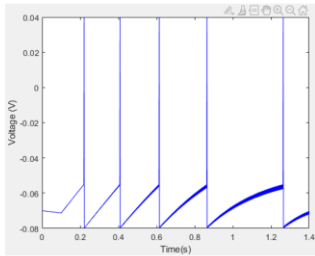
A. Tonic Spiking in Matlab
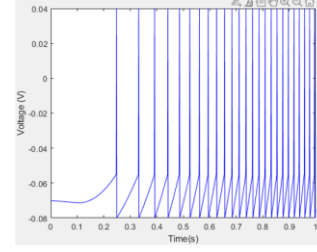

Tonic spiking behavior of the neuron in Matlab

B. Spike Frequency Adaptation in Matlab

Spike Frequency Adaptation of the neuron in Matlab

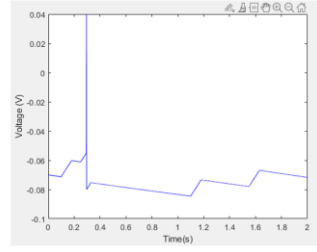### C. Class 1 Excitable in Matlab
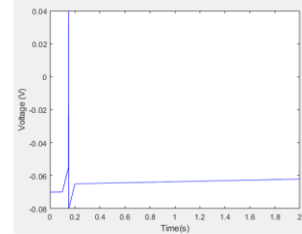

Class 1 excitable of the neuron in Matlab

D. Integrator

Integrator behavior of the neuron in Matlab

E. Depolarization after potential

Depolarization after potential behavior of the neuron in Matlab

From the above results we could see that there is a great consistency between the Verilog implement and Matlab mathematical models. Thus, the correct behavior of the Verilog implementation is verified using Matlab result.

V. VERILOG DESIGN

We use Verilog to describe the hardware of the model. We use 16-bit fixed point decimals to represent our inputs, outputs and parameters. 8 of the bits represent the integer part, and the rest 8 bits represent the decimal part. I and e are the inputs, and V is the output. Other parameters are stored internally and initialized in the beginning. 32-bit numbers are used to store the direct binary product of two numbers. Then, we take the middle 16 bits (i.e., bit 8 – 23) as the final product.

VI. SYNTHESIS

In this part, we synthesize the Verilog implementation of LIF-SRA model, translating the Verilog code into netlist.

A. Area

The combinational area of the design is 3072.98 μm^2. Buf/Inv area is 655.14 μm^2. Noncombinational area is 236.28 μm^2. Total cell area is 3336.25 μm^2.

B. Power

The cell internal power is 303.52 μW. The net switching power is 147.23 μW. Total dynamic power is 450.76 μW. Cell leakage power is 15.55 μW.

C. Timing

The minimal slack of the design is 1.76. Positive slack indicates that the timing constraints of the design is met.
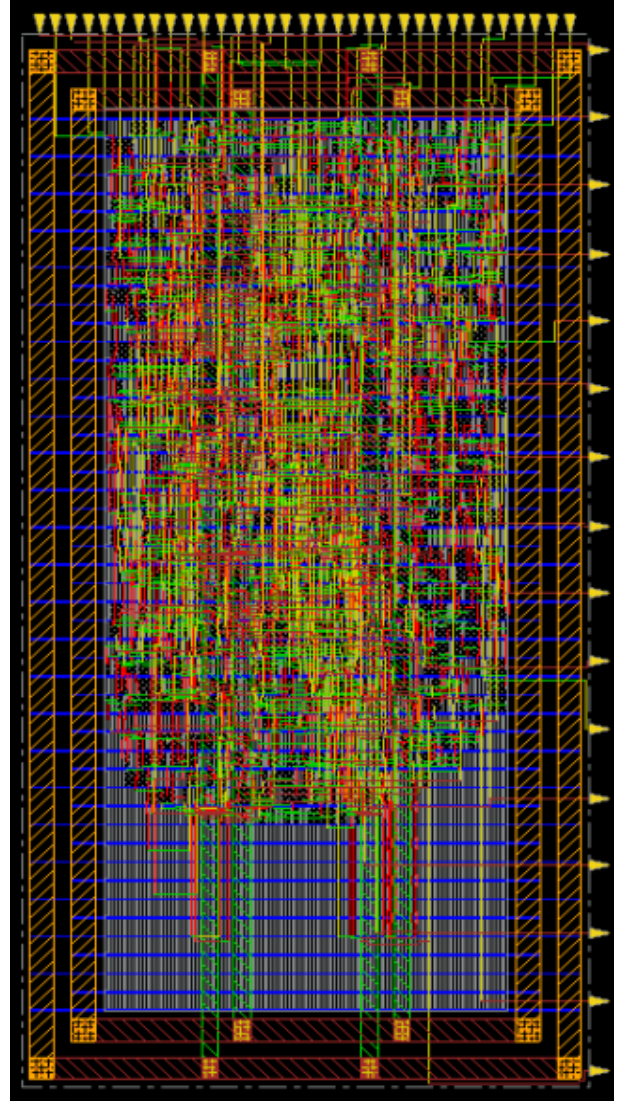
D. FLOPS and FOM

The number of floating point operations in every cycle/update is 9. Assuming a timestep of 1ms, FLOP will be 9000. Figure of merit, which is defined by

$$FOM = \frac{FLOPS}{AREA \cdot POWER}$$

Is $5.99 \times 10^{-3} \, \mu m^{-2} \cdot \mu W^{-1}$.

VII. PLACE AND ROUTE

A. Place and Route Visual Result

Place and route result from Innovus

The size of the cell is 69×138. Density is 46.477%.

VIII. GLOBAL IMPACTS OF IC DESIGN

Starting from quartz, the production of microprocessors involves many stages. Quartz, which is the natural form of SiO_2, will react with charcoal in furnace and turn into Si. To purify the silicon, it will be reacted with HCl to form $SiHCl_3$. During this process, impurities such as Fe, Al will be removed. Finally, $SiHCl_3$ will react with H_2 to yield pure Si. The pure Si can be melted and form Silicon wafer, which is the basis for further IC fabrication.

A silicon wafer will then go through many processes, including doping, etching, photolithography, metal deposition, during which IC circuits or patterns will be formed on the wafer. Finally, the wafer is cut into dies and packaged as a microprocessor.

Extensive material and energy are consumed in the fabrication of microprocessors, and at the same time a lot of emission is produced. Many procedures, including photoresist used in photolithography involves use of chemicals. It is estimated that for every cm^2 of input wafer,

45.2 g of different chemicals are used [3]. Energy consumption is also huge: more than 3000 kWh of energy is used for every kg of output. Up to 30 L of water is consumed in the production of 1 cm^2 chip, and 445 g of elemental gases (O_2, N_2 etc.) is consumed.

Despite the huge amount of input, the yield of the processes can be as low as 9.5%, meaning that many of the resources are wasted because of the errors in fabrication process.

IX. ENGINEERING ETHICS

In the work of the project, we adhered to IEEE Code of Ethics. We avoided unethical or unlawful behaviors such as plagiarism. We accepted criticism from others and tried to correct our errors. We tried to understand the technological, societal and environmental impact of the technology.

REFERENCES

[1]   Izhikevich, E. M. (2004). Which model to use for cortical spiking neurons? IEEE Transactions on Neural Networks, 15(5), 1063–1070. https://doi.org/10.1109/tnn.2004.832719 W.-K. Chen, Linear

[2]   Corathers, L., Pizzini, S., Calligarich, S., Calligarich, Barron, C., Smith, C., & Barron. (n.d.). Refining silicon. Retrieved December 18, 2021, from https://www.pveducation.org/pvcdrom/manufacturing-si-cells/refining-silicon

[3]   Williams, E. D., Ayres, R. U., & Heller, M. (2002). The 1.7 kilogram microchip: energy and material use in the production of semiconductor devices. Environmental Science & Technology, 36(24), 5504-5510. doi:10.1021/es025643o

[4]   IEEE code of Ethics. (n.d.). Retrieved December 18, 2021, from https://www.ieee.org/content/dam/ieee-org/ieee/web/org/about/corporate/ieee-code-of-ethics.pdf