

**ECE 385**

Spring 2024

Experiment # 1

# **Introduction to TTL**

Jie Wang 3200112404

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TA: Jiebang Xia

## Introduction

In this lab, we build a 2-to-1 MUX with Quartus Prime Simulation and understand the static hazards through the image provided by prof. Chen. Adding a redundant component helps to fix this hazard.

Here is the K-map for 2-to-1 MUX, the formula is  $MUX = B'C + BA$

		BC			
		00	01	11	10
A	0	0	1	0	0
	1	0	1	1	1

$B'C$                        $BA$

Here is the NAND chip representation of the 2-to-1 MUX:

A slight modification of the circuit of Figure 15 is given in Figure 16. Notice that this circuit requires only one 7400, whereas the original design (Figure 13) required three chips to implement. In this example, the conversion to an all NAND implementation reduced the package count by two thirds.

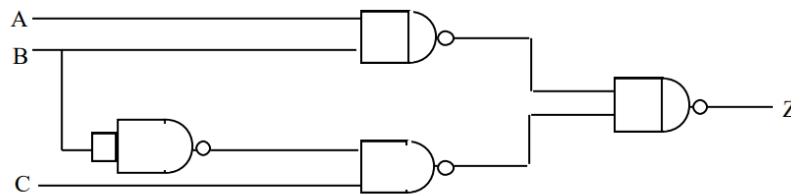
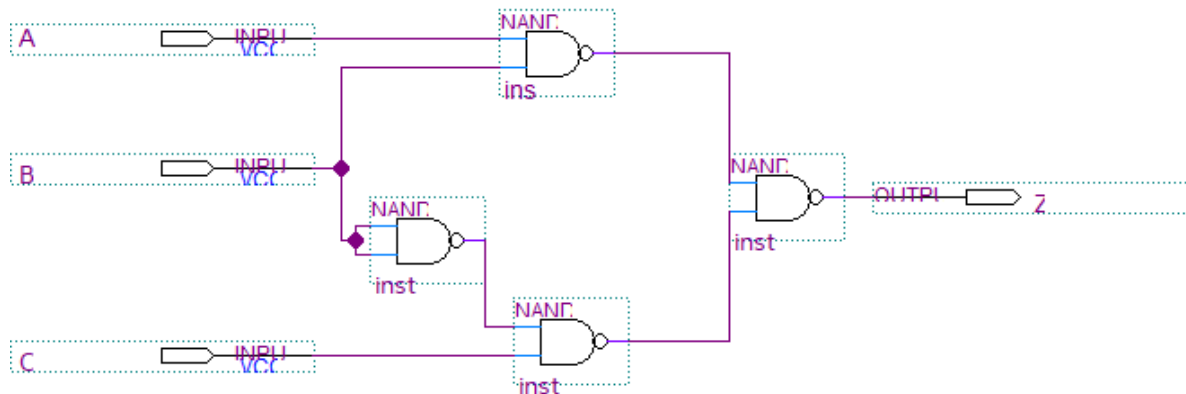


FIGURE 16. Single chip implementation using one 7400 Quad 2-input NANDs

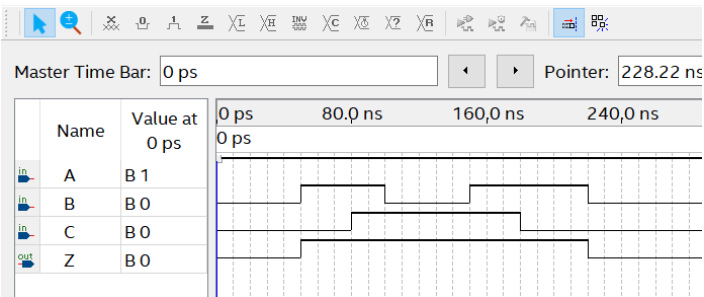
Here is my implementation in the Quartus Prime:



## My waveform:

Simulation Waveform Editor - D:/intelFPGA\_lite/Lab/lab01/ECE385\_Lab\_01 -

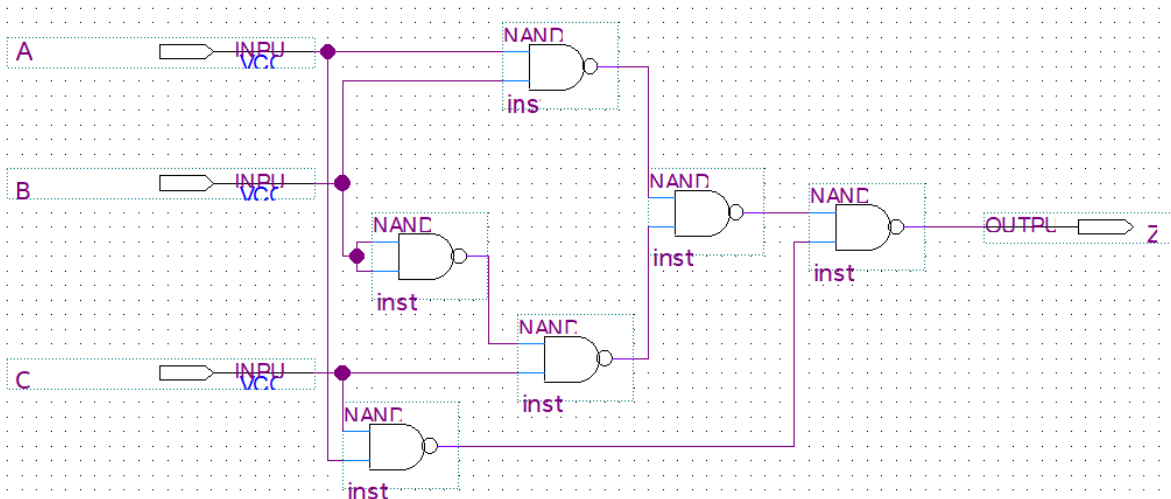
File Edit View Simulation Help



It can be clearly seen that my circuit runs exactly same as the formula.

## Redesign the circuit of part A

Here is the improved version, solving the static hazard caused by the delay of B-Z's extra NAND gate.

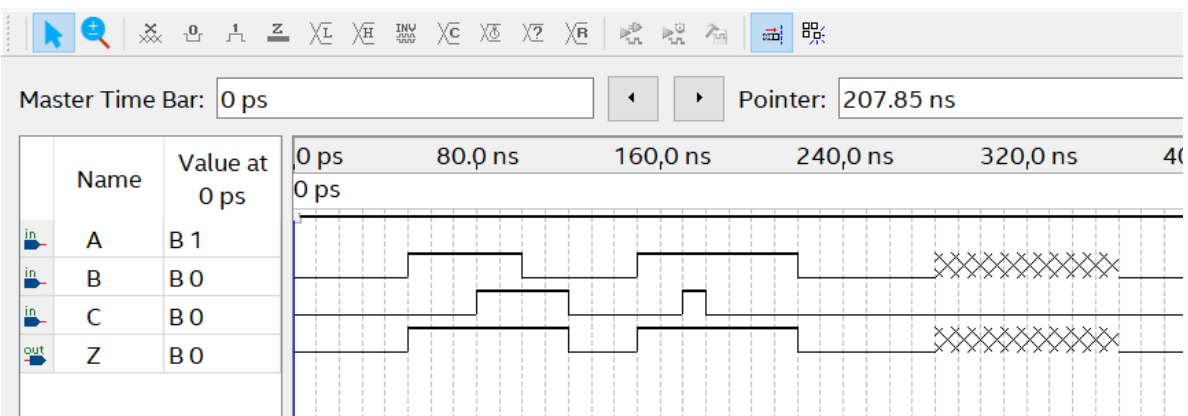


## New waveform:

It behaves the same way as last circuit as it is simulation. Still, my circuit works as expected.

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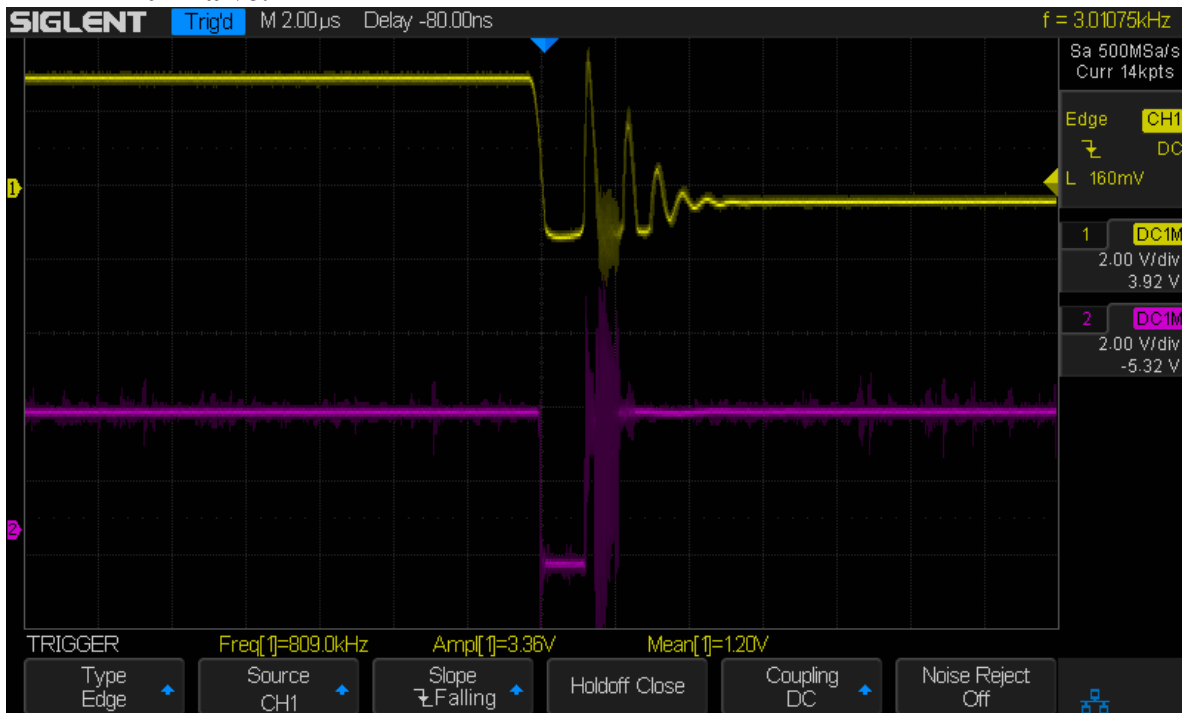
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## Answers to Lab Questions

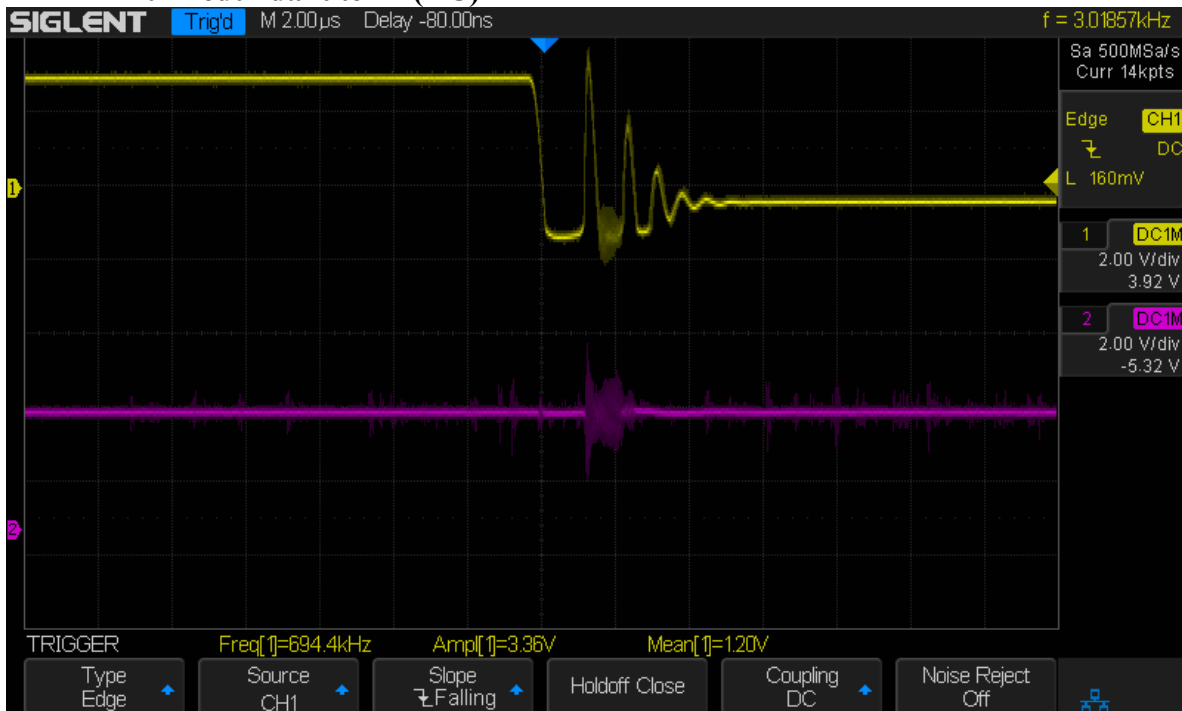
In the lab, we have two images provided by Prof. Chen about the glitch effect observed using oscilloscope.

- **2-1-mux naïve:**



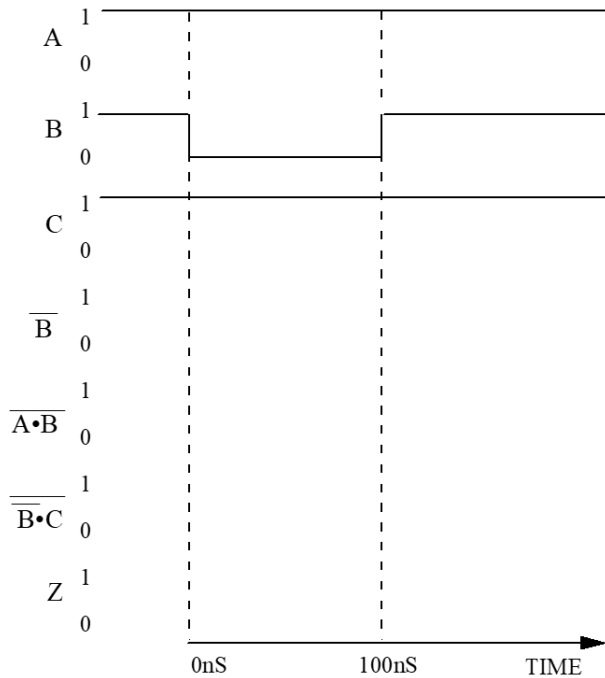
As

- **2-1-mux redundant term (AC)**



## Answers to Post-Lab Questions

1. Given that the guaranteed minimum propagation delay of a 7400 is 0ns and that its guaranteed maximum delay time is 20ns, complete the timing diagram below for the circuit of part A. (See GG.23 if you are not sure how to proceed.)



2. How long does it take the output Z to stabilize on the falling edge of B (in ns)? How long does it take on the rising edge (in ns)? Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.

## Conclusions

Lab01 is pretty straightforward, basically emphasizing on the Quartus Prime configuration. Through this lab, I refresh my memory about the ECE110, ECE120 & ECE220.

