ECE 385

Spring 2024

Experiment # 1

Introduction to TTL

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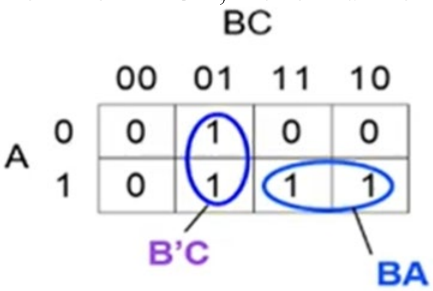
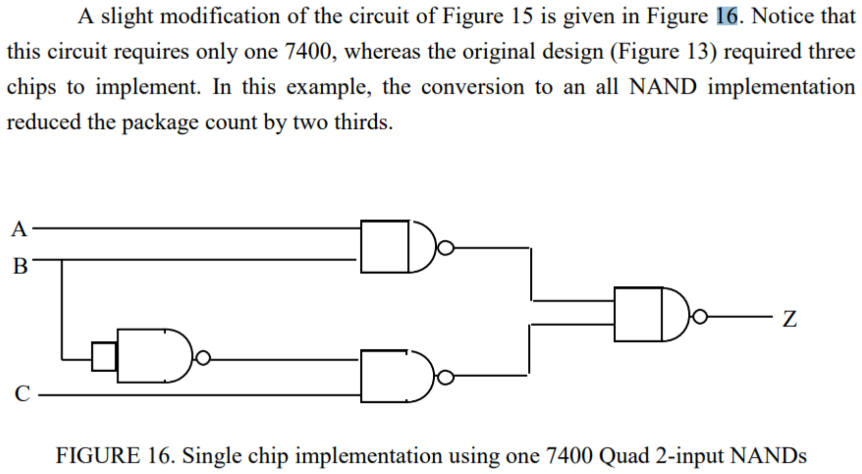
Introduction

In this lab, we build a 2-to-1 MUX with Quartus Prime Simulation and understand the static hazards through the image provided by prof. Chen. Adding a redundant component helps to fix this hazard.

Here is the K-map for 2-to-1 MUX, the formula is $MUX = B'C + BA$



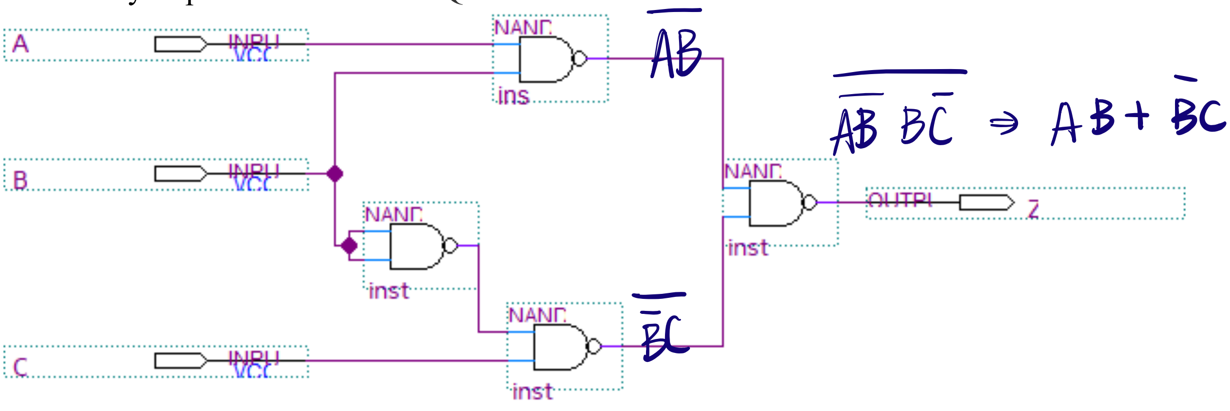
Here is the NAND chip representation of the 2-to-1 MUX:



A slight modification of the circuit of Figure 15 is given in Figure 16. Notice that this circuit requires only one 7400, whereas the original design (Figure 13) required three chips to implement. In this example, the conversion to an all NAND implementation reduced the package count by two thirds.

FIGURE 16. Single chip implementation using one 7400 Quad 2-input NANDs

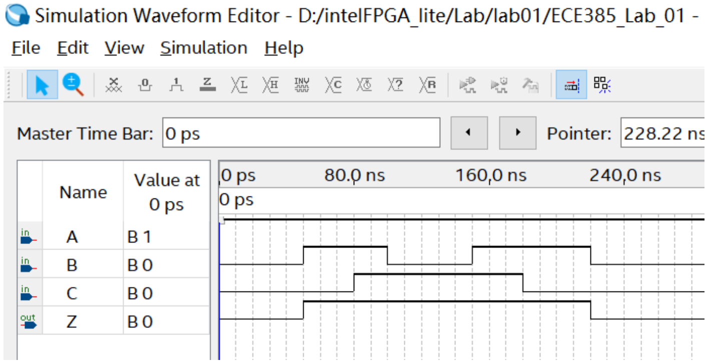
Here is my implementation in the Quartus Prime:



$\overline{\overline{AB}\ B\bar{C}}$ ⇒ $AB + \bar{B}C$

A	B	C	Z
1	0	0	0
1	1	0	1
1	1	1	1
1	0	1	1
1	1	1	1
1	0	0	0

My waveform:


Simulation Waveform Editor - D:/intelFPGA_lite/Lab/lab01/ECE385_Lab_01 -

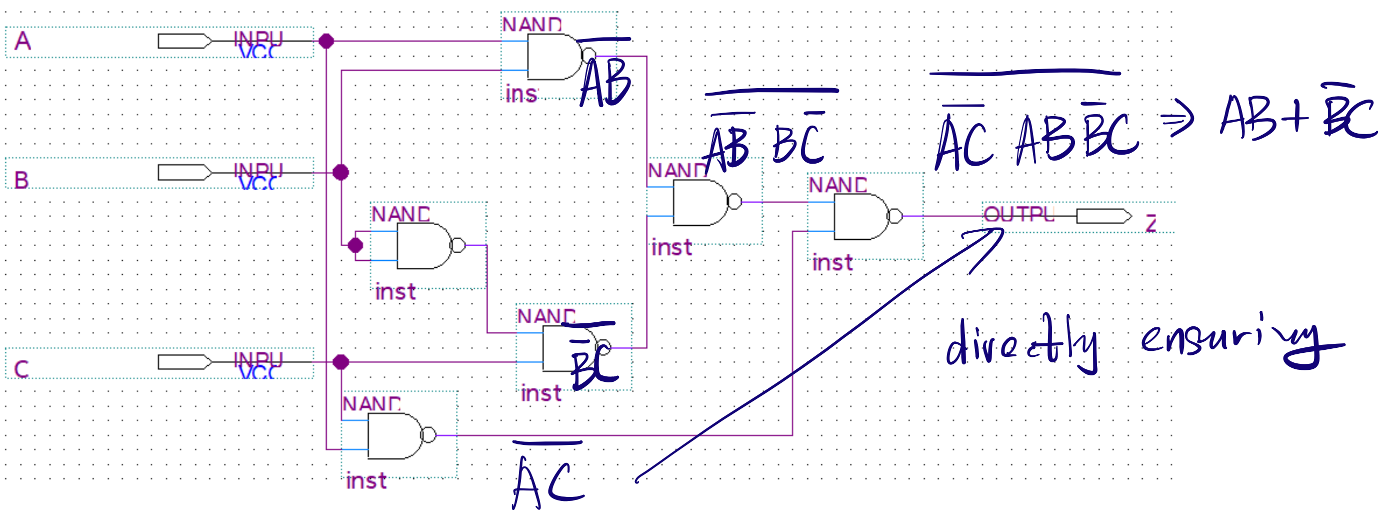
Master Time Bar: 0 ps Pointer: 228.22 ns

Name	Value at 0 ps
A	B 1
B	B 0
C	B 0
Z	B 0

It can be clearly seen that my circuit runs exactly same as the formula.

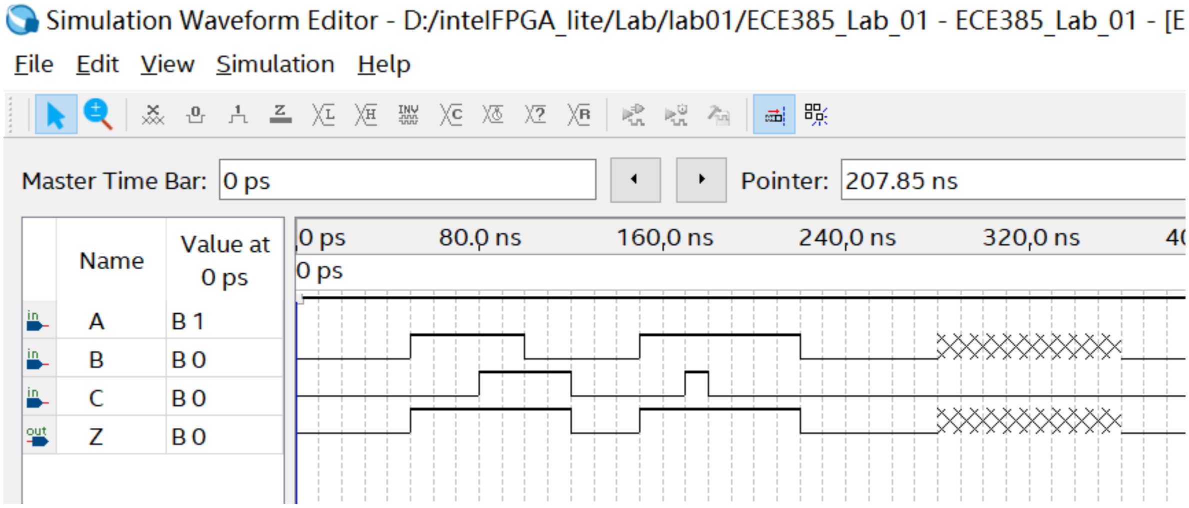
Redesign the circuit of part A

Here is the improved version, solving the static hazard caused by the delay of B-Z’s extra NAND gate.



New waveform:

It behaves the same way as last circuit as it is simulation. Still, my circuit works as expected.


Simulation Waveform Editor - D:/intelFPGA_lite/Lab/lab01/ECE385_Lab_01 - ECE385_Lab_01 - [E

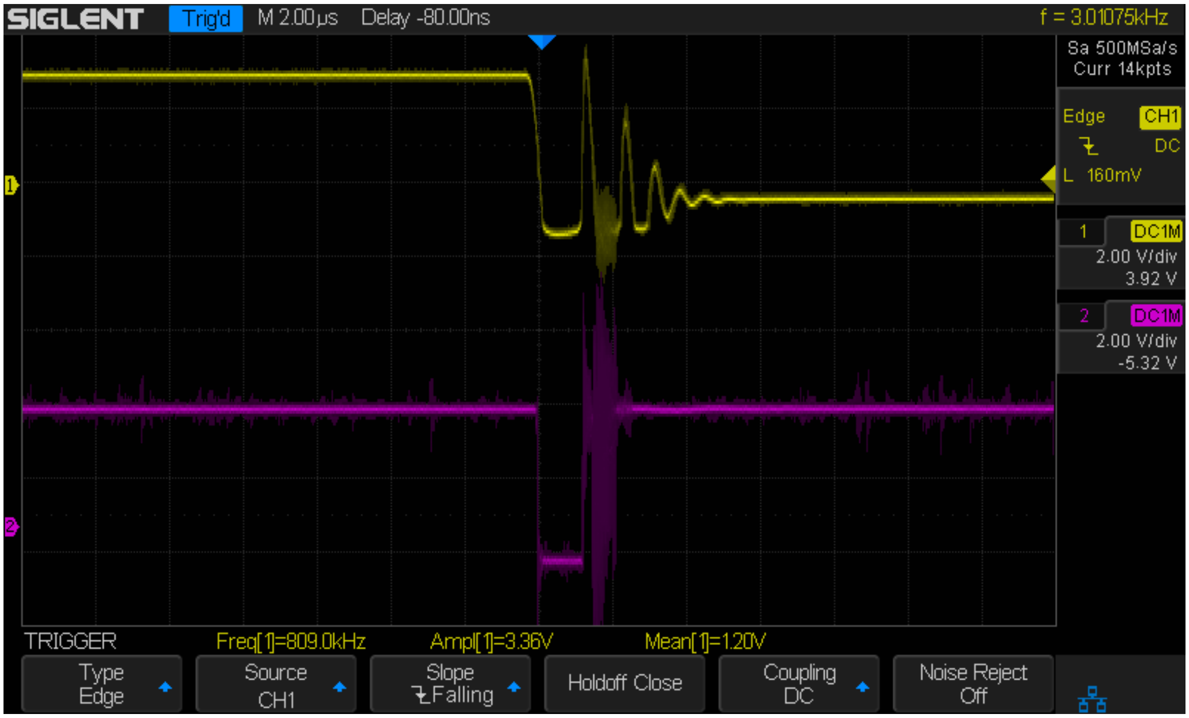
Master Time Bar: 0 ps Pointer: 207.85 ns

Name	Value at 0 ps
A	B 1
B	B 0
C	B 0
Z	B 0

Answers to Lab Questions

In the lab, we have two images provided by Prof. Chen about the glitch effect observed using oscilloscope.

- **2-1-mux naïve:**



M 2.00μs Delay -80.00ns

f = 3.01075kHz

Sa 500MSa/s
Curr 14kpts

Edge CH1
DC
L 160mV

1 DC1M
2.00 V/div
3.92 V

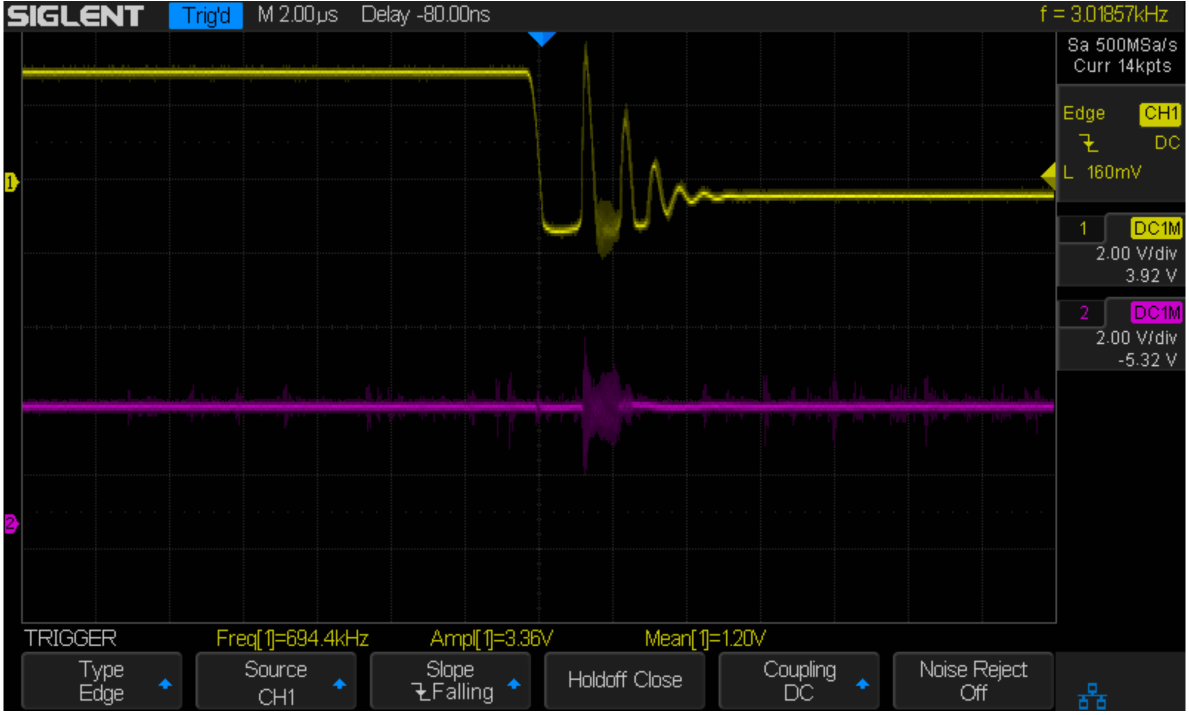
2 DC1M
2.00 V/div
-5.32 V

TRIGGER Freq[1]=809.0kHz Ampl[1]=3.36V Mean[1]=1.20V

Type Edge | Source CH1 | Slope Falling | Holdoff Close | Coupling DC | Noise Reject Off

As

- **2-1-mux redundant term (AC)**



M 2.00μs Delay -80.00ns

f = 3.01857kHz

Sa 500MSa/s
Curr 14kpts

Edge CH1
DC
L 160mV

1 DC1M
2.00 V/div
3.92 V

2 DC1M
2.00 V/div
-5.32 V

TRIGGER Freq[1]=694.4kHz Ampl[1]=3.36V Mean[1]=1.20V

Type Edge | Source CH1 | Slope Falling | Holdoff Close | Coupling DC | Noise Reject Off

Analysis:

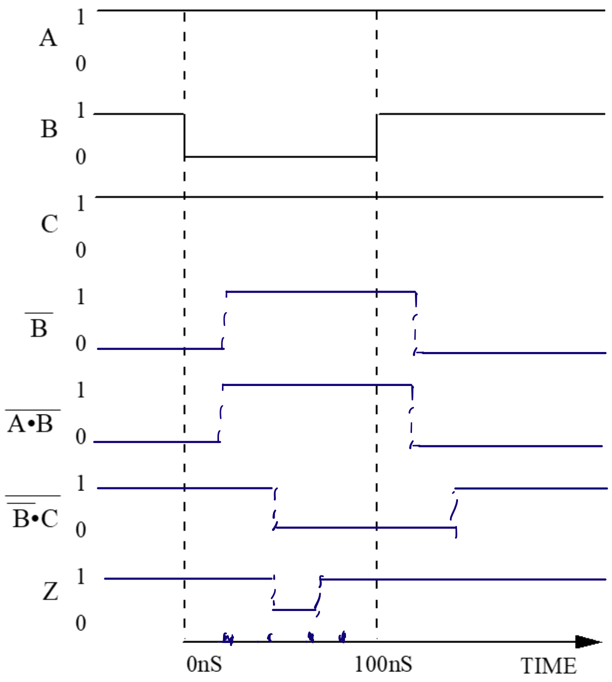
The naive approach cause a subsequent glitch as the signal drops from 1 to 0, this is casused by the delay within circuit

To suppress this glitch, reducing the static hazards we includes a new redundant term, avoiding this happens,

As for the noise, it's hard to handle, we may include filter or trigger to reduce,

Answers to Post-Lab Questions

1. Given that the guaranteed minimum propagation delay of a 7400 is 0ns and that its guaranteed maximum delay time is 20ns, complete the timing diagram below for the circuit of part A. (See GG.23 if you are not sure how to proceed.)



Shown left, delay cause the system failed to reflect the 2-to-1 input.

As $\overline{B}C$ delayed, $\overline{AB}$ gets faster thus making a glitch

2. How long does it take the output Z to stabilize on the falling edge of B (in ns)? How long does it take on the rising edge (in ns)? Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.

Falling: 20ns

rising: 0 ns

As $\overline{B}C$ delayed, $\overline{AB}$ gets faster thus making a glitch

Conclusions

Lab01 is pretty straightforward, basically emphasizing on the Quartus Prime configuration. Through this lab, I refresh my memory about the ECE110, ECE120 & ECE220.

Further, I better understand the necessity of learning HDL to construct FPGA circuit.