ECE 385 Sample Midterm Solution

General Guide and Lab 1

1. How many TTL inputs can a TTL output typically drive?

   a. 1 **b. 10** c. 100 d. unlimited

2. For a circuit with three inputs and zero propagation delay, which of the following input pairs can cause a static-0 hazard?

   a. 000, 111 b. 110, 010 c. 110, 011 **d. none**

3. How to avoid a static hazard?

   a. It is impossible **b. Create redundancy on k-maps** c. Pick a better chip

4. What voltage (VCC) should be used to power your TTL chips?

   a. 0V **b. 5V** c. 1V

5. If a mechanical switch is not debounced, which of the following might occur?

   a. The circuit may not register a desired switch transition.

   b. The circuit may register multiple, undesired switch transitions.

   c. The circuit may receive an undesired voltage spike.

   d. Both (a) and (b).

Lab 2

1. Name one emerging memory technology. **Solution: EEPROM; NVRAM**
2. If the data word is 111001001100 and the odd parity bit read from memory is 1, will the Error LED for odd parity bit verification light on? **Solution: No**
3. Which part of the shift-register storage circuit serves both to receive the input data and to hold the fetched stored data? **Solution: SBR**
4. How do you create a parity error in the RAM? (select all answers)

   a. Run for at least 10 minutes

   b. Unplug one of the four data lines during readc.

   c. Unplug one of the four data lines during write

   d. Turn power off and then on

5. Which of the following statement is false about clock signal in Lab 2

a. If should be generated either by a pulse generator or a debounced switch

b. All the chips should be connected to the same clock signal

c. It can be ANDed with some other signal to control the operation of a shift-register

d. There is a maximum frequency above which the circuit would stop functioning properly

Lab 3

6. The following is a snippet from a transition table,

Current State	Input	Next state
010	1	110
010	0	011
000	0	010
000	1	011
001	1	101
001	0	000

Assuming that the bits are not changing simultaneously (which is almost always the case in real life) during the state transition, which of the following states can the transition from 000 with input 1 can end up in ?

a. 010 with non critical race

b. 110 with critical race

c. 111 with critical race

d. 011 with non critical race

7. A _____ must eventually reach reliable operation from any starting condition (without reset) while _____ must generally be reset to a particular starting state after it is turned on and before actual operation begins. **Solution: self-starting system, non-self-starting system**

8. The simplest two-input one-output circuit that can optionally invert a signal is:

a. AND gate

b. OR gatec. NAND gate

d. XOR gate

Lab 4

9. If the even parity bit for a 2-bit input A,B is generated by A XOR B, which of the following generates even parity bit for 5-bit input P,Q,R,S,T ?
a) (P XOR Q) XOR (R XOR S) XOR T b) ((P XOR Q) XOR R) XOR S) XOR T)
c) None **d) both**

10. The following is a snippet from a transition table,

Current State	Input	Next State
010	1	110
010	0	011
000	0	010

000	1	011
001	1	101
001	0	000

Which of the following states can the transition from 000 with input 1 can end up in?
a) 010 with non critical race **b) 110 with critical race**
c) 111 with critical race d) 011 with non critical race

11. Bit serial processing may be useful for FPGA-based applications because
a) it reduces the routing overhead of design
b) it reduces the amount of logic required by an operation
c) it reduces the latency (in cycles) of an operation
d) a&b
e) a&b&c

12. Is the following statement true or false: If a design simulates it is guaranteed to synthesize.
a) True **b) False**

13. We can trace variables in simulation waveforms. (**True**/False).

Lab 5

14. In lab 6, when do we need to perform ADD?
a) When M=0 **b) When M=1** c) When B[0]=0 d) When B[0]=1

15. Which of the following is a good way to debounce a button like the one typically used to begin execution of your FPGA circuit?
a) A counter. b) A state machine.
c) A D-latch. **d) Both a. and b.** e) Both b. and c.

16. In experiment#6, if the multiplier's MSB is 1 AND multiplicand's MSB is 1, the last step in multiplication involves

a) Subtracting the multiplier from the current partial sum
b) Adding the multiplier to the current partial sum
c) Subtracting the multiplicand from the current partial sum
d) Adding the multiplicand to the current partial sum

Lab 6

17. For ADD instruction, which of the following register operation sequence is in the correct order?

a. PC<- MAR PC<- PC+1 IR <- MDR set cc
b. IR <- MDR set cc PC <- MAR PC<- PC+1
c. IR <- MDR PC<- MAR PC<- PC+1 set cc
d. PC<- MAR PC<- PC+1 set cc IR <- MDR