ZJU-UIUC-INSTITUTE – COURSE SYLLABI

ECE 385 Digital Systems Laboratory

- **Credits: 3**
- **Lecture meeting times and location:**

  Tuesday 08:30-10:30, LTN-A 418
- **Lab meeting times and location:**

  Friday 18:00-20:50; Lab building E-319, D-231, D-225
- **Instructor:**

  Dr. Zuofu Cheng zcheng1@illinois.edu

  Dr. Chushan Li chushan@intl.zju.edu.cn
- **TA:**

  Yinan Yao: Yinan.22@intl.zju.edu.cn E-319

  Ziyang An: ziyang1.23@intl.zju.edu.cn D-231

  Jiebang Xia: jiebang.23@intl.zju.edu.cn D-225
- **Open Lab:**

  Thursday 18:00-20:50 D-231
- **Office Hours:**

  Tuesday 18:30-21:30 (ZJUI Building B313)
- **Course website:**

  Everything is on Blackboard System!
- **Textbook:**
  - Course PPT;

- Lab manual (ECE 385 Lab Manual 20.0_ZJUI Version)
- Online materials on TTL and FPGA.
- Online tutorial books on SystemVerilog.
- Reference books
  - Patt, Yale N., Sanjay J. Patel, and J. Patel. Introduction to Computing Systems: From Bits and Gates to C and Beyond, 2004.
  - John F. Wakerly, Digital Design: Principles and Practices, Prentice Hall, New Jersey, (Third Edition), 2000.
  - Stuart Sutherland, SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, Springer, New York, 2006.
  - James. O. Hamblen and M. J. Furman, Rapid Prototyping of Digital Systems A Tutorial Approach, Kluwer, 2001.
  - Stuart Sutherland and Don Mills, Verilog and SystemVerilog Gotchas, Springer, 2007.
  - Weste, Neil, David Harris, and Ayan Banerjee. “CMOS VLSI Design." A circuits and systems perspective 11 (2005): 739.

Course Goal

The goal of ECE 385 course is to teach students design, build, and test/debug a digital system, which can be a 16-bit microprocessor, a dedicated logic core, or a system-on-a-chip (SoC) platform. Students will learn about the modular design approach, which is the underlining principle of IP-based SoC design methodology. Students will start with TTL logic in the first three weeks to strengthen their skills of using physical logic elements to build relatively complex circuits such as a 4-bit serial processor. Then, the course will make a transition to SystemVerilog and RTL design methodology. The concept of modular design is carried over to SystemVerilog so students would have a concrete understanding of the connection between wired circuits on the proto-board and mapped circuits on the FPGA board, and the RTL design abstraction can be better captured through this process. Students will then start to gradually learn how to design and realize digital circuits using SystemVerilog and the FPGA board. These labs would include 8-bit serial processor, arithmetic units, 16-bit SLC-3 processor, USB input and VGA display, and a simple SoC that connects a NIOS II embedded processor with a dedicated hardware driver for VGA display. Finally, students will have four weeks at the end of the semester to work on an open project of their own choice based on FPGA design with SystemVerilog. This open final project will be graded by creativity, complexity, and functionality of the design. At the conceptual level, students will learn combinational and sequential logic, storage elements, I/O and display, timing analysis, design tradeoffs, synchronous and asynchronous design methods, data-path and controller, microprocessor design, software/hardware co-design, and embedded systems.

Prerequisites

Prerequisites from ECE 110: KVL, KCL, basic circuit analysis, resistors, transistors, LEDs, breadboard wiring and instrument usage

Prerequisites from ECE 120: Boolean algebra, K-maps, combinational and sequential logic, storage elements, CPU building blocks (registers, ALU…)

Prerequisites from ECE 220: C programming, CPU organization, basic data structures, I/O methods

● Course Organization – Overview of Topics

▪ Design on Quartus Prime Schematic and Modelsim Simulation (labs 1-3)

▪ Design on the FPGA (Altera Cyclone IV) using SystemVerilog HDL (Hardware Description Language) (labs 4-6)

▪ Hardware and software co-design using FPGA and embedded CPU (labs 7-9)

▪ Final Project using FPGA board

● Lecture, Lab, and Exam Schedule

Week	Lectures	Lab	Notes	Instructor
1	1/16 In class	1/19 (Lab 1 Introduction)	Simulation	Chushan Li
2	1/23 In class/Zuofu will join online	1/26 (Lab 2 TTL storage)	Simulation	Zuofu Cheng/ Chushan Li
3	2/27 In class	3/1 (Lab 3 Bit-serial processor)	Simulation	Chushan Li
4	3/5 In class	3/8 (Lab 4 Intro-SV-adders)		Chushan Li
5	3/12 In class	3/15 (Lab 5 SV multiplier)		Chushan Li
6	3/19 In class	3/22 (Lab 6 Week 1 SLC-3 CPU)		Chushan Li
7	3/26 Mid-Term Review In class	3/29 (Lab 6 Week 2 SLC-3 CPU)	Midterm on Mon. (4/1)	Chushan Li
8	4/2 In class	4/5 (Lab 7 SoC with NIOS II)		Chushan Li
9	4/9 In class	4/12 (Lab 8 Drivers on NIOS II for USB host and VGA)		Chushan Li
10	4/16 online	4/19 (Lab 9 VGA Text Mode Controller with Avalon-MM Interface)		Zuofu Cheng
11	4/23 online Final Project Kick-off	4/26 (Lab 9 VGA Text Mode Controller with Avalon-MM Interface)		Zuofu Cheng
12	4/30 Review Session	5/3 Optional checkpoint	Final Project starts (proposal due)	Chushan Li
13	5/7 Final Exam In class	5/10 Required checkpoint		Chushan Li
14	5/14 In class Seminar-RAM	5/17 Optional checkpoint		Chushan Li /Zuofu Cheng
15	5/21 In class Seminar-Audio	5/24 Final project demos	Return kits after demo	Chushan Li /Zuofu Cheng

Important notes about the lab session:

- 11 sections, 170-minute weekly meeting (9 labs + mid checkpoint + final demo).
- Each meeting is intended for debugging, measurements and demonstration
- Design, wiring, or coding **must be done outside the regular lab** before coming to the scheduled meeting
- **Do not expect** to complete lab assignment within the 170 minutes without significant preparation

Assignments:

Lab Demo:

- Pre-lab (if there is one) write-up is **required** to begin lab meeting
- Demo points documented on wiki for each lab
- You are responsible for convincing TA that you deserve partial demo points (come up with required tests)
- Lab report due before session one week after lab meeting

A Pre-Lab write-up consists of:

- Demonstrate that you attempted to understand and implement goals in lab
- Answers to questions, if asked in the experiment
- Pre-lab write-up is required to begin lab session (checked off by TA to be included in post-lab)

A Post-Lab write-up consists of:

- Goals of the lab assignment
- Documentation regarding the design process (elaboration of pre-lab)
- Written description of the operation of the circuit
- A block diagram with details of each block
- A logic diagram if applicable
- A component-layout diagram if applicable
- Answer specific questions if asked
- Measurements and analysis of final design (any waveforms, state diagrams, K-maps, simulation results, etc.)

Complete written lab report

- Pre and Post Lab write-ups plus additional details
- **Report must upload to Blackboard System**
- Reports due at 11:59 PM day of next lab (**per group, except for lab 1 which is individual)**
- **All codes also must be uploaded**

Grading policy:

Breakdown of the total points:

- 9 Labs (195 points)
- Final Project (60 points)

- **Midterm Exam – in-class multiple choice (25 points)**
- **Final Exam – in-class multiple choice (25 points)**
- **Peer Evaluation (15 points)**
- Total – 320 Points

Final Project: (60 points)

- 30 points for the proposal and written report
- 20 points for demonstration
- 10 points for difficulty
- See Final Project page on Blackboard System for details

Mid-Term and Final:

- Midterm (40 minutes long) (25 points)
- Sample midterm problems are online (newer set is much more reflective of current exams)
- Final exam (40 minutes long –in class) (25 points)
- Recommendation for exams –**print out lecture slides and take notes!**

Peer Evaluation: Discretionary Points (15 points)

- given by **your partner** in end-of-semester review

9 Labs:

	report	demo	total
experiment 1	15	0	15
experiment 2	15	5	20
experiment 3	15	5	20
experiment 4	15	5	20
experiment 5	15	5	20
experiment 6	20	10	30
experiment 7	15	5	20
experiment 8	15	5	20
experiment 9	20	10	30
Total for 9 labs			195

Partnership, Late Policy, Academic Honesty

- Partnership
  - Partners share the same lab scores and thus the same responsibilities
  - Choose partner carefully (make sure your partner has similar goals, expectations, work ethic)
  - Contact TAs immediately when a conflict or a lack of communication occurs (defined as no contact within 48 hours)
- Cheating Policy
  - Simple definition of cheating–taking someone else's work for credit
  - Every time caught cheating, the student will receive
    - A zero score for the entire lab or the test.

  - A whole letter grade reduction from the student's final grade.
  - Being reported to the college upon any cheating incident.
  - For the SystemVerilog/C codes students submitted after demo, we will use automated similarity detection tool
- Late Policy
  - No late policy for lab reports –upload what you have at 11:59 PM on day it is due and start working on next lab
  - Exceptions will be made for excused illness, family emergency, etc.