ECE 385 – Practice Midterm Sample (2)

1. Assuming we have a fully synchronous TTL design, which signals need to be de-bounced when coming from switches?
a) All input signals from switches
b) Clock only
c) Clock and any load enables
d) Clock and reset
e) Clock, load enables, and reset
We need to de-bounce only clock, assuming the design is fully synchronous. Note that this is a different concept than synchronizing on the FPGA, which is another issue when we cross clock domains.

2. In experiment 2, which of the followings shows the desired memory storage structure?
a) 2 word x 4 bit
b) 4 word x 2 bit
c) 2 word x 2 bit
d) 4 word x 4 bit
Memory is always given in n words x b bits form. There are 4 words because we can address 4 different locations.

3. Which one of these modules' output is asynchronous in experiment 3?
a) Computation Unit
b) Routing Unit
c) Both
d) Neither
Both the routing unit and the computation unit are asynchronous. The only synchronous elements are the flip flops in the state machine (or counter) and the shift registers.

4. True or false: In a carry look-ahead adder, generation of P/G bits (P_n, G_n) requires the value of the previous P/G bits (P_{n-1}, G_{n-1}) to be known.
a) True
b) False
The performance savings from the CLA come from not having dependencies between the various bits for generating the carry, note that P and G can be bitwise computed from the A and B inputs.

5. In the multiplier lab (experiment 5), how is the 9th bit of the adder's sum generated?
a) S8 = S7
b) S8 = C_out7
c) S8 = A7 + B7
d) S8 = A7 + B7 + C_out7
The adder has to be a true 9-bit adder with A and B sign extended as inputs. Otherwise an overflow may occur in an add stage (e.g. 127 + 1).

6. In experiment 6, what is the purpose of the IR?
a) The IR tells the CPU what address it should fetch its next instruction from
b) The IR contains the data that are either written to or read from memory
c) The IR contains the address of memory the CPU is currently operating on
d) The IR contains the current execution cycle's instruction
The instruction register contains the current instruction, which is decoded into the proper control signals.

7. Inside an `always_comb` procedure block, which type of assignment should be used?
a) blocking
b) non-blocking
Combinational logic has implicit ordering, due to their dependencies when drawn out as a schematic.