

CS7381 Project 7: Verilog Code Development – MIPS Data Path Control Unit

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Distance

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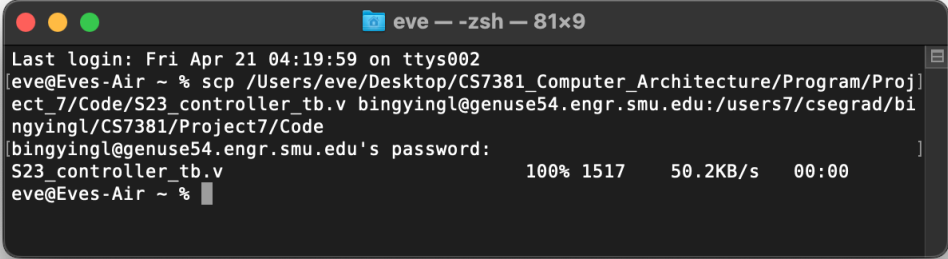
For this exercise, you will write a Verilog code program to implement the MIPS ALU Control Unit. You will test your Control Unit module using the testbench provided in the assignment.

Recall the following web site links for Verilog help:

- http://lyle.smu.edu/manikas/CAD_tool_info.html
- https://s2.smu.edu/manikas/CAD_Tools/Verilog/Xcelium.html.

1. Please download the following Verilog file from the assignment page:

- (a) S23_controller_tb.v - the testbench for testing your Control Unit
- (b) This testbench will have machine code for various MIPS instructions
- (c) See the format of the testbench to help you design your control unit



```
eve — zsh — 81x9
Last login: Fri Apr 21 04:19:59 on ttys002
eve@Eves-Air ~ % scp /Users/eve/Desktop/CS7381_Computer_Architecture/Program/Project_7/Code/S23_controller_tb.v bingyingl@genuse54.engr.smu.edu:/users7/csegrad/bingyingl/CS7381/Project7/Code
bingyingl@genuse54.engr.smu.edu's password:
S23_controller_tb.v                                100% 1517    50.2KB/s   00:00
eve@Eves-Air ~ %
```

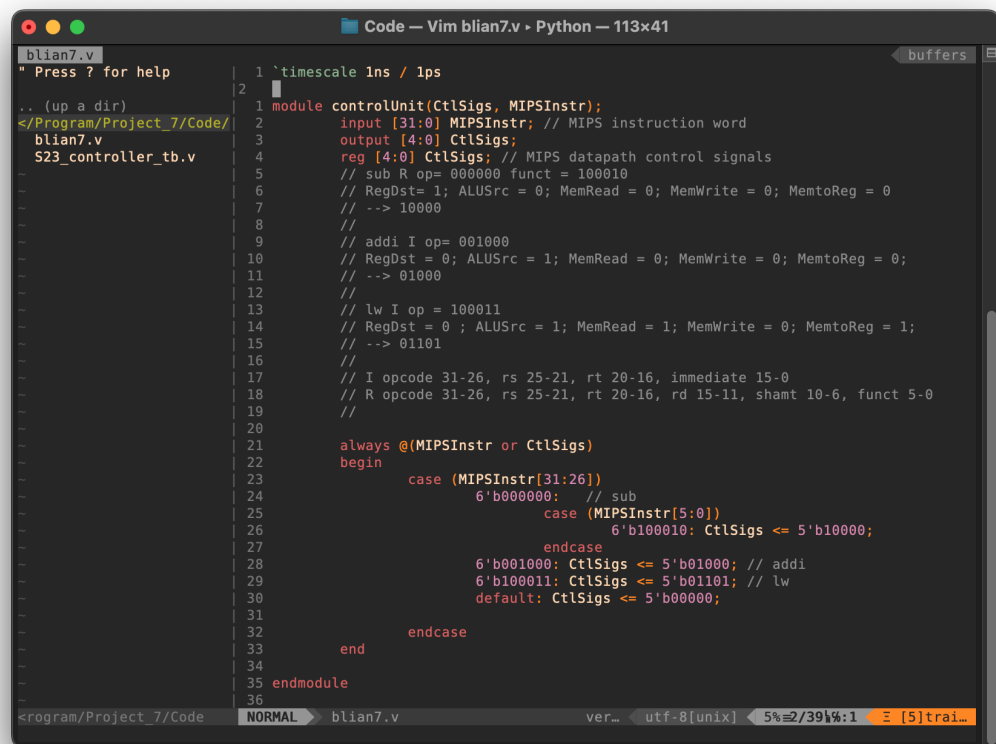
Depending on the testbench we can analyse the right result of these tests.

4. For other MIPS instructions, set these control signals to 0.

```
RegDst = 0 ; ALUSrc = 0; MemRead = 0; MemWrite = 0; MemtoReg = 0;
```

5. Develop the MIPS control unit in Verilog.

- (a) Save the program as a *.v file – use the first initial of your first name and the first 4 letters of your last name, then the number 3 (to distinguish from your code for previous Verilog projects). For example, my file submission name would be tmani3.v.



```
blan7.v
" Press ? for help
.. (up a dir)
~/Program/Project_7/Code/
blan7.v
S23_controller_tb.v

1 `timescale 1ns / 1ps
2
3 module controlUnit(CtlSigs, MIPSInstr);
4     input [31:0] MIPSInstr; // MIPS instruction word
5     output [4:0] CtlSigs; // MIPS datapath control signals
6     // sub R op= 000000 funct = 100010
7     // RegDst= 1; ALUSrc = 0; MemRead = 0; MemWrite = 0; MemtoReg = 0
8     // --> 10000
9     //
10    // addi I op= 001000
11    // RegDst = 0; ALUSrc = 1; MemRead = 0; MemWrite = 0; MemtoReg = 0;
12    // --> 01000
13    //
14    // lw I op = 100011
15    // RegDst = 0 ; ALUSrc = 1; MemRead = 1; MemWrite = 0; MemtoReg = 1;
16    // --> 01101
17    //
18    // I opcode 31-26, rs 25-21, rt 20-16, immediate 15-0
19    // R opcode 31-26, rs 25-21, rt 20-16, rd 15-11, shamt 10-6, funct 5-0
20    //
21    always @(MIPSInstr or CtlSigs)
22    begin
23        case (MIPSInstr[31:26])
24            6'b000000: // sub
25                case (MIPSInstr[5:0])
26                    6'b100010: CtlSigs <= 5'b10000;
27                endcase
28            6'b001000: CtlSigs <= 5'b01000; // addi
29            6'b100011: CtlSigs <= 5'b01101; // lw
30            default: CtlSigs <= 5'b00000;
31        endcase
32    end
33 endmodule
34
35
36
```

- (b) Test your Control Unit using the testbench provided in Step 1.

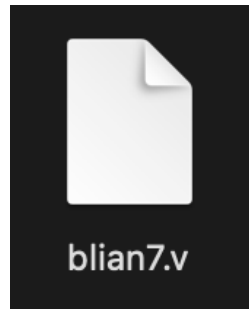
```
eve — -zsh — 81x9
eve@Eves-Air ~ % scp /Users/eve/Desktop/CS7381_Computer_Architecture/Program/Project_7/Code/blian7.v bingyingl@genuse54.engr.smu.edu:/users7/csegrad/bingyingl/CS7381/Project7/Code
bingyingl@genuse54.engr.smu.edu's password:
blian7.v 100% 975 22.4KB/s 00:00
eve@Eves-Air ~ %
```

```
eve — ssh bingyingl@genuse54.smu.edu — 95x47
bingyingl@genuse54.engr.smu.edu$ xmverilog blian7.v S23_controller_tb.v
/usr/local/cds2008/XCELIUM/tools/bin/xmverilog
T00L: xmverilog 21.09-s002: Started on Apr 21, 2023 at 04:43:41 CDT
T00L: xmverilog 21.09-s002: Started on Apr 21, 2023 at 04:43:41 CDT
xmverilog(64): 21.09-s002: (c) Copyright 1995-2021 Cadence Design Systems, Inc.
file: blian7.v
    module worklib.controlUnit:v
        errors: 0, warnings: 0
file: S23_controller_tb.v
    module worklib.test_controlUnit:v
        errors: 0, warnings: 0
        Caching library 'worklib' ..... Done
    Elaborating the design hierarchy:
    Building instance overlay tables: ..... Done
    Generating native compiled code:
        worklib.controlUnit:v <0x3092b326>
            streams: 2, words: 780
        worklib.test_controlUnit:v <0x5c24c790>
            streams: 6, words: 7132
    Building instance specific data structures.
    Loading native compiled code: ..... Done
    Design hierarchy summary:
        Instances Unique
    Modules:      2      2
    Registers:    2      2
    Vectored wires: 2      -
    Always blocks: 1      1
    Initial blocks: 4      4
    Pseudo assignments: 1      1
    Simulation timescale: 1ps
    Writing initial simulation snapshot: worklib.test_controlUnit:v
    Loading snapshot worklib.test_controlUnit:v ..... Done
xcelium> source /usr/local/cds2008/XCELIUM/tools/xcelium/files/xmsimrc
xcelium> run
        opcode RegDst ALUSrc MemRead MemWrite MemtoReg
        0 000000 x      x      x      x      x
        2 001111 0      0      0      0      0
        4 100011 0      1      1      0      1
        8 001111 0      0      0      0      0
       10 000000 0      0      0      0      0
       12 001000 0      1      0      0      0
       14 000000 1      0      0      0      0
Simulation complete via $finish(1) at time 114 NS + 0
./S23_controller_tb.v:36 #finishtime $finish;
xcelium> exit
T00L: xmverilog 21.09-s002: Exiting on Apr 21, 2023 at 04:43:43 CDT (total: 00:00:02)
bingyingl@genuse54.engr.smu.edu$
```

Compare the result with testbench annotation and table they are the same and mapped correctly.

6. Please include the following for your homework submission:

- (a) Your Control Unit Verilog file – submit the actual *.v file so that the grader can run them.



- (b) Your testbench results – this can be a copy of the results on a Word document.
I download the result file log from the server and modify the name as blian7.log

A terminal window with a dark background and light text. The title bar at the top says "eve - zsh - 81x9". The terminal shows a user at a prompt typing an SCP command to download a file from a remote server. The command is: `scp bingyingl@genuse54.engr.smu.edu:/users7/csegrad/bingyingl/CS7381/Project7/Code/xmverilog.log /Users/eve/Desktop/CS7381_Computer_Architecture/Program/Project_7/Result`. The prompt then shows the user's password being entered. The next line shows the file being downloaded: `xmverilog.log`. The progress bar shows 100% completion, with a file size of 1819 bytes, a transfer rate of 37.2KB/s, and a time of 00:00. The prompt then shows the user's name and the terminal is ready for the next command.

```
eve@Eves-Air ~ % scp bingyingl@genuse54.engr.smu.edu:/users7/csegrad/bingyingl/CS7381/Project7/Code/xmverilog.log /Users/eve/Desktop/CS7381_Computer_Architecture/Program/Project_7/Result
bingyingl@genuse54.engr.smu.edu's password:
xmverilog.log                                100% 1819    37.2KB/s   00:00
eve@Eves-Air ~ %
```

```

xmvverilog(64): 21.09-s002: (c) Copyright 1995-2021 Cadence Design Systems, Inc.
TOOL:  xmvverilog  21.09-s002: Started on Apr 21, 2023 at 04:43:41 CDT
xmvverilog
  blian7.v
  S23_controller_tb.v
file: blian7.v
  module worklib.controlUnit:v
    errors: 0, warnings: 0
file: S23_controller_tb.v
  module worklib.test_controlUnit:v
    errors: 0, warnings: 0
    Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Building instance overlay tables: ..... Done
Generating native compiled code:
  worklib.controlUnit:v <0x3092b326>
    streams: 2, words: 780
  worklib.test_controlUnit:v <0x5c24c790>
    streams: 6, words: 7132
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances  Unique
Modules:         2      2
Registers:       2      2
Vectored wires:  2      -
Always blocks:   1      1
Initial blocks:  4      4
Pseudo assignments: 1      1
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.test_controlUnit:v
Loading snapshot worklib.test_controlUnit:v ..... Done
xcelium> source /usr/local/cds2008/XCELIUM/tools/xcelium/files/xmsimrc
xcelium> run
      opcode RegDst ALUSrc MemRead MemWrite MemtoReg
      0 000000 x  x  x  x  x
      2 001111 0  0  0  0  0
      4 100011 0  1  1  0  1
      8 001111 0  0  0  0  0
     10 000000 0  0  0  0  0
     12 001000 0  1  0  0  0
     14 000000 1  0  0  0  0
Simulation complete via $finish(1) at time 114 NS + 0
./S23_controller_tb.v:36      #finishtime $finish;
xcelium> exit
TOOL:  xmvverilog  21.09-s002: Exiting on Apr 21, 2023 at 04:43:43 CDT  (total: 00:00:02)

```

(c) PLEASE MAKE SURE THAT YOUR NAME APPEARS ON ALL SUBMITTED ITEMS FOR PROPER CREDIT