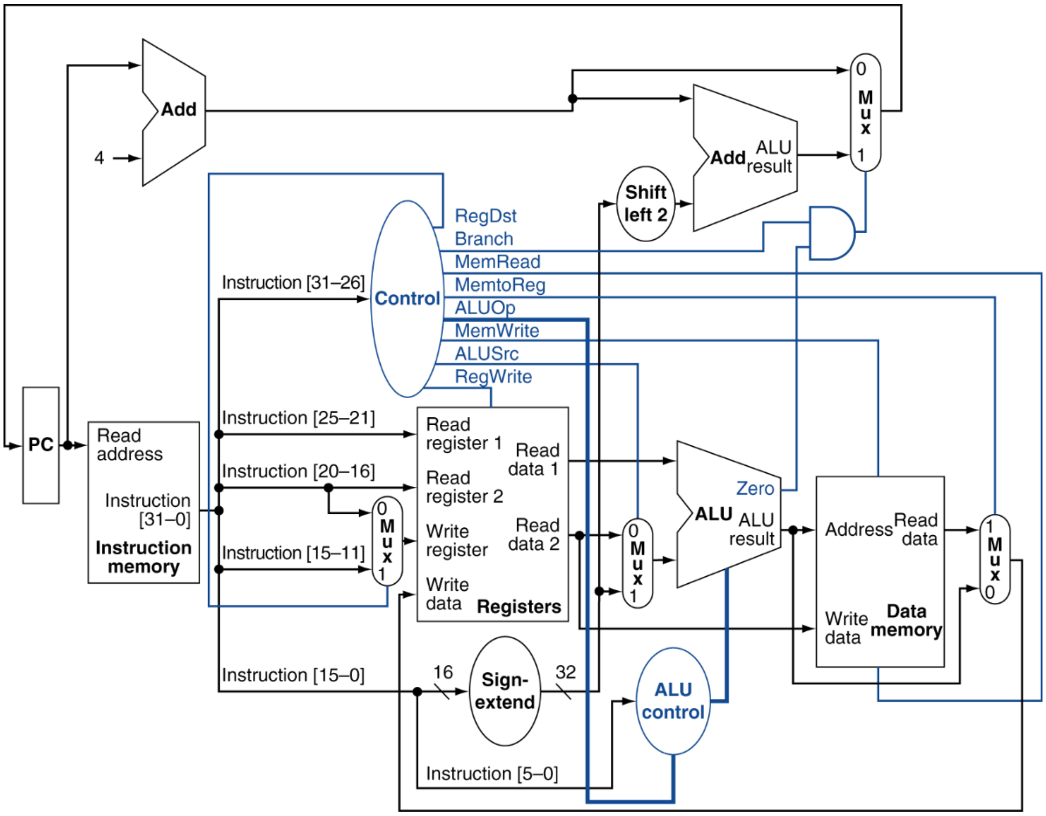
1 Project 7: Verilog Code Development – MIPS Data Path Control Unit

10 points

For this exercise, you will write a Verilog code program to implement the MIPS Data Path Control Unit. You will test your Control Unit module using the testbench provided in the assignment.

Please see the figure MIPS Data Path with Control Signals to help guide your design. You may also want to refer to the previous lecture slides on the MIPS Processor (Appendix A).



Also recall the following web site links for Verilog help:

- http://lyle.smu.edu/~manikas/CAD_tool_info.html
- https://s2.smu.edu/~manikas/CAD_Tools/Verilog/Xcelium.html

1. Please download the following Verilog file from the assignment page:
    a. **S23_controller_tb.v** - the testbench for testing your Control Unit
    b. This testbench will have machine code for various MIPS instructions
    c. See the format of the testbench to help you design your control unit
2. For simplicity in design, your control unit will just need to decode the following MIPS instructions: **sub, addi**, and **lw**.
3. For these instructions, your control unit will need to output the correct values for the following control signals:
    a. RegDst
    b. ALUSrc
    c. MemRead
    d. MemWrite
    e. MemtoReg
4. **For other MIPS instructions, set these control signals to 0.**
5. Develop the MIPS control unit in Verilog.
    a. Save the program as a *.v file – use the first initial of your first name and the first 4 letters of your last name, then the number 3 (to distinguish from your code for previous Verilog projects). For example, my file submission name would be **tmani3.v.**
    b. Test your Control Unit using the testbench provided in Step 1.
6. **Please include the following for your homework submission:**
    a. Your Control Unit Verilog file – **submit the actual *.v file so that the grader can run them.**
    b. Your testbench results – this can be a copy of the results on a Word document.
    c. **PLEASE MAKE SURE THAT YOUR NAME APPEARS ON ALL SUBMITTED ITEMS FOR PROPER CREDIT**

2 SOLUTION

2.1 Verilog code: MIPS Data Path Control Unit

An example of the Verilog code solution is the following:

```
//==============================================================
// tmani3.v
// T. Manikas    2022 Dec 29
//
// Control Unit for MIPS processor datapath
//
// decodes MIPS instruction word
// and generates control signals for MIPS datapath
//
//==============================================================

`timescale 1ns / 1ps

module controlUnit(CtlSigs, MIPSInstr);

   input [31:0] MIPSInstr;      // MIPS instruction word
   output [4:0] CtlSigs;        // MIPS datapath control signals
   // order is RegDst, ALUSrc, MemRead, MemWrite, MemtoReg
   reg      [4:0] CtlSigs;

     always @(MIPSInstr)
     begin
      case (MIPSInstr[31:26])
        6'b000000:  CtlSigs = 5'b10000;    // R-type (sub)
        6'b001000:  CtlSigs = 5'b01000;    // addi
        6'b100011:  CtlSigs = 5'b01101;    // lw
        default:  CtlSigs = 5'b00000;    // set all ctl sigs to 0
      endcase
     end

endmodule // controlUnit
```

2.2 Testbench results

```
opcode RegDst ALUSrc MemRead MemWrite MemtoReg
  0   000000      1     0     0     0     0
  2   001111      0     0     0     0     0
  4   100011      0     1     1     0     1
  8   001111      0     0     0     0     0
 10   000000      1     0     0     0     0
 12   001000      0     1     0     0     0
 14   000000      1     0     0     0     0
```