CS7381 Project 7: Verilog Code Development – MIPS Data Path Control Unit

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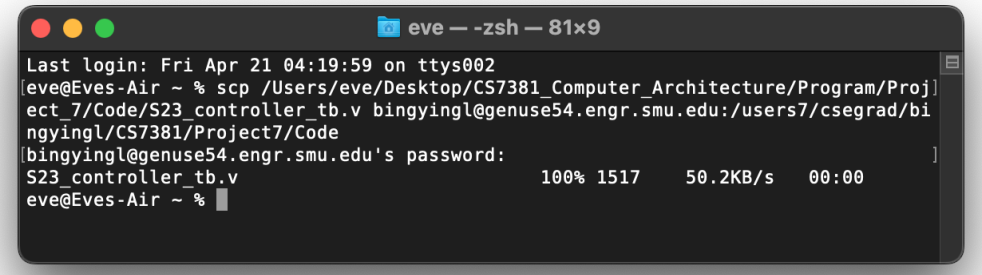
For this exercise, you will write a Verilog code program to implement the MIPS ALU Control Unit. You will test your Control Unit module using the testbench provided in the assignment.

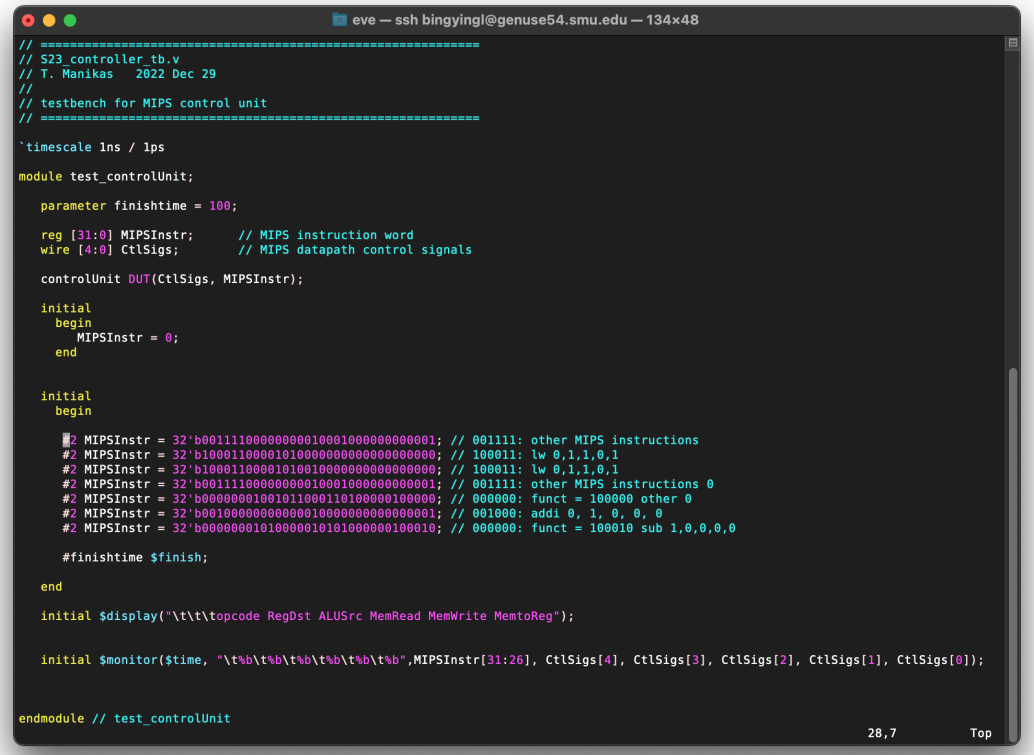
Recall the following web site links for Verilog help:

- http://lyle.smu.edu/ manikas/CAD_tool_info.html
- https://s2.smu.edu/ manikas/CAD_Tools/Verilog/Xcelium.html.

1. Please download the following Verilog file from the assignment page:
   (a) S23_controller_tb.v - the testbench for testing your Control Unit
   (b) This testbench will have machine code for various MIPS instructions
   (c) See the format of the testbench to help you design your control unit



Depending on the testbench we can analyis the right result of these test.



2. For simplicity in design, your control unit will just need to decode the following MIPS instructions: sub, addi, and lw.

```
sub: R; opcode = 000000; funct = 100010
addi: I; opcode = 001000;
lw: I; opcode = 100011;
```

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3. For these instructions, your control unit will need to output the correct values for the following control signals:

   (a) RegDst
   (b) ALUSrc
   (c) MemRead
   (d) MemWrite
   (e) MemtoReg

```
lw: RegDst = 0 ; ALUSrc = 1; MemRead = 1; MemWrite = 0; MemtoReg = 1;
addi: RegDst = 0; ALUSrc = 1; MemRead = 0; MemWrite = 0; MemtoReg = 0;
sub: RegDst= 1; ALUSrc = 0; MemRead = 0; MemWrite = 0; MemtoReg = 0;
```

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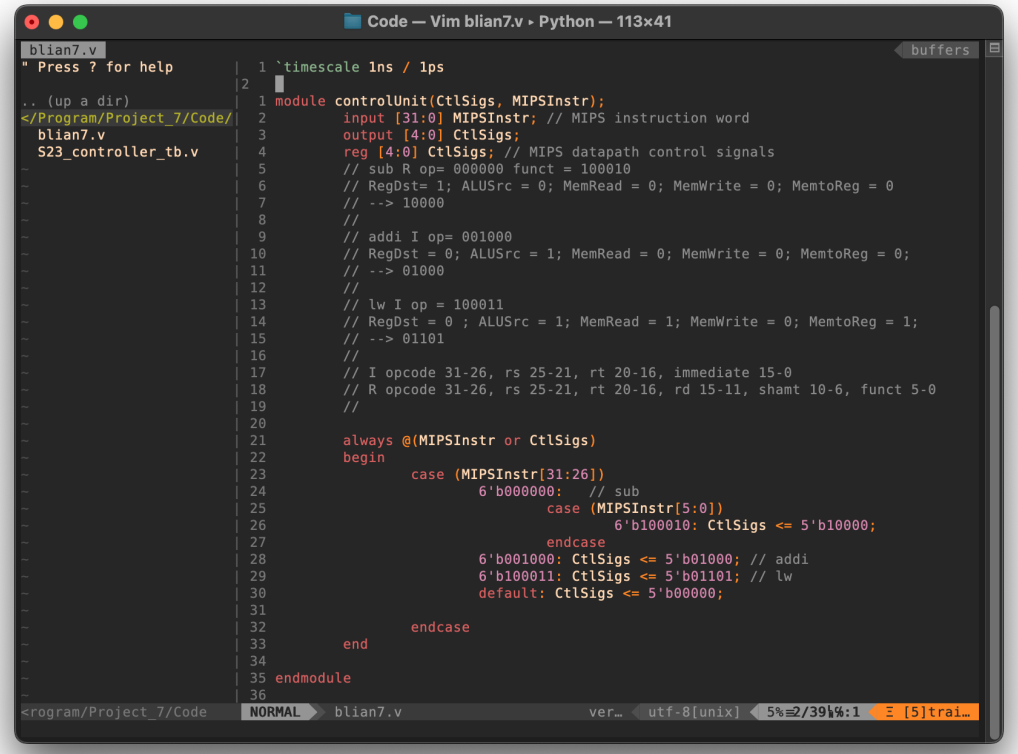
4. For other MIPS instructions, set these control signals to 0.

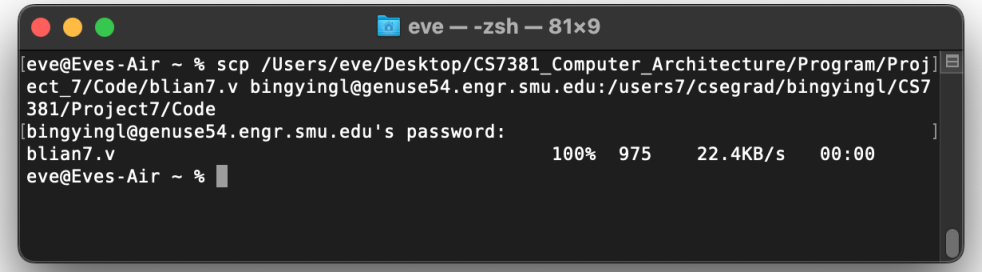
```
RegDst = 0 ; ALUSrc = 0; MemRead = 0; MemWrite = 0; MemtoReg = 0;
```

5. Develop the MIPS control unit in Verilog.

   (a) Save the program as a *.v file – use the first initial of your first name and the first 4 letters of your last name, then the number 3 (to distinguish from your code for previous Verilog projects). For example, my file submission name would be tmani3.v.



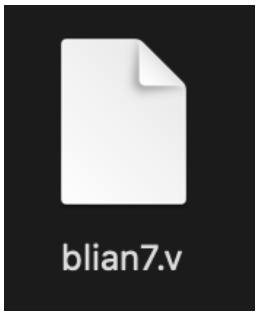
   (b) Test your Control Unit using the testbench provided in Step 1.



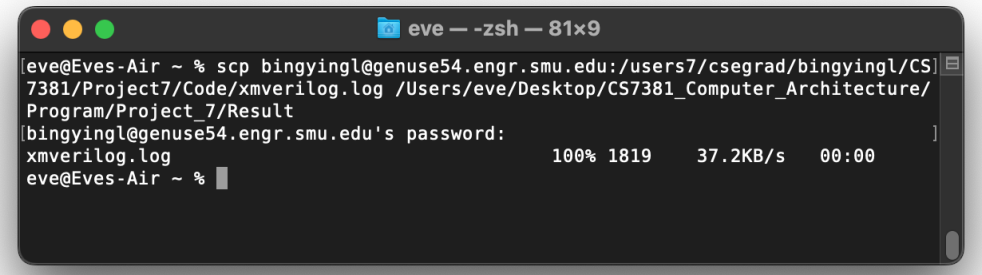
Compare the result with testbench annotation and table they are the same and mapped correctly.

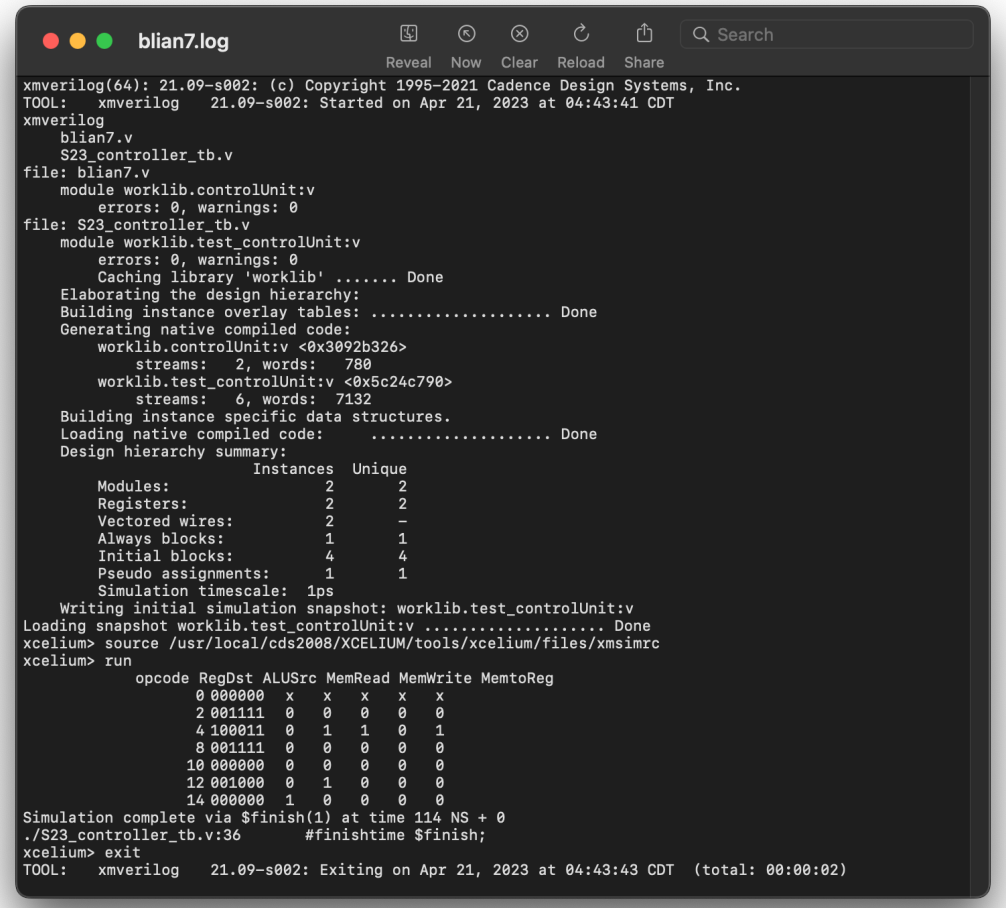
6. Please include the following for your homework submission:

(a) Your Control Unit Verilog file – submit the actual *.v file so that the grader can run them.



(b) Your testbench results – this can be a copy of the results on a Word document.
I download the result file log from the server and modify the name as blian7.log





(c) PLEASE MAKE SURE THAT YOUR NAME APPEARS ON ALL SUBMITTED ITEMS FOR PROPER CREDIT