Results

NOTE: this is the SOLUTION to Quiz 4.

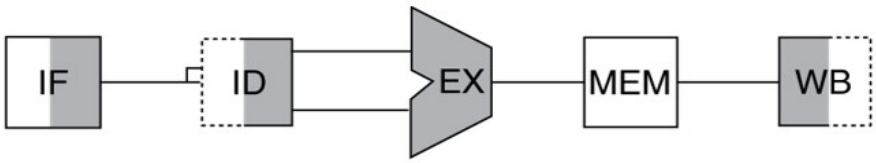
The correct answers are indicated for each question, with explanations as needed.

Dr. Manikas

Your Answers:

1 4 / 4 points

We are using our MIPS pipeline with the five stages as shown below:



We are also given the following instruction sequence for our 5-stage MIPS pipeline:

```
SUB R5, R2, R1
ADD R3, R5, R0
OR  R4, R5, R2
AND R6, R3, R0
```

Identify the registers that have **data hazards** (check all that apply):

- [ ] R1
- [ ] R4
- [ ] R6
- [x] R3
- [ ] R2
- [x] R5

- [ ] R0

Feedback

General Feedback

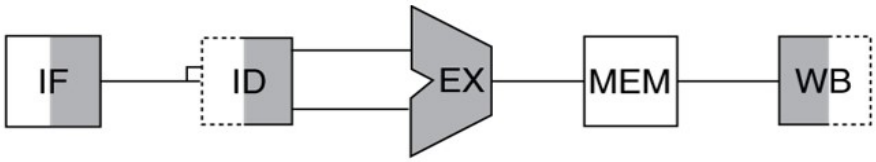
```
SUB R5, R2, R1

ADD R3, R5, R0

OR   R4, R5, R2

AND R6, R3, R0
```

"SUB" produces result in R5 that is input to "ADD" and "OR", so register R5 has a data hazard

"ADD" produces result in R3 that is input to "AND", so register R3 has a data hazard

2 4 / 4 points

We are using our MIPS pipeline with the five stages as shown below:



We are also given the following instruction sequence for our 5-stage MIPS pipeline:

```
ADD R0, R2, R1
OR  R4, R0, R3
SUB R5, R0, R2
AND R6, R4, R3
```

Identify the registers that have **data hazards** (check all that apply):

- [x] R4
- [ ] R5
- [x] R0
- [ ] R3

- [ ] R1
- [ ] R2
- [ ] R6

Feedback

General Feedback

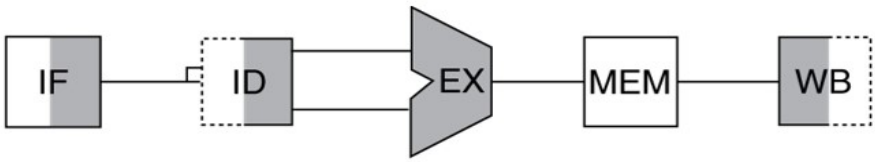
```
ADD  R0, R2, R1

OR   R4, R0, R3

SUB  R5, R0, R2

AND  R6, R4, R3
```

"ADD" produces result in R0 that is input to "OR" and "SUB", so register R0 has a data hazard

"OR" produces result in R4 that is input to "AND", so register R4 has a data hazard

3 4 / 4 points

We are using our MIPS pipeline with the five stages as shown below:



We are also given the following instruction sequence for our 5-stage MIPS pipeline:

```
ADD  R5, R2, R1
SW   R5, 32(R1)
SUB  R3, R5, R0
```

How many stalls are required after the ADD instruction?

- [ ] 1
- [ ] 4

- [x] 2
- [ ] 3
- [ ] 0

Feedback

General Feedback

There is a data hazard in register R5

Clock Cycle (CC)	1	2	3	4	5	6
ADD R5, R2, R1	IF	ID	EX	MEM	WB	
SW R5, 32(R1)		IF	ID	EX	MEM	WB

SW uses register R5 as an input register during its ID stage (CC 3), but R5 is not updated until ADDIs WB stage (CC 5). Therefore, we need to stall the SW instruction by **2** cycles.

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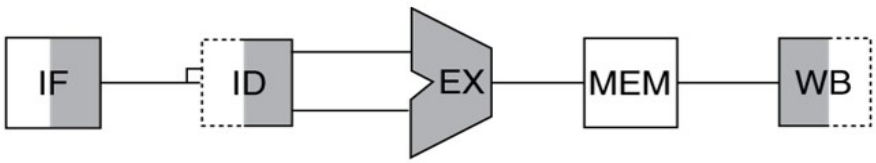
4 4 / 4 points

We are using our MIPS pipeline with the five stages as shown below:



We are also given the following instruction sequence for our 5-stage MIPS pipeline:

```
ADD  R5, R2, R1
SW   R5, 32(R1)
SUB  R3, R5, R0
```

How many stalls are required after the SW instruction?

- [ ] 3
- [ ] 4

2

✓ 0

1

Feedback

General Feedback

SW uses register R5 as an input register during its ID stage (CC 3), but does not change the value of R5.

SUB also uses register R5 as an input. However, since SW does not change the value of R5, there is no data hazard.

Therefore, **0** stalls are required.

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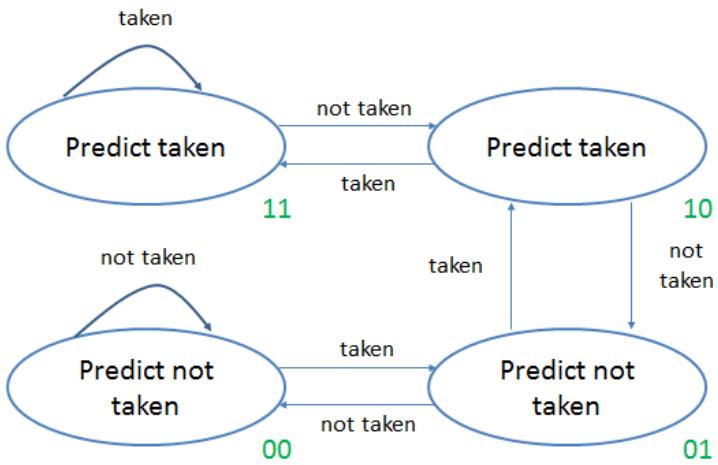
5 4 / 4 points

We have a sequence of branch outcomes, where T = branch taken, and NT = branch not taken. What is the **accuracy** of the **two-bit branch predictor** for the following sequence, assuming that the predictor starts in state **00**?
Sequence is: **T, NT, NT, NT, NT**



✓ 80%

Feedback

General Feedback

We are starting in the the lower left state (00), so we follow the sequence as

Current state	Prediction	Branch outcome	Accurate?	Next state
00	NT	T	No	01
01	NT	NT	Yes	00
00	NT	NT	Yes	00
00	NT	NT	Yes	00
00	NT	NT	Yes	00

So the 2-bit predictor is accurate 4/5 time = **80%** for this sequence