CS7381 Project 4
Verilog Code Development using Cadence Xcelium

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Distance

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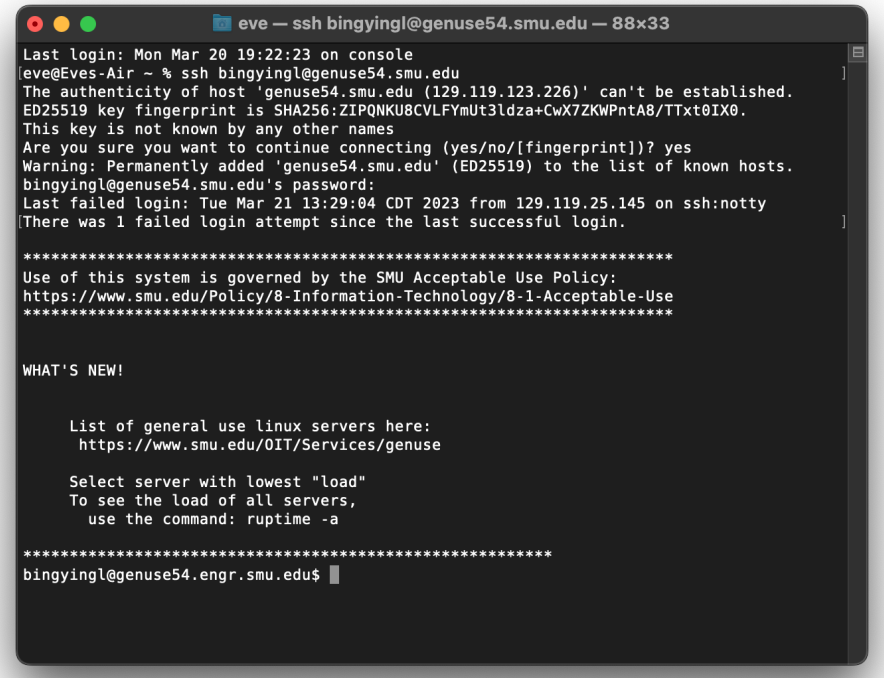
In previous projects, we learned how to use the MARS tool to develop and simulate MIPS assembly code. Next, we will use the Verilog HDL (Hardware Description Language) to develop and simulate various MIPS components.

We will use the Cadence Xcelium tool on the Lyle Unix servers. Please go to my web site Links to an external site. for information on how to do the following steps:

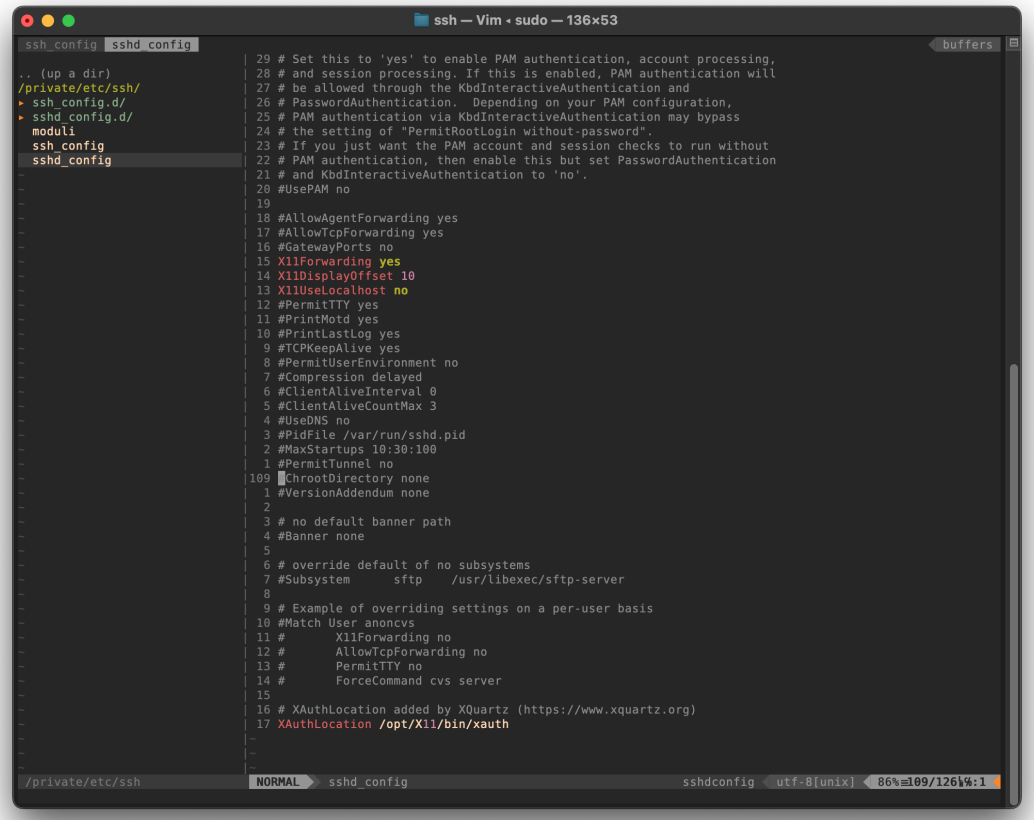
1. Obtain a Lyle Unix account, if you do not already have one: Links to an external site.

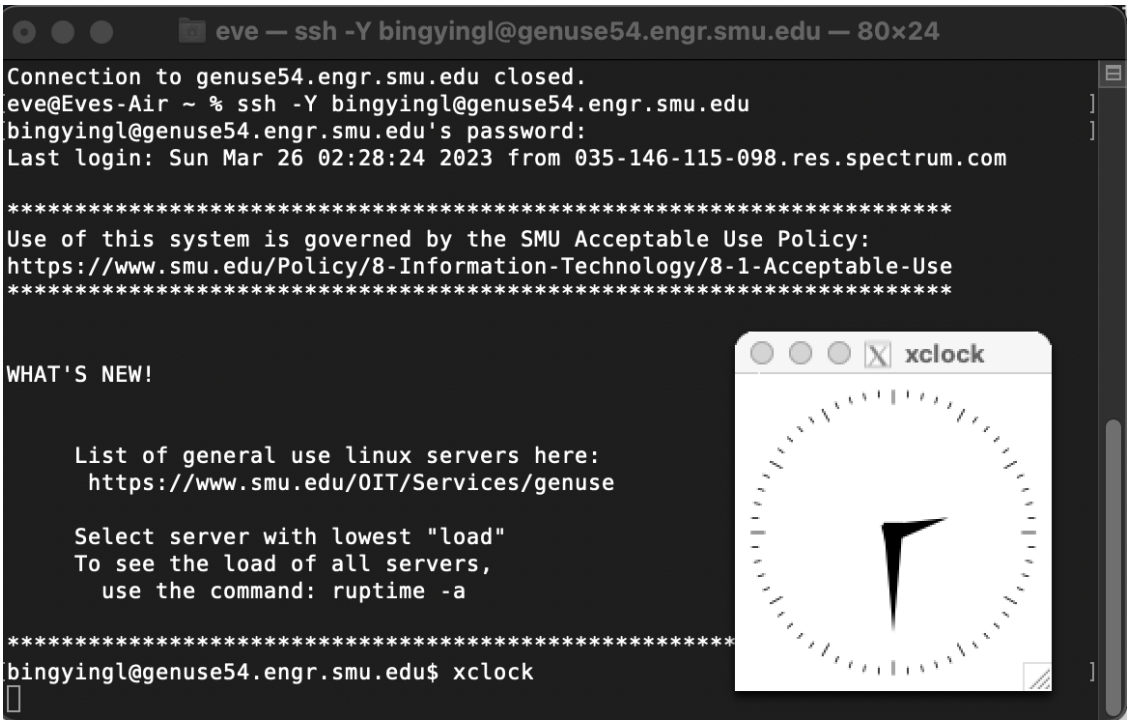
   Solution:



2. Set up an X-Windows emulator on your computer.

   Solution: I use XQuartz. And for OS, have to modify sshd_config.

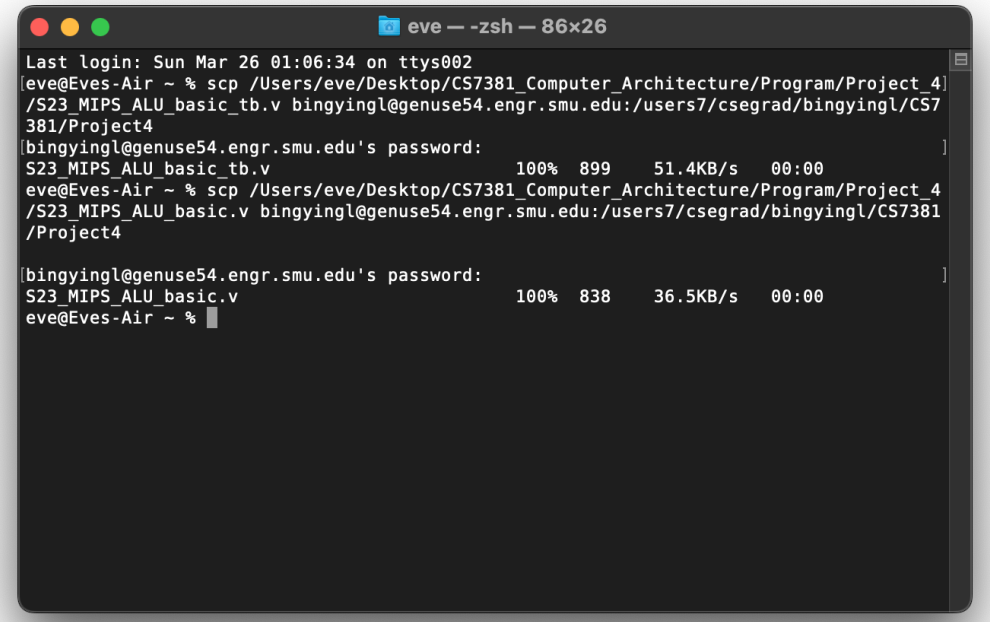


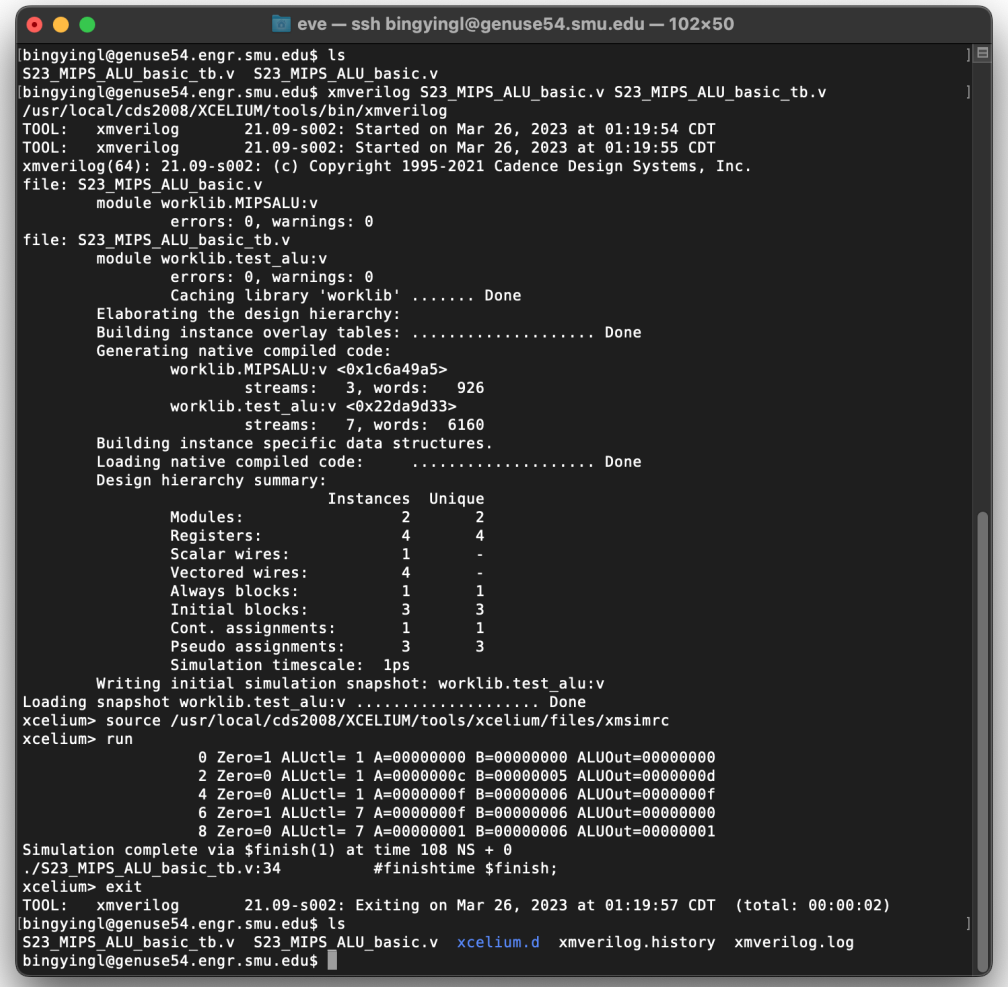


After you have set up your computer to run Xcelium, do the following to complete the project:

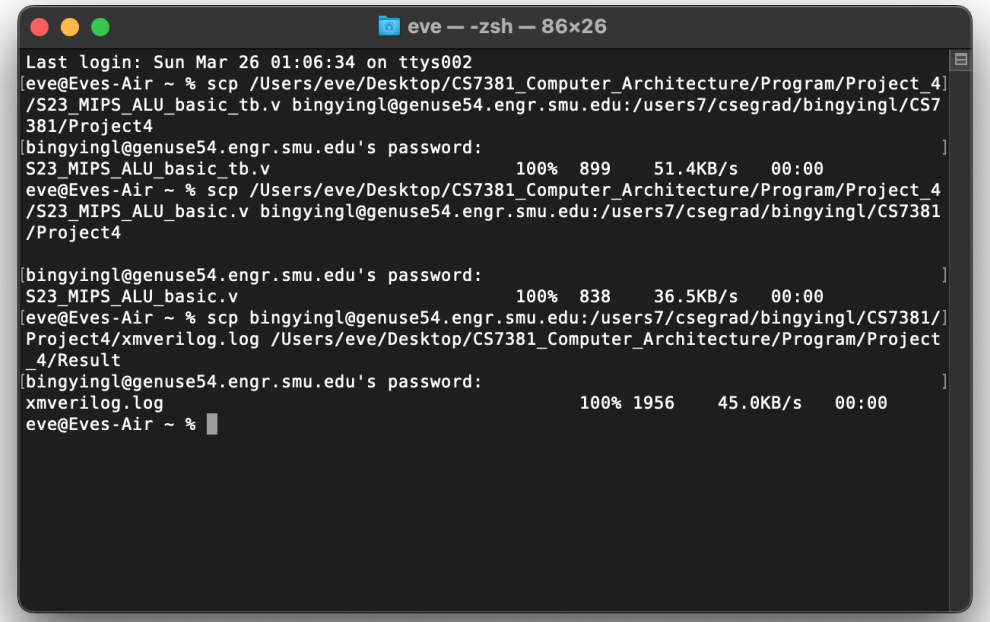
1. Please download the following Verilog files:
   - S23_MIPS_ALU_basic.v - a Verilog module for a simple MIPS arithmetic/logic unit (ALU).
   - S23_MIPS_ALU_basic_tb.v - the testbench for testing the ALU
2. This ALU performs the following 2 functions:
   - Function code 1 to implement bitwise OR (A or B)
   - Function code 7: set if $A < B$
3. Run the Verilog code using Xcelium:
   - Use the command: **xmverilog S23_MIPS_ALU_basic.v S23_MIPS_ALU_basic_tb.v**
   - Note that a copy of the testbench output will be stored in the log file by Xcelium
   - Please submit the resulting log file, edited with your name in the file.

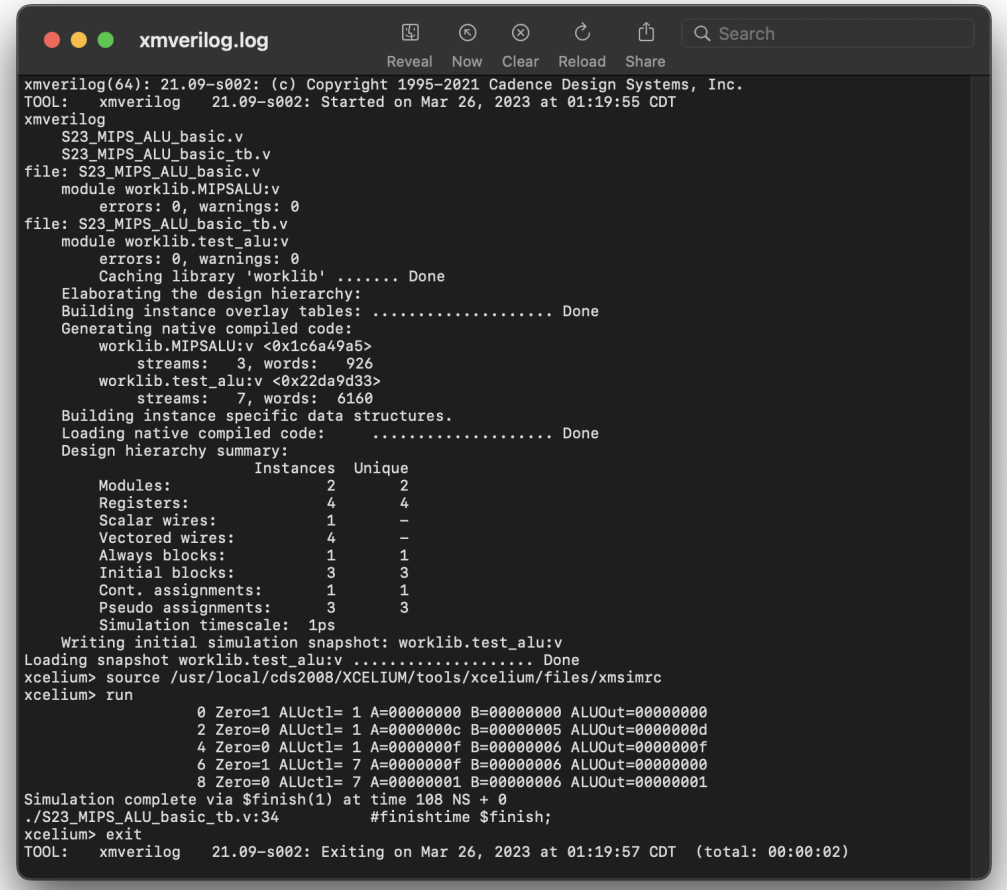
Solution: Upload File to the Server, and run the Verilog code.


eve — -zsh — 86×26
Last login: Sun Mar 26 01:06:34 on ttys002
eve@Eves-Air ~ % scp /Users/eve/Desktop/CS7381_Computer_Architecture/Program/Project_4/S23_MIPS_ALU_basic_tb.v bingyingl@genuse54.engr.smu.edu:/users7/csegrad/bingyingl/CS7381/Project4
bingyingl@genuse54.engr.smu.edu's password:
S23_MIPS_ALU_basic_tb.v 100% 899 51.4KB/s 00:00
eve@Eves-Air ~ % scp /Users/eve/Desktop/CS7381_Computer_Architecture/Program/Project_4/S23_MIPS_ALU_basic.v bingyingl@genuse54.engr.smu.edu:/users7/csegrad/bingyingl/CS7381/Project4
bingyingl@genuse54.engr.smu.edu's password:
S23_MIPS_ALU_basic.v 100% 838 36.5KB/s 00:00
eve@Eves-Air ~ %



And then download the log file from the server


eve — -zsh — 86×26
Last login: Sun Mar 26 01:06:34 on ttys002
eve@Eves-Air ~ % scp /Users/eve/Desktop/CS7381_Computer_Architecture/Program/Project_4/S23_MIPS_ALU_basic_tb.v bingyingl@genuse54.engr.smu.edu:/users7/csegrad/bingyingl/CS7381/Project4
bingyingl@genuse54.engr.smu.edu's password:
S23_MIPS_ALU_basic_tb.v 100% 899 51.4KB/s 00:00
eve@Eves-Air ~ % scp /Users/eve/Desktop/CS7381_Computer_Architecture/Program/Project_4/S23_MIPS_ALU_basic.v bingyingl@genuse54.engr.smu.edu:/users7/csegrad/bingyingl/CS7381/Project4
bingyingl@genuse54.engr.smu.edu's password:
S23_MIPS_ALU_basic.v 100% 838 36.5KB/s 00:00
eve@Eves-Air ~ % scp bingyingl@genuse54.engr.smu.edu:/users7/csegrad/bingyingl/CS7381/Project4/xmverilog.log /Users/eve/Desktop/CS7381_Computer_Architecture/Program/Project_4/Result
bingyingl@genuse54.engr.smu.edu's password:
xmverilog.log 100% 1956 45.0KB/s 00:00
eve@Eves-Air ~ %


xmverilog.log
Reveal
Now
Clear
Reload
Share
Search
xmverilog(64): 21.09-s002: (c) Copyright 1995-2021 Cadence Design Systems, Inc.
TOOL: xmverilog 21.09-s002: Started on Mar 26, 2023 at 01:19:55 CDT
xmverilog
S23_MIPS_ALU_basic.v
S23_MIPS_ALU_basic_tb.v
file: S23_MIPS_ALU_basic.v
module worklib.MIPSALU:v
errors: 0, warnings: 0
file: S23_MIPS_ALU_basic_tb.v
module worklib.test_alu:v
errors: 0, warnings: 0
Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Building instance overlay tables: ..... Done
Generating native compiled code:
worklib.MIPSALU:v <0x1c6a49a5>
streams: 3, words: 926
worklib.test_alu:v <0x22da9d33>
streams: 7, words: 6160
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 2 2
Registers: 4 4
Scalar wires: 1 -
Vectored wires: 4 -
Always blocks: 1 1
Initial blocks: 3 3
Cont. assignments: 1 1
Pseudo assignments: 3 3
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.test_alu:v
Loading snapshot worklib.test_alu:v ..... Done
xcelium> source /usr/local/cds2008/XCELIUM/tools/xcelium/files/xmsimrc
xcelium> run
0 Zero=1 ALUctl= 1 A=00000000 B=00000000 ALUOut=00000000
2 Zero=0 ALUctl= 1 A=0000000c B=00000005 ALUOut=0000000d
4 Zero=0 ALUctl= 1 A=0000000f B=00000006 ALUOut=0000000f
6 Zero=1 ALUctl= 7 A=0000000f B=00000006 ALUOut=00000000
8 Zero=0 ALUctl= 7 A=00000001 B=00000006 ALUOut=00000001
Simulation complete via $finish(1) at time 108 NS + 0
./S23_MIPS_ALU_basic_tb.v:34 #finishtime $finish;
xcelium> exit
TOOL: xmverilog 21.09-s002: Exiting on Mar 26, 2023 at 01:19:57 CDT (total: 00:00:02)