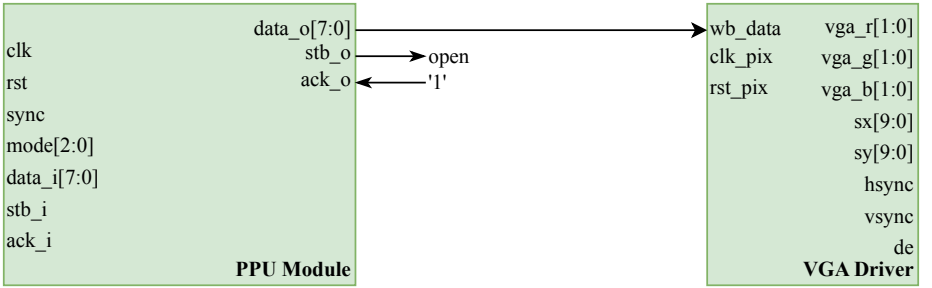

PPU Module

clk: clock sync at rising edge
rst: reset the PPU when '1'
sync: frame sync when '1'
mode: atm we have 5 pattern modes
data_i: used to for varying patterns in each mode
stb_i: '1' means data_i is ready for PPU
ack_i: '1' means PPU is ready for the next data_i

data_o: pixel, RGB info to HDMI driver
stb_o: indicate data of current pixel, currently not used
ack_o: Must always give '1'

VGA Driver

wb_data: get pixel info from PPU
clk_pix: clock sync at rising edge
rst_pix: reset the vga driver
vga_r/vga_g/vga_b: output rgb to vga module
hsync: horizontal sync to vga module
vsync: vertical sync to vga module
sx: only for simulation
xy: only for simulation
de: only for simulation

Color Scheme Explanation

Red: critical signals
Green: signals **must** to ASIC's pins
Blue: signals assuming connects to eFPGA
black: signals connects PPU and VGA module
gray: can be removed or current needed for simulation