CSARCH1 Mock Long Exam 3

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General Reminders:

1. Read ALL instructions carefully and thoroughly before answering this mock exam.
2. If applicable, denote don't-care conditions by "X" and inteterminate outputs as "indeterminate" or "indet."
3. Take note of what variables are used in the questions. Incorrect variables used will immediately be marked as 0.
4. All variables are to be written in lexographical order.

I. Concepts of Sequential Circuits [24 pts]

1) How many output lines are there in multiplexers? (write in terms of n input lines)	1
2) How many output lines are there in decoders? (write in terms of n input lines)	2^n
3) What can be used to simplify boolean expressions?	Karnaugh Maps
4) What is used to synchronize the operations of a circuit?	Clock
5) What is the type of FSM where the output is a function of the present state?	Moore Machine
6) What is the type of FSM where the output is a function of both the present state and the input?	Mealy Machine
7) What is the type of sequential circuit that operates without a global clock signal?	Asynchronous Sequential Circuits
8) What is the type of sequential circuit that operates with a global clock signal?	Synchronous Sequential Circuits
9) Level-trigger memory is also known as?	Latches
10) Edge-trigger memory is also known as?	Flip-Flops
11) Given a 18-state machine with 4 of said states being denoted as don't-cares, how many JK flip-flops are needed to represent the machine?	5
12) What is the full name of this course?	Introduction to Computer Organization and Architecture

II. Understanding Synchronous Sequential Circuits [40 pts]

1. Fill in the truth table and excitation table for the following flip-flops:

Q(t)	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indet.
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indet.

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q(t)	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Q(t)	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

III. Analysis of Sequential Circuit #1 [16 pts]

A hypothetical BS flip-flop has four operations: no change, toggle, reset to 0, and set to 1 when B and S are 00, 01, 10, and 11 respectively.

1. Fill in the characteristic table:

B	S	Q(t+1)
0	0	$Q(t)$
0	1	$\overline{Q(t)}$
1	0	0
1	1	1

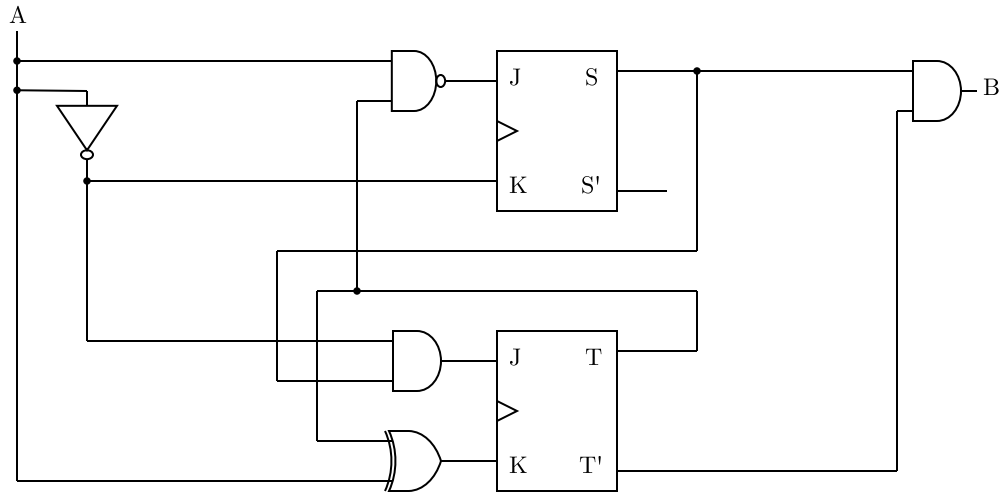
2. Fill in the truth table and excitation table:

Q(t)	B	S	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Q(t)	Q(t+1)	B	S
0	0	X	0
0	1	X	1
1	0	X	X
1	1	X	X

IV. Analysis of Sequential Circuit #2 [46 pts]

Analyze the circuit diagram and complete the state table.



Input	Present State		Flip-Flop Inputs				Output	Next State	
A	**S**	**T**	**JS**	**KS**	**JT**	**KT**	**B**	**S**	**T**
0	0	0	1	1	0	0	0	1	0
0	0	1	1	1	0	1	0	1	0
0	1	0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0	0	0
1	0	0	1	0	0	1	0	1	0
1	0	1	0	0	0	0	0	0	1
1	1	0	1	0	0	1	1	1	0
1	1	1	0	0	0	0	0	1	1

1) SOP for J input to flip-flop S	$\overline{AT}$
2) SOP for K input to flip-flop S	$\overline{A}$
3) SOP for J input to flip-flop T	$\overline{A}S$
4) SOP for K input to flip-flop T	$T \oplus A$ or $\overline{T}A + T\overline{A}$
5) SOP for output B	$S\overline{T}$
6) Type of FSM: Mealy or Moore?	Moore

V. Design of Sequential Circuit #1 [12 pts]

Design a T flip-flop using a JK flip-flop. Fill in the excitation table.

Present State	Input	Next State	Flip-Flop Inputs	
A	**T**	**A**	**JA**	**KA**
0	0	0	0	X
0	1	1	1	X
1	0	1	X	0
1	1	0	X	1

1) SOP for J input to flip-flop A	T
2) SOP for K input to flip-flop A	T

VI. Design of Sequential Circuit #2 [20 pts]

Design a sequential circuit with a single JK flip-flop A, and two inputs S and T.

If S = 0, the circuit goes to the other state.

If ST = 11, the circuit goes to state 1.

If ST = 10, the circuit remains at the same state.

Present State	Inputs		Next State	Flip-Flop Inputs	
A	**S**	**T**	**A**	**JA**	**KA**
0	0	0	1	1	X
0	0	1	1	1	X
0	1	0	0	0	X
0	1	1	1	1	X
1	0	0	0	X	1
1	0	1	0	X	1
1	1	0	1	X	0
1	1	1	1	X	0

1) SOP for J input to flip-flop A	$\overline{S} + T$
2) SOP for K input to flip-flop A	$\overline{S}$

VII. Design of Sequential Circuit #3 [63 pts]

Design a 3-bit Gray code counter using JK flip-flops that outputs 1 if there are an even number of 1s in the present state and outputs 0 otherwise.

Present State			Next State			Flip-Flop Inputs						Output
A	**B**	**C**	**A**	**B**	**C**	**JA**	**KA**	**JB**	**KB**	**JC**	**KC**	**Z**
0	0	0	0	0	1	0	X	0	X	1	X	1
0	0	1	0	1	1	0	X	1	X	X	0	0
0	1	0	1	1	0	1	X	X	0	0	X	0
0	1	1	0	1	0	0	X	X	0	X	1	1
1	0	0	0	0	0	X	1	0	X	0	X	0
1	0	1	1	0	0	X	0	0	X	X	1	1
1	1	0	1	1	1	X	0	X	0	1	X	1
1	1	1	1	0	1	X	0	X	1	X	0	0

1) SOP for J input to flip-flop A	$B\overline{C}$
2) SOP for K input to flip-flop A	$\overline{B}\overline{C}$
3) SOP for J input to flip-flop B	$\overline{A}C$
4) SOP for K input to flip-flop B	AC
5) SOP for J input to flip-flop C	$\overline{A \oplus B}$ or $\overline{A}\overline{B} + AB$
6) SOP for K input to flip-flop C	$A \oplus B$ or $A\overline{B} + \overline{A}B$
7) SOP for output Z	$\overline{A}\overline{B}\overline{C} + \overline{A}BC + A\overline{B}C + AB\overline{C}$