CSARCH1 LE2 Reviewer Series

Sequential Circuit Analysis

Version: 0.0

Sequential Circuit:

- "Memory" circuit (has capacity for storage
- Specified by a time sequence of inputs, outputs, and states. The next state is a function of the current state plus input.
  - This is opposed to combinational circuit where the output is purely based on the input.
- Feedback paths are characteristic of sequential circuits as this serves as the memory element.

Latch Vs. Flip Flop:

- Latch is based on signal/level trigger (Async)
- Flip-Flop is based on edge trigger (Sync)

Each of the flip-flops can be described by the following: Truth Table, Characteristic Table, and Excitation Table.

TYPES OF SEQUENTIAL CIRCUIT:

Synchronous:

- Behavior is defined by signals at discrete instants of time
- Synchronized through clock signals by a clock generator which produce periodic clock pulses.
  - Clock signals are Denoted as clock or clk.
- Clock pulse can be
  - Signal/Level Trigger
  - Clock Transition or Edge Trigger

Asynchronous:

- No System Clock
- Depends on the order of input signals
- Transitions are defined in units of gate delay

The **truth table** takes the previous state at $Q(t)$ and two flip-flop inputs S and R and $Q(t+1)$ as the output.
The **characterstic table** takes the flip-flop inputs and determines the properties of the next state based on these inputs only.
The **excitation table** is a table that determines the minimum inputs to change a state into a different state.

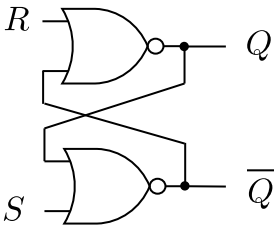
Flip-Flop Operations:

No Change: $Q(t) \rightarrow Q(t+1) = Q(t)$

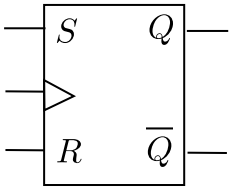
Toggle: $Q(t) \rightarrow Q(t+1) = \overline{Q(t)}$

SR Flip Flop:

Circuit Diagram

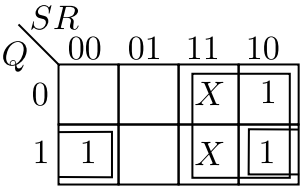


Block Diagram



Truth Table

$Q(t)$	S	R	$Q(t+1)$	Comment
0	0	0	0	No Change
0	0	1	0	Reset
0	1	0	1	Set
0	1	1	X	Indeterminate
1	0	0	1	No Change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	X	Indeterminate



$$Q(t+1) = S + Q\overline{R}$$

Note: $S = 1 \wedge R = 1$ cannot be true.

Characteristic Table

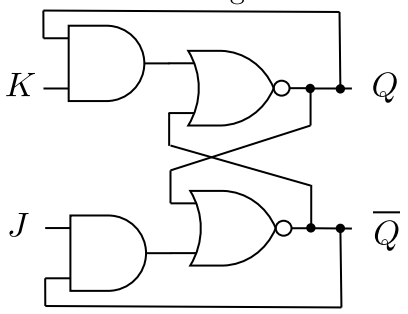
S	R	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	Indeterminate

Excitation Table

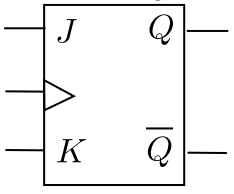
$Q(t)$	$Q(t+1)$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK Flip Flop:

Circuit Diagram



Block Diagram



Truth Table

$Q(t)$	J	K	$Q(t+1)$	Comment
0	0	0	0	No Change
0	0	1	0	Reset
0	1	0	1	Set
0	1	1	1	Toggle
1	0	0	1	No Change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	0	Toggle

Q \ JK	00	01	11	10
0			1	1
1	1			1

$$Q(t+1) = J\overline{Q} + \overline{K}Q$$

Characteristic Table

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

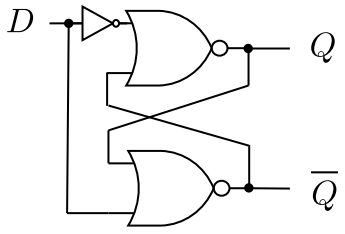
Excitation Table

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

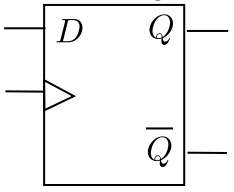
Note: The JK flip-flop is a modification of the SR flip-flop which removes the indeterminate state when both flip-flop inputs are 1. This is achieved by having an AND gate.

D Flip Flop:

Circuit Diagram

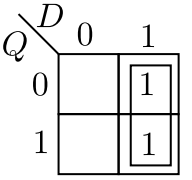


Block Diagram



Truth Table

$Q(t)$	D	$Q(t+1)$	Comment
0	0	0	Matches D
0	1	1	Matches D
1	0	0	Matches D
1	1	1	Matches D



$Q(t+1) = D$

Characteristic Table

D	$Q(t+1)$
0	0
1	1

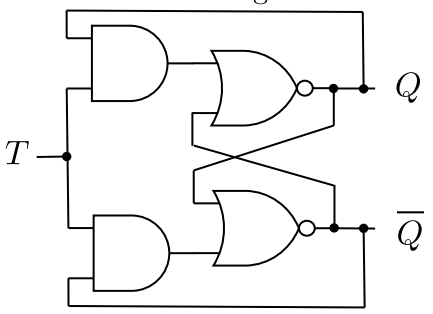
Excitation Table

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

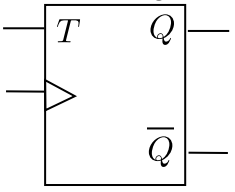
Note: The D flip-flop also known as a data flip-flop can be seen as a flip-flop that stores the current input.

T Flip Flop:

Circuit Diagram

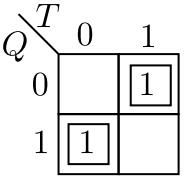


Block Diagram



Truth Table

$Q(t)$	T	$Q(t+1)$	Comment
0	0	0	No Change
0	1	1	Toggle
1	0	1	No Change
1	1	0	Toggle



$$Q(t+1) = \overline{T}Q + T\overline{Q}$$

Characteristic Table

T	$Q(t+1)$
0	$Q(t)$
1	$\overline{Q(t)}$

Excitation Table

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

Note: The T flip-flop also known as a toggle flip-flop can be seen as a flip-flop that changes state from 0 to 1 and 1 to 0 when a high signal is received. No change otherwise.