CSARCH1 LE2 Reviewer Series

Analysis of Synchronous Sequential Circuit

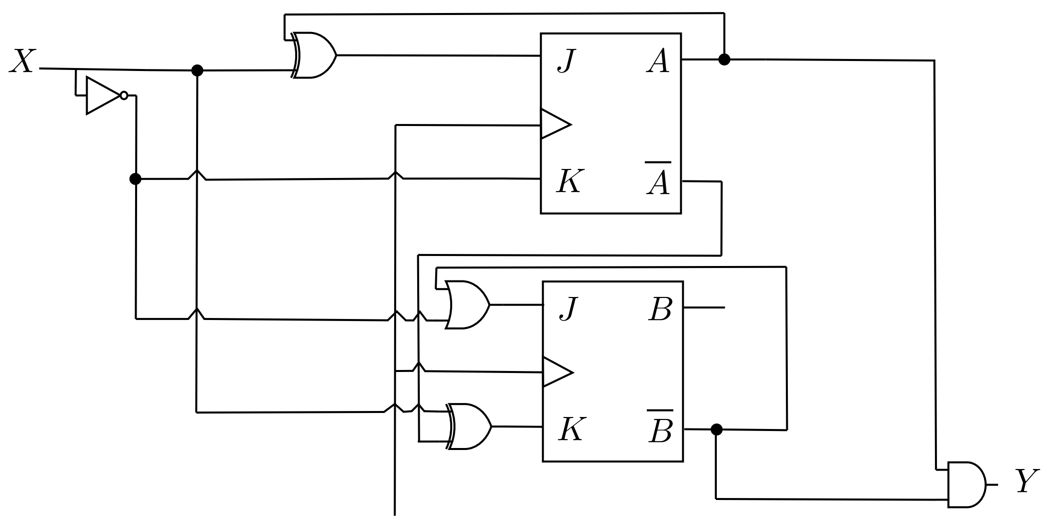
Version: 0.0

To analyze a synchronous sequential circuit we must:

1. Solve: Flip-Flop Input
2. Solve: State Transition Table
3. State Diagram
4. Classify Mealy Vs. Moore

Example 1:

Analyze the following Synchronous Sequential Circuit:



When analyzing this circuit, we must first label each part according to their function:

input/s: X

output/s: Y

We have two JK flip-flops with flip-flop input:

JA, KA, JB, KB

Tracing the diagram, we assign the following algebraic functions to each of the flip-flop inputs:

$JA = X \oplus A$

$KA = \overline{X}$

$JB = \overline{B} + \overline{X}$

$KB = X \oplus \overline{A}$

We can also assign the algebraic function to the output Y: $Y = \overline{B}A$

Based on this, we can now create a truth table with the following inputs X, A, B (Note that A, B represents state). We use the *algebraic equations* of the flip-flop inputs.

Input	Present State		Flip Flop Input				Next State		Output
X	A	B	JA	KA	JB	KB	A	B	Y
0	0	0	0	1	1	1			
0	0	1	0	1	1	1			
0	1	0	1	1	1	0			
0	1	1	1	1	1	0			
1	0	0	1	0	1	0			
1	0	1	1	0	0	0			
1	1	0	0	0	1	1			
1	1	1	0	0	0	1			

$$JA = X \oplus A$$
$$KA = \overline{X}$$
$$JB = \overline{B} + \overline{X}$$
$$KB = X \oplus \overline{A}$$

To assign the next state, we must remember the *characteristic table* of JK flip flop. After which we can fill out the output Y as well.

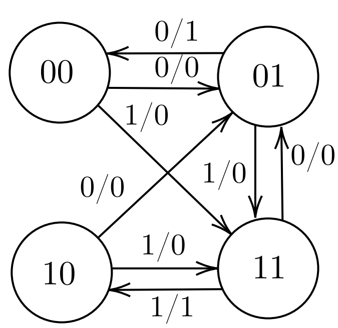
Input	Present State		Flip Flop Input				Next State		Output
X	A	B	JA	KA	JB	KB	A	B	Y
0	0	0	0	1	1	1	0	1	0
0	0	1	0	1	1	1	0	0	1
0	1	0	1	1	1	0	0	1	0
0	1	1	1	1	1	0	0	1	0
1	0	0	1	0	1	0	1	1	0
1	0	1	1	0	0	0	1	1	0
1	1	0	0	0	1	1	1	1	0
1	1	1	0	0	0	1	1	0	1

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

$$Y = \overline{B}A$$

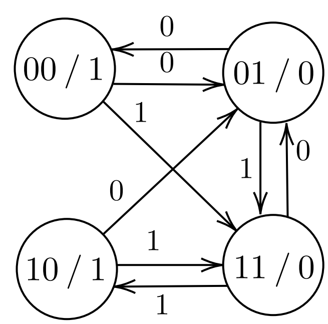
From this, we can generate a state diagram based on the input, present state, next state, and output. We have four distinct states from each combaination of A and B $(00, 01, 10, 11)$

Input	Present State		Next State		Output
X	A	B	A	B	Y
0	0	0	0	1	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	1	0	1



The diagram above is known as a Mealy Finite State Machine.

Note that each state can be viewed as having a "transition" for each input to another state.



Because the output is not dependent on the current input, we can also design this to be a Moore Finite State Machine.