CSARCH2 Mock Long Exam 2

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Important Reminders:

1. Read ALL instructions carefully and thoroughly before answering this mock exam.
2. The use of calculators and other computing devices are NOT allowed in the exam. However, you will be answering this in the comfort of your own home, so I literally have 0 control over the enforcement of that rule. ¯_(ツ)_/¯
3. Cheating in ANY form during the actual exam will be considered a major offense, merit you a 0.0 in the course, and would result in both Sir Rog and I becoming very sad.
4. This exam is GOOD FOR 4 HOURS. To be sufficiently prepared for the long exam proper, try to finish this mock exam in a shorter amount of time (while keeping a high score obv).
5. Yes, I'm sadistic and this mock exam reflects that. -Clive

I don't think Clive knows what Sadism means. -Enzo

i had fun making this :D -Sean

shout out fraser -Brent

I. Understanding Cache Memory #0

1. If the MM has 64 words and each block has 4 words, how many blocks does the MM have?
   (a) 16
   (b) 32
   (c) 128
   (d) 256
2. What MM block is MM address 32 stored if each block has 8 words
   (a) 4
   (b) 5
   (c) 6
   (d) 7
3. What MM block is MM address 37 stored if each block has 8 words
   (a) 4
   (b) 5
   (c) 6
   (d) 7

4. If CM has 4 blocks, each block has 4 words, what CM block will MM address 57 be stored?
    (a) 0
    (b) 1
    (c) 2
    (d) 3
5. What is the purpose of the Tag bit?
    (a) To uniquely identify a block within the main memory.
    (b) To determine the main memory block in the MM based on the MM blocks possibly mapped to that CM block.
    (c) To replace blocks in a set based on the chosen replacement algorithm (e.g. Least Recently Used or Most Recently Used).
    (d) To calculate which cache block the main memory block should go into.
6. In direct mapping, which part of the memory address determines the specific cache block a memory block maps to?
    (a) Tag bits
    (b) Word bits
    (c) Block bits
    (d) Address bits
7. In a fully associative cache, how is a memory block placed into the cache?
    (a) Only in one specific location
    (b) Any block in any cache line
    (c) Based on hash function
    (d) Based on index bits in address
8. In a 4-way Block Set Associative Cache, each set can contain:
    (a) 1 block
    (b) 4 sets
    (c) 4 blocks
    (d) 4 bytes
9. A high cache hit rate usually implies:
    (a) More cache misses
    (b) Better CPU performance
    (c) Slower access time
    (d) Increased memory swapping

10. In a cache hit write-through:
    (a) Writes are done only to cache
    (b) Writes are done to memory only when the block is evicted
    (c) Data is written to both cache and main memory
    (d) Cache is bypassed
11. **Statement A:** In direct-mapped cache, each memory block maps to exactly one cache block.

    Statement B: In fully-associative cache, a memory block can be stored in any cache line.
    (a) Only A is true
    (b) Only B is true
    (c) Both A and B are true
    (d) Neither A nor B are true
12. Typically, what is the ratio between the MM size and the CM size?
    (a) 100:1
    (b) 100:10
    (c) 100:5
    (d) 100:20
13. To solve for CM size in bits, which of the following do we consider? (Select all that applies)
    (a) Valid bits
    (b) Set bits
    (c) Word bits
    (d) Address bits
    (e) Tag bits
    (f) Block bits
    (g) Data bits

II. Understanding Cache Memory #1

A Direct Mapping Non-Load Through Policy Cache has 8 blocks with a block size of 8 words. CAT is 1ns, and MAT is 10ns.

- Given the main memory BLOCK sequence (in decimal):

    16, 15, 22, 11, 22, 16, 23, 26, 12, 24, 15, 26.

- Show the final content of the cache memory after fetching all the sequences. Use the table below; write the letter E to denote empty.

Cache Block	MM block mapped here.
0	
1	
2	
3	
4	
5	
6	
7	

a.) How many blocks in the sequence are a cache hit?	
b.) How many blocks in the sequence are a cache miss?	
c.) What is the miss penalty of the cache (in ns)?	
d.) What is the average access time of the MM block sequences (in ns)?	
e.) What is the total access time of the MM block sequences (in ns)?	

III. Understanding Cache Memory #2

A Direct Mapping Load Through Policy Cache has 4 blocks with a block size of 4 words. CAT is 1ns, and MAT is 10ns.

- Given the main memory ADDRESS sequence (in decimal):

    16, 15, 0, 4, 14, 22, 19, 17, 15, 29, 26, 19

- Show the final content of the cache memory after fetching all the sequences. Use the table below; write the letter E to denote empty.

Cache Block	MM block mapped here.
0	
1	
2	
3	

a.) How many addresses in the sequence are a cache hit?	
b.) How many addresses in the sequence are a cache miss?	
c.) What is the miss penalty of the cache (in ns)?	
d.) What is the average access time of the MM addresses sequences?	
e.) What is the total access time of the MM addresses sequences?	

IV. Understanding Cache Memory #3

A 2-way Block Set Associative Non-Load Through Policy Cache with 2048 words has a block size of 16 words. There are 2048 MM blocks. Each word has 8 bits.

a.) MM Address Bits	
b.) How many CM blocks	
c.) Tag Block Word	
d.) MM size in bits	
e.) CM size in bits (Including Tag and Valid Bit)	
f.) What CM block will Memory Address 1987 be stored in?	
g.) What CM block will Memory Block 1987 be stored in?	
h.) Assume a 4 Way Set, CM size in bits	
i.) Assume Direct Mapping, CM size in bits	
j.) Assume Fully Associative, CM size in bits	

V. Understanding Cache Memory #4

A 33554432 Bit Direct Mapping Non-Load Through Policy Cache has a block size of 512 words. There are 262144 MM blocks. Each word has 32 bits. CPU fetches memory blocks (0-4000) 5 times. MAT is 10 ns.

a.) MM Address Bits	
b.) How many CM blocks	
c.) Tag Block Word	
d.) MM size in bits	
e.) CM size in bits (Including Tag and Valid Bit)	
f.) What CM block will Memory Address 111387 be stored in?	
g.) What CM block will Memory Block 111387 be stored in?	
h.) Total Access Time	
i.) Assume a 4 Way Set, CM size in bits	
j.) Assume a 8 Way Set, CM size in bits	
k.) Assume a 16 Way Set, CM size in bits	

VI. Understanding Cache Memory #5

We have a 8 Block Fully Associative LRU Load Through Policy Cache with each block having 16 words. Assume cache initially has no value, CPU fetches the ff MM blocks in this loop. MAT is 10ns, CAT is 1ns.

```
for 0 to 9
        CPU fetch Memory Address 0-31
        for 0 to 19
                CPU fetch Memory Address 32-127
        end
        CPU fetch Memory Address 128-159
end
```

a.) Hit and Miss in 1st pass	
b.) Hit and Miss in 2nd pass	
c.) Total Hit and Miss	
d.) Total Access Time 1st Pass	
e.) Average Access Time 1st Pass	
f.) Total Access Time 2nd Pass	
g.) Average Access Time 2nd Pass	
h.) Total Access Time	
i.) Average Access Time	
j.) CM Final Snapshot	

VII. Understanding Cache Memory #6 [BONUS]

Given these specifications:

- MAT is 20 ns
- CAT is 2 ns
- 8 Cache Blocks
- Cache Set Size is 4 blocks
- Block Set Associative
- MRU
- No Load Through Policy
- Main Memory has 262144 words
- Each word has 16 bits
- Each block has 16 words

Assume cache initially has no values.

CPU fetches the ff. MM blocks in this loop.

```
1       for 0 to 4
2               CPU fetch Memory Address 0-31
3               for 0 to 19
4                       CPU fetch Memory Address 32-127
5               end
12              CPU fetch Memory Address 304-319
13      end
```

a.) Hit and Miss in 1st pass	
b.) Hit and Miss in 3nd pass	
c.) Total Hit and Miss	

d.) Total Access Time 1st Pass	
e.) Average Access Time 1st Pass	
f.) Total Access Time 3nd Pass	
g.) Average Access Time 3nd Pass	
h.) Total Access Time	
i.) Average Access Time	
j.) CM Snapshot after Loop 3	
k.) CM Snapshot after Loop 5	
l.) CM Final Snapshot	
m.) Total Hit and Miss if we did not change to LRU	
n.) MM Address Bits	
o.) MM size in Bits	
p.) CM size in Bits	
q.) Assume Direct Mapping, CM size in Bits	

VIII. Understanding Cache Memory #7 [IGNORE - Naglabas lang ng pagkasadista]

Given these specifications:

- MAT is 20 ns
- CAT is 2 ns
- 16 Cache Blocks
- 2 Cache Sets
- Block Set Associative
- No Load Through Policy
- Main Memory has 262144 words
- Each word has 16 bits
- Each block has 16 words
- Each set has 8 blocks

Assume cache initially has initial values given below.

Set	Block	Data	Age
0	0	8	0
	1	4	1
	2	2	2
	3	1	3
	4		
	5		
	6		
	7		
1	0	3	0
	1	5	1
	2	7	2
	3	9	3
	4		
	5		
	6		
	7		

CPU fetches the ff. MM blocks in this loop.

```
1     for i in 0 to 9
2           CPU fetch Memory Address 0 to 31
3           for j in 0 to 19
4                 CPU fetch Memory Address 32 to 255
5           end
6           for j in 0 to i
7                 for k in 0 to 2
8                       CPU fetch Memory Address 256 to 303
9                 end
10                CPU fetch Memory Address 16 to 127
11          end
12          CPU fetch Memory Address 304 to 319
13    end
```

a.) What is the Total Access Time and Average Access Time when using MRU?	
b.) What is the Total Access Time and Average Access Time when using LRU?	

c.) Which replacement algorithm had the lowest Average Access Time? Why? Explain in less than 100 words.	
d.) What would be the effect of swapping the algorithm from MRU to LRU at the 3rd pass then LRU to MRU at the 6th pass to the Average Access Time? Why? Explain in less than 100 words.	
e.) Theoretically at line 2, if we changed the code to CPU fetch Memory Address 0 to [(i * 2 + 10) * 16 - 1], what would be the new Average Access Time?	