```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04/13/2022 06:18:11 PM
// Design Name:
// Module Name: Fulladder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Fulladder(
    input Aa,
    input Bb,
    input Cin,
    output sum,
    output carry
    );
    wire inverseC;
    assign inverseC = ~Cin;
    m4_1 m1 ( .in({Cin,inverseC, inverseC, Cin}), .sel({Aa, Bb}), .o(sum) );
    m4_1 m2 ( .in({1'b1, Cin, Cin, 1'b0}), .sel({Aa, Bb}), .o(carry));
endmodule
```