```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 05/11/2022 03:20:09 PM
// Design Name:
// Module Name: countU8L
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module countU8L(
    input clk,
    input Up,
    input Dw,
    input LW,
    input [7:0] d,

    output [7:0] q,
    output UTC,
    output timeup
    );
    wire [1:0] utc;


    // 111100 = 60 decmial
   // assign timeup = 6'b00111100;
    countUD4L cnt0to3(.clk(clk), .Up(Up), .Dw(Dw), .LW(LW), .d(d[3:0]), .q(q[3:0]),
.UTC(utc[0]));
    countUD4L cnt4to7(.clk(clk), .Up(Up & utc[0]), .Dw(Dw), .LW(LW), .d(d[7:4]),
.q(q[7:4]), .UTC(utc[1]));
    //0011
    assign timeup = q & 8'b00111100;
    //when all true it returns left most dot is going to be on
    assign UTC = utc[0] & utc[1] ;
```

```
    //dtc is gotten from the count4dl which is why non of these are inverted
    //the inversion for dtc is already made in count4dl

endmodule
```