```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 05/11/2022 03:31:13 PM
// Design Name:
// Module Name: stateMachine
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module SM(
    input clk,
    input left,
    input right,
    input timesUp,


    output startleft,
    output startright,
    output exitleft,
    output exitright,
    output load,
    output run,
    output idle,
    output reset,
    output [3:0]R
    );

    wire [6:0] q;
    wire [6:0] d;
    wire [3:0]s;

    //HOT LOGIC
    //the conditions of my staemachine
```

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    assign d[0] = (|q[5:0]) & (~left & ~right);
    assign d[1] = ~timesUp & ( (q[0]) & (left & ~right | (~left & right) ));
    assign d[2] = ~timesUp & ( (|q[4:1]) & (left &  right));
    assign d[3] = ~timesUp & ( (q[3] | q[2] | q[0]) & (left & ~right) );
    assign d[4] = ~timesUp & ( (q[4] | q[2] | q[0]) & (~left & right) );
    assign d[5] =  timesUp & ( |q[5:1] );

    //connection outputs
    assign load= ~q[0];
    assign run= ~q[0] & ~q[5];
    assign idle= q[0];
    assign reset= (|q[5:3]) & ~left & ~right;

    //STATE MACHINE FLIP FLOPS
    //Flip flops for the stateMachine, 6 states total
    //attemt at 9 state but there was too much complication
    FDRE #(.INIT(1'b1)) FF0 (.C(clk), .CE(1'b1), .D(d[0]), .Q(q[0]));
    FDRE #(.INIT(1'b0)) FF1 (.C(clk), .CE(1'b1), .D(d[1]), .Q(q[1]));
    FDRE #(.INIT(1'b0)) FF2 (.C(clk), .CE(1'b1), .D(d[2]), .Q(q[2]));
    FDRE #(.INIT(1'b0)) FF3 (.C(clk), .CE(1'b1), .D(d[3]), .Q(q[3]));
    FDRE #(.INIT(1'b0)) FF4 (.C(clk), .CE(1'b1), .D(d[4]), .Q(q[4]));
    FDRE #(.INIT(1'b0)) FF5 (.C(clk), .CE(1'b1), .D(d[5]), .Q(q[5]));
    //FDRE #(.INIT(1'b0)) FF6 (.C(clk), .CE(1'b1), .D(D[6), .Q(q[6]));
    //FDRE #(.INIT(1'b0)) FF7 (.C(clk), .CE(1'b1), .D(D[7]), .Q(q[7]));
    //FDRE #(.INIT(1'b0)) FF8 (.C(clk), .CE(1'b1), .D(D[8]), .Q(q[8]));


    //voodoo magic of the dark world (somehow makes my counter work better)
    FDRE #(.INIT(1'b0)) Lleft (.C(clk), .CE(q[0]), .D(s[0]), .Q(R[0]));
    assign s[0]= q[0] & left & ~right;
    FDRE #(.INIT(1'b0)) Lright (.C(clk), .CE(q[0]), .D(s[1]), .Q(R[1]));
    assign s[1]= q[0] & ~left & right;
    FDRE #(.INIT(1'b0)) turkleft (.C(clk), .CE(q[3] | q[0]), .D(s[2]), .Q(R[2]));
    assign s[2]=  q[3] & ~timesUp & ~left & ~right;
    FDRE #(.INIT(1'b0)) turkright (.C(clk), .CE(q[4] | q[0]), .D(s[3]), .Q(R[3]));
    assign s[3]= q[4] & ~timesUp & ~left & ~right;

endmodule
```