Hongzheng Chen

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Education

2017.8–2021.6 **Sun Yat-sen University**, Guangzhou, China.
B.Sc. in Computer Science, School of Data and Computer Science
Overall GPA: 92.0/100 (3.95/4.00) Ranking: 1/188

Publications

1. **Hongzheng Chen**, Minghua Shen, *A Deep-Reinforcement-Learning-Based Scheduler for FPGA HLS*, in Proceedings of the 38th International Conference on Computer-Aided Design (ICCAD), 2019.
2. Minghua Shen, **Hongzheng Chen***, Nong Xiao, *Entropy-Directed Scheduling for FPGA High-Level Synthesis*, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020.
3. Yichi Zhang, Junhao Pan, Xinheng Liu, **Hongzheng Chen**, Deming Chen, Zhiru Zhang, *FracBNN: Accurate and FPGA-Efficient Binary Neural Networks with Fractional Activations*, in Proceedings of the 29th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), 2021.

* **Corresponding Author**

Research Experience

2020.5–Present **Auto-Streaming Support for Heterogeneous Programming Platform**.
Supervisor: Prof. Zhiru Zhang, Cornell University
Project Link: `https://github.com/cornell-zhang/heterocl`

- Designed a binary neural network library for HeteroCL, and implemented the quantized ReAct-ResNet that outperforms previous BNN models with large accuracy improvement and significant speedup.
- Provided dataflow architecture generation support for HeteroCL, and proposed a fully pipelined BNN accelerator that achieved 1,992 FPS on Xilinx Alveo U280 FPGA.
- Implemented an auto-profiling IR pass for HeteroCL, enabling to generate the roofline model automatically and guide users to make better optimizations.

2018.8–2020.4 **Large-Scale Graph Processing Systems for Concurrent Graph Jobs**.
Supervisor: Dr. Minghua Shen and Prof. Nong Xiao, National Supercomputer Center in Guangzhou, Prof. Xuehai Qian, University of Southern California

- Designed a graph processing system *Krill* that consists of a compiler and a runtime, enabling to execute multiple graph applications on a shared graph concurrently.
- Proposed property buffer and its compiler to enable data layout transformation, and graph kernel fusion for runtime system to maximumly reduce the number of memory accesses.
- Shown up to 7x speedup, 5x memory access reduction, and 4x latency reduction compared with the state-of-the-art graph processing system.
- This work has been summited to anonymous peer-review and is open-sourced on Github `https://github.com/chhzh123/krill`.

2018.3–2019.1 **High-Level Synthesis for Field-Programmable Gate Array (FPGA)**.
Supervisor: Dr. Minghua Shen and Prof. Nong Xiao, National Supercomputer Center in Guangzhou

2018.3–2018.7 **Project 1: Entropy-Directed Scheduler for FPGA HLS**.

- Proposed a heuristic scheduler based on information entropy for FPGA HLS.
- Established a connection between the maximum entropy principle and resource/time-constrained scheduling problems theoretically.
- Integrated the scheduler into the open-source HLS system *Legup* and obtained up to 20% performance improvement.
- This work has been published in Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD).

2018.7–2019.1 **Project 2: Deep-Reinforcement-Learning-Based Scheduler for FPGA HLS**.

- Designed a novel state and action representation for leveraging deep reinforcement learning in HLS scheduling.
- Proposed a training pipeline that consists of supervised learning and reinforcement learning enabling better scheduling performance.
- This work has been accepted by International Conference on Computer-Aided Design (ICCAD'19).

Internship

2020.8–Present **Large-Scale Graph Neural Network Training Platform**.
Supervisor: Jun He and Yibo Zhu, Bytedance AI Lab

Awards & Honors

2020.10 **CCF Elite Collegiate Award** (98 undergrads in China), China Computer Federation (CCF).
2018-2020 **National Scholarship** $\times$ **2** (Top 1%), Ministry of Education of PRC.
2017-2020 **First-Prize Scholarship** $\times$ **3** (Top 5%), Sun Yat-sen University.
2017-2018 **Samsung Scholarship**, Samsung Electronics.
2019.7 **Second Place**, *IEEE EDAthon*, IEEE Council on Electronic Design Automation (CEDA).
2019.1 **Meritorious Winner**, *Mathematical Contest in Modeling (MCM)*, COMAP.

Selected Projects

2019 Fall **Chatbot-Based Agenda Management System**.
Project link: `https://github.com/chhzh123/AIDO`

- Designed a chat bot based on natural language processing, which can grab user's schedule information and add it to database when chatting.
- Provided functions like daily chatting, agenda management, and voice input.
- Ranked the 1st in *Database System* course among 190 students.

2019 Spring **Advanced Operating System in Protected Mode**.
Project link: `https://github.com/chhzh123/AdvancedOS`

- Implemented an operating system running in 32-bit protected mode from a bare machine, which enables to load and run user programs concurrently in a time-sharing setting.
- Provided a simple shell with multiple consoles, a FAT file system with C file operations support, and a basic *pthread* library that can be directly called from user programs.
- Attained the only full score (100/100) in *Operating Systems* course among 190 students.

2018 Fall **Multi-Cycle CPU in MIPS Architecture**.

- Designed a multi-cycle CPU, implemented in Verilog, and fully emulated on FPGA.
- Proposed a simple assembler written in Python, enabling MIPS operations to be transformed into binary instructions automatically.
- Ranked the 1st in *Computer Organization* course among 190 students.

Skills

Programming C, C++, Python, Haskell, Prolog, x86 assembly, Verilog
Toolkits OpenMP, CUDA, MPI, Pytorch, Wolfram Mathematica, Matlab, Vivado HLS, LaTeX
Languages English (fluent), Chinese (native)