Hongzheng Chen

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Education

2017.9–2021.7 **Sun Yat-sen University**, Guangzhou, China.
B.Sc. in Computer Science, School of Data and Computer Science
Overall GPA: 91.5/100 Ranking: 5/240

Publications

1. **Hongzheng Chen**, Minghua Shen, *A Deep-Reinforcement-Learning-Based Scheduler for FPGA HLS*, in Proceedings of the 38th International Conference on Computer-Aided Design, 2019.
2. Minghua Shen, **Hongzheng Chen (Corresponding author)**, Nong Xiao, *Entropy-Directed Scheduling for FPGA High-Level Synthesis*, in Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019.

Research Experience

2018.8–Present **Large-Scale Graph Processing Systems and Accelerators**.
Supervisor: Dr. Minghua Shen and Prof. Nong Xiao, National Supercomputer Center in Guangzhou

2018.8–2019.8 **Project 1: High-Performance Concurrent Graph Processing System**.

- Designed a graph processing system *Krill* enabling to execute multiple graph applications concurrently.
- Proposed graph kernel fusion and fast frontier filters to maximumly reduce the number of memory accesses.
- Shown up to 8x speedup and 14x memory access reduction compared with the state-of-the-art single graph processing system.
- This work has been summited to anonymous peer-review and is open-sourced on Github `https://github.com/chhzh123/krill`.

2019.8–Present **Project 2: FPGA-Based Accelerator for Graph Computing**.

- Designed an accelerator for graph computing equipped with prefetching and pipelining techniques to maximumly hide the access delay.
- Decoupled graph structure and graph properties enabling different event-triggered prefetch strategies.
- Implementing in *Chisel* and to be emulated on FPGA.

2018.3–2019.1 **High-Level Synthesis for Field-Programmable Gate Array (FPGA)**.
Supervisor: Dr. Minghua Shen and Prof. Nong Xiao, National Supercomputer Center in Guangzhou

2018.3–2018.7 **Project 1: Entropy-Directed Scheduler for FPGA HLS**.

- Proposed a heuristic scheduler based on information entropy for FPGA HLS.
- Established a connection between the maximum entropy principle and resource/time-constrained scheduling problems theoretically.
- Integrated the scheduler into the open-source HLS system *Legup* and obtained up to 20% performance improvement.
- This work has been published in Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD).

2018.7–2019.1 **Project 2: Deep-Reinforcement-Learning-Based Scheduler for FPGA HLS**.

- Designed a novel state and action representation for leveraging deep reinforcement learning in HLS scheduling.
- Proposed a training pipeline that consists of supervised learning and reinforcement learning enabling better scheduling performance.
- This work has been accepted by International Conference on Computer-Aided Design (ICCAD'19).

Awards & Honors

2018-2019 **National Scholarship**, Ministry of Education of PRC (Top 2% of 240).

2017-2019 **First-Prize Scholarship** × **2**, Sun Yat-sen University (Top 5% of 240).

2017-2018 **Samsung Scholarship**, Samsung Electronics (Top 1% of 240).

2019.7 **Second Place**, *IEEE EDAthon*, IEEE Council on Electronic Design Automation (CEDA).

2019.1 **Meritorious Winner**, *Mathematical Contest in Modeling (MCM)*, COMAP.

Selected Projects

2019 Spring **Advanced Operating System in Protected Mode**.

Project link: `https://github.com/chhzh123/AdvancedOS`

- Implemented an operating system running in 32-bit protected mode from a bare machine, which enables to load and run user programs concurrently in a time-sharing setting.
- Provided a simple shell with multiple consoles, a FAT file system with C file operations support, and a basic *pthread* library that can be directly called from user programs.
- Attained the only full score (100/100) in *Operating Systems* course among 190 students.

2019 Spring **BitTorrent Protocol for Peer-to-Peer Networks**.

- Implemented the BitTorrent Protocol in sever and client programs using C++ sockets.
- Enabled the severs and clients to create and parse BitTorrent seeds, as well as download and upload files concurrently.
- Awarded as one of the best projects in *Computer Networking* course.

2018 Fall **Multi-Cycle CPU in MIPS Architecture**.

- Designed a multi-cycle CPU, implemented in Verilog, and fully emulated on FPGA.
- Proposed a simple assembler written in Python, enabling MIPS operations to be transformed into binary instructions automatically.
- Ranked the 1st in *Computer Organization* course among 190 students.

Selected Courses

- Operating Systems 100/100
- Parallel Computing 95/100
- Computer Organization Principle 98/100
- Computer Networking 95/100
- Distributed Systems 96/100
- Artificial Intelligence 97/100

Skills

Programming C, C++, Python, Haskell, Prolog, x86 assembly, Verilog

Toolkits Pytorch, Wolfram Mathematica, Matlab, LaTeX

Languages English (fluent), Chinese (native)