

CSE460

Lab Assignment 0

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Section: 06

PROBLEM 1

a.

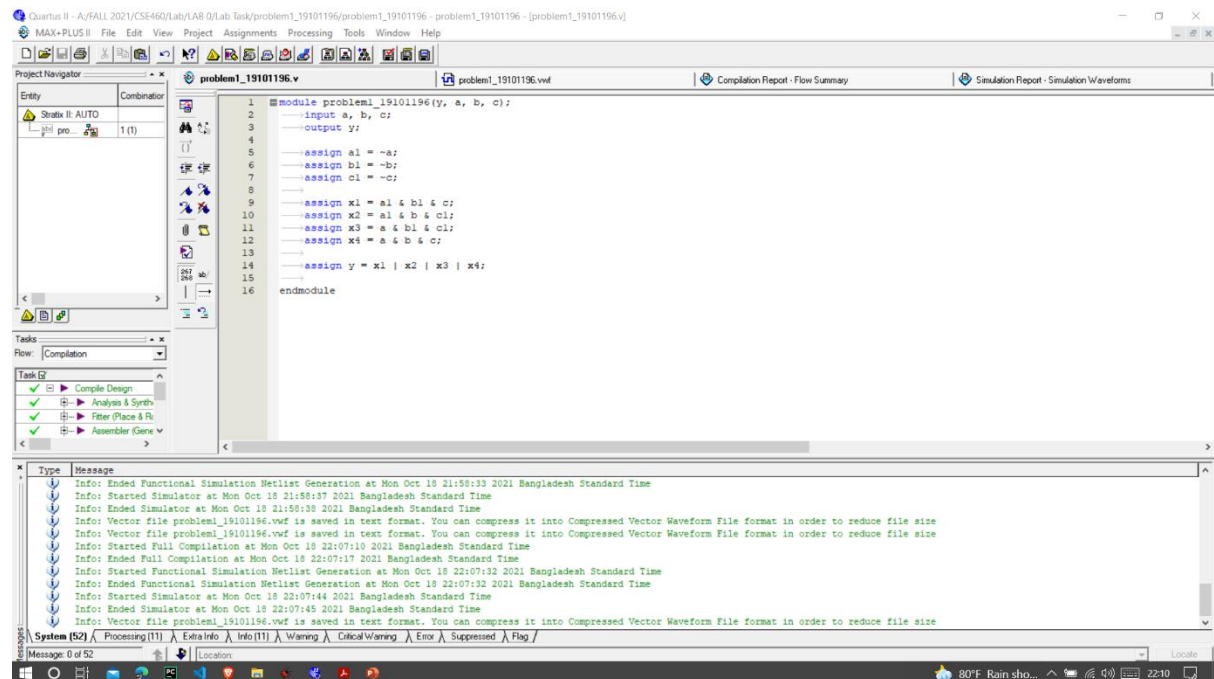
Truth Table:

A	B	C	$\sim A \sim B C$	$\sim A B \sim C$	$A \sim B \sim C$	$A B C$	$Y = \sim A \sim B C + \sim A B \sim C + A \sim B \sim C + A B C$
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1
0	1	0	0	1	0	0	1
0	1	1	0	0	0	0	0
1	0	0	0	0	1	0	1
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	1	1

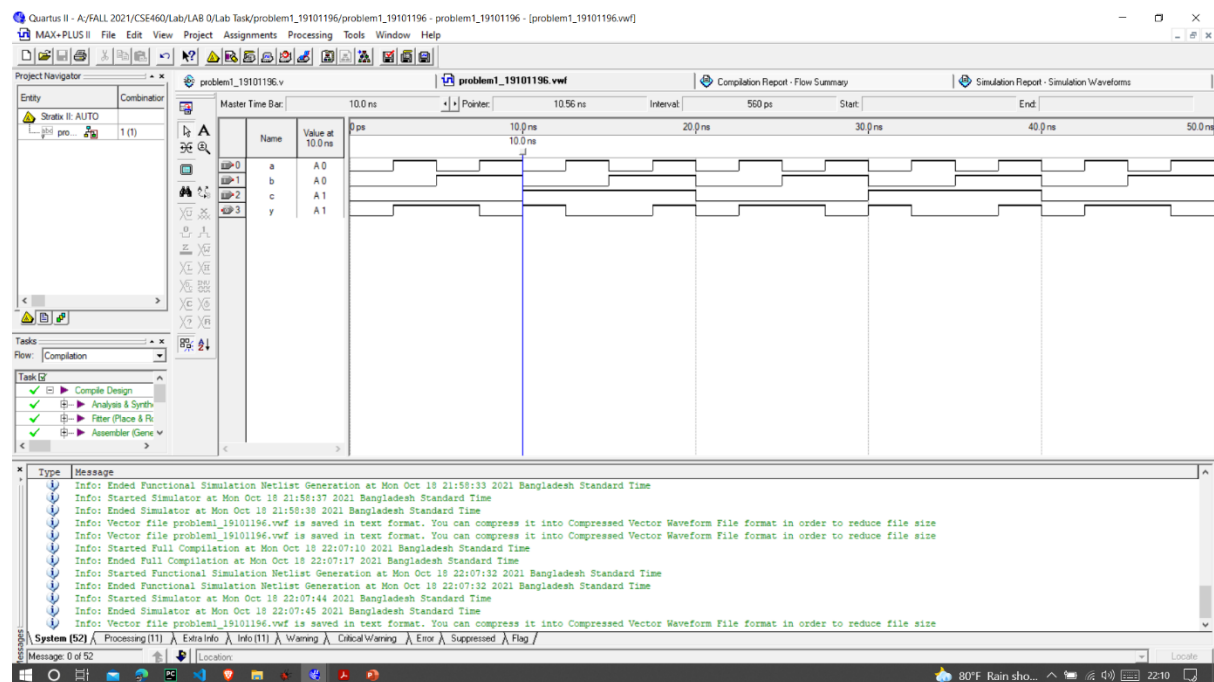
From the above truth table, we can say when A is low or 0 the output is XOR of B and C, when A is high or 1 the output is XNOR of B and C. In general, when one of the inputs is 0, $Y = \text{XOR of other 2 inputs}$, similarly when that same input is 1, $Y = \text{XNOR of the other two inputs}$.

b.

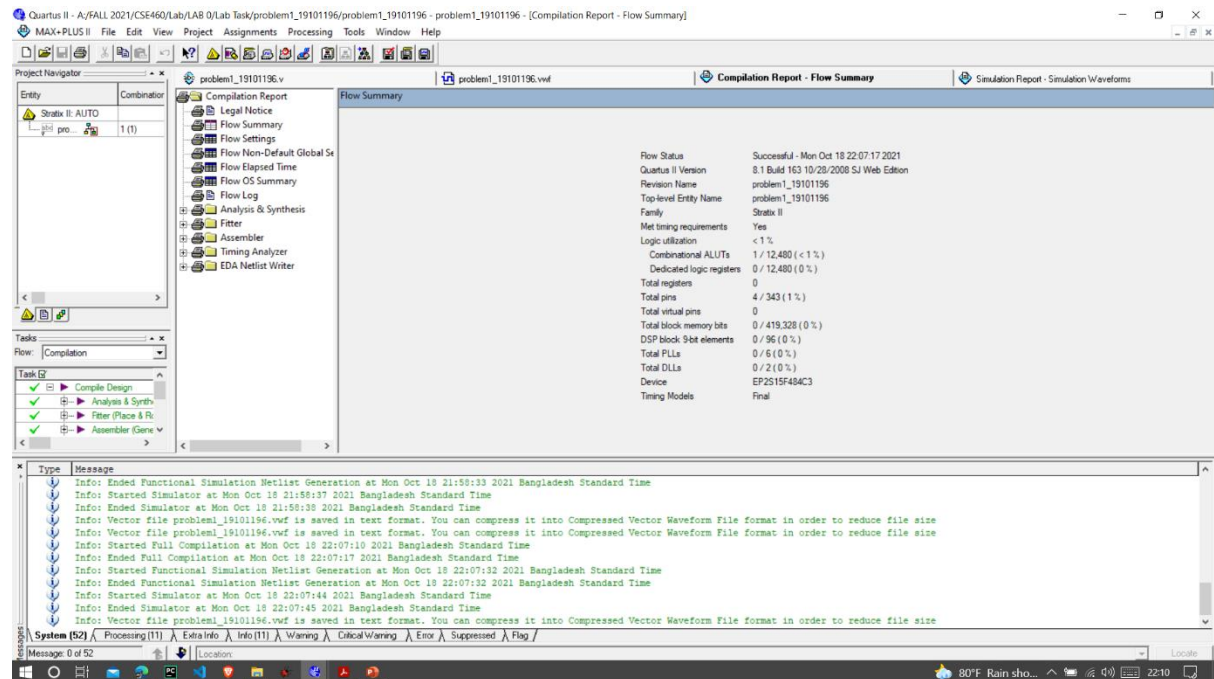
Code:



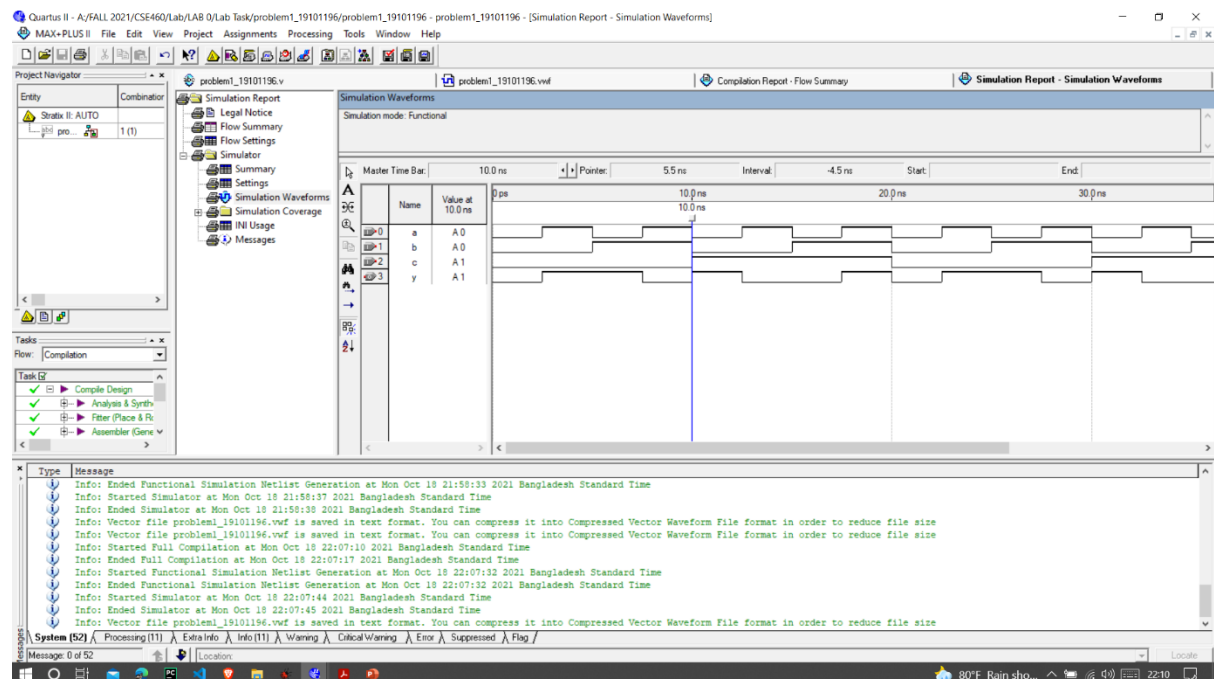
Waveform:



Compilation Report:



Simulation Report:



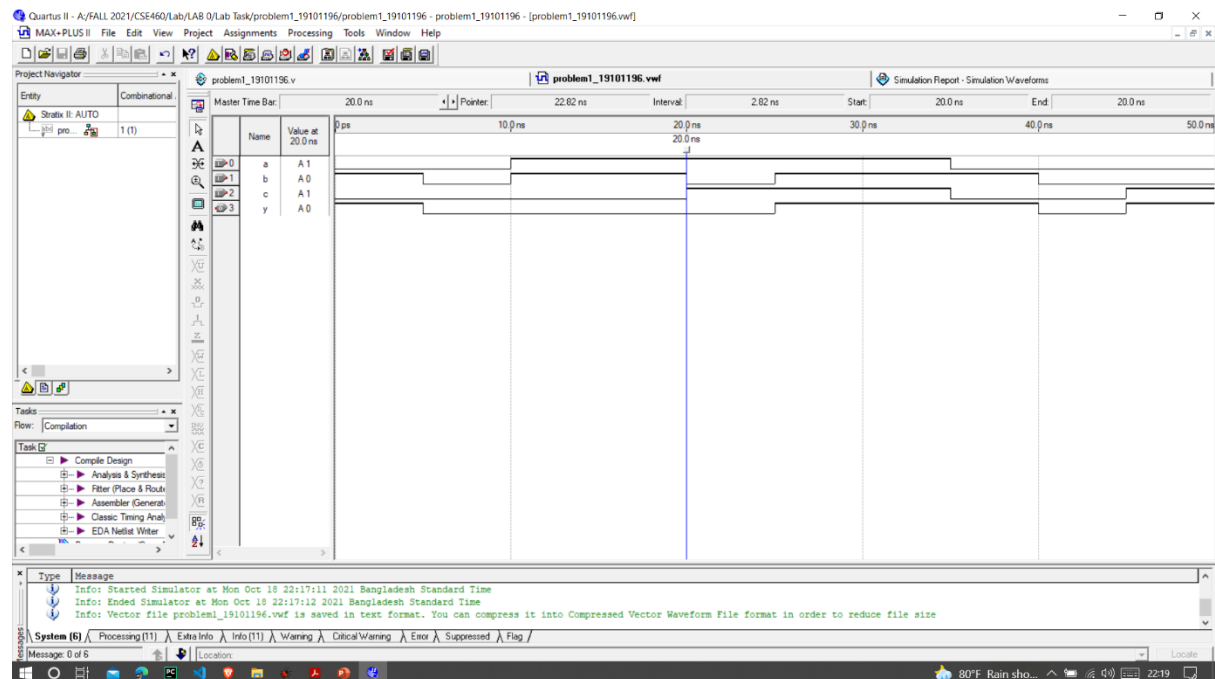
From the above waveform, at time = 4ns, when A = 1, B = 0, C = 0 we get Y = 1

From the above waveform, at time = 8ns, when A = 1, B = 1, C = 0 we get Y = 0

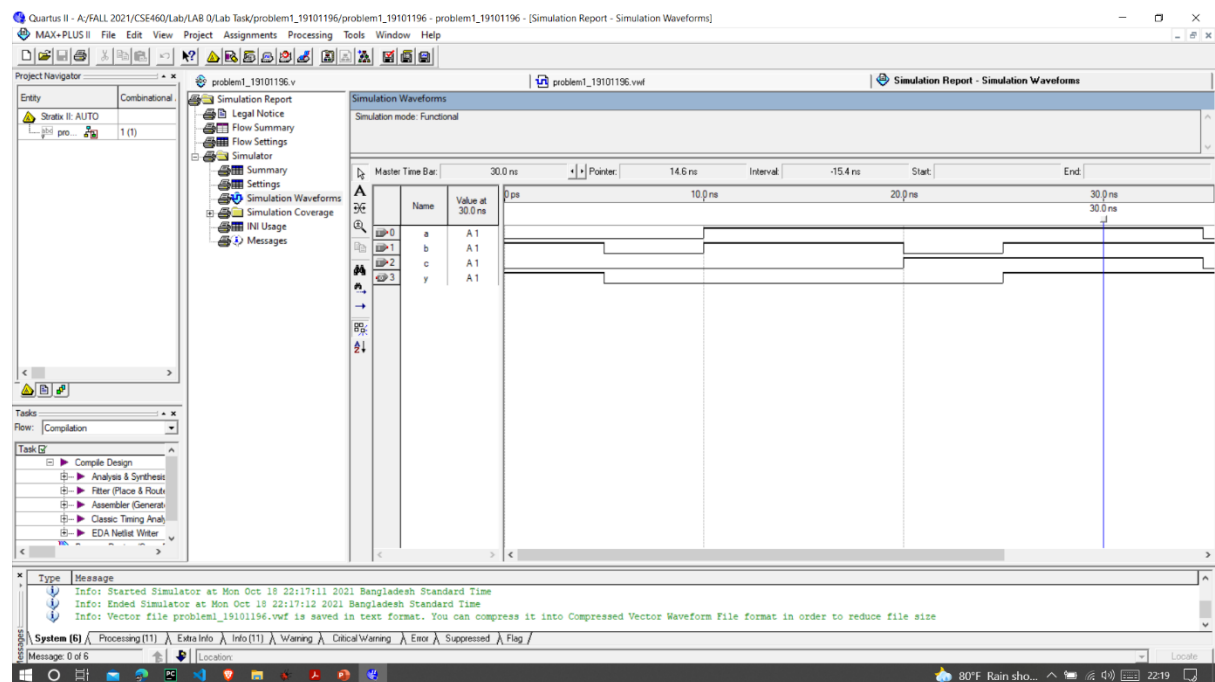
For both time instances, the timing diagram input and output values match with the above truth table.

C.

Waveform (random values to the input pins at half grid intervals):



Simulation Report (random values to the input pins at half grid intervals):



From the above waveform, at time = 15ns, when A = 1, B = 1, C = 0 we get Y = 0

From the above waveform, at time = 22ns, when A = 1, B = 0, C = 1 we get Y = 0

For both time instances, the timing diagram input and output values match with the above truth table.

d.

$$Y = \sim A \sim B C + \sim A B \sim C + A \sim B \sim C + A B C$$

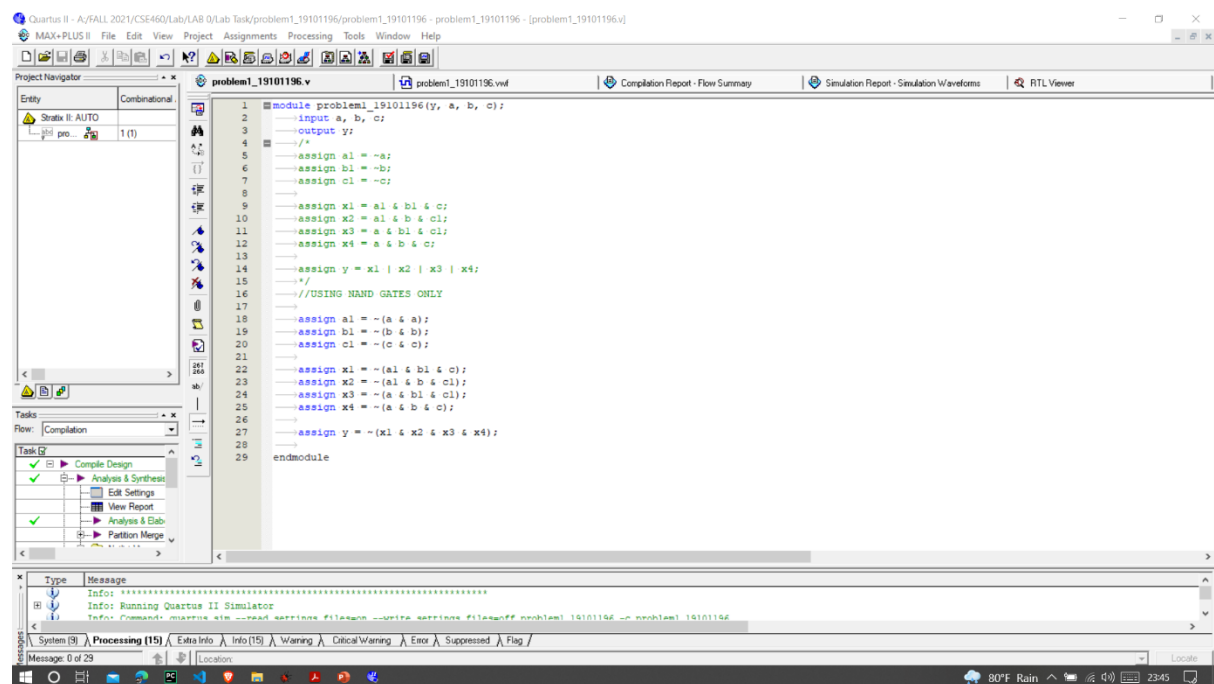
Converting the NOT Gates to NAND Gates:

$$Y = \sim(AA) \sim(BB) C + \sim(AA) B \sim(CC) + A \sim(BB) \sim(CC) + A B C$$

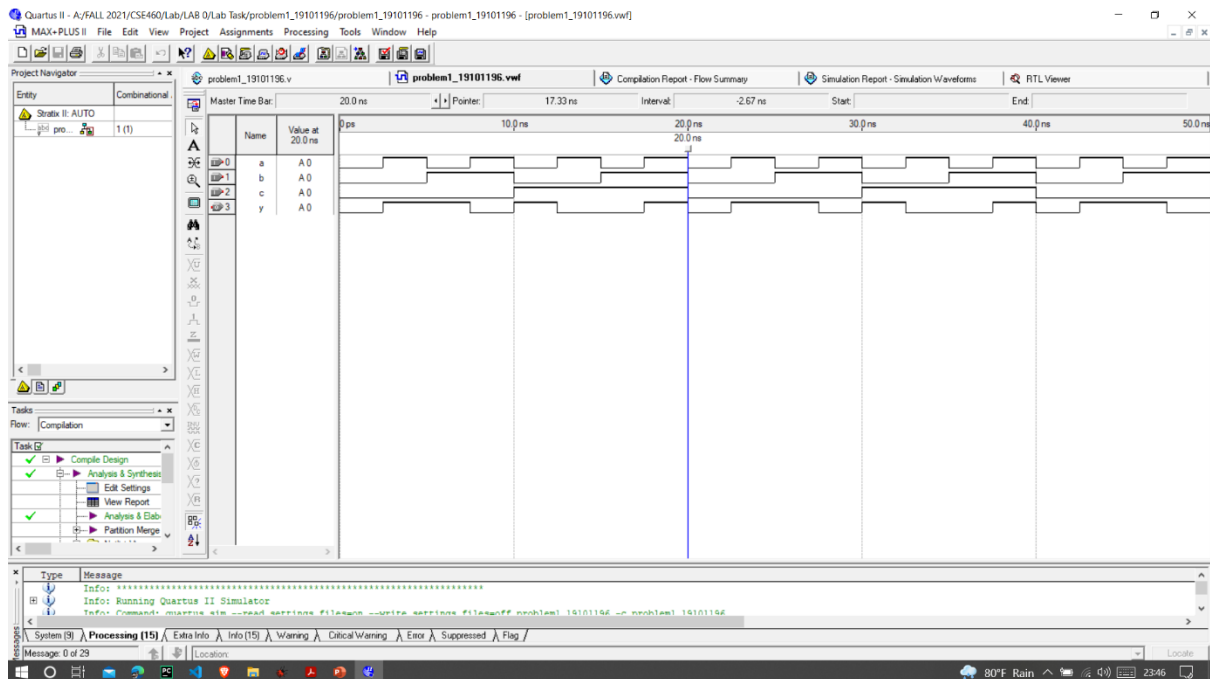
Converting the AND gates followed by OR gates to NAND Gates:

$$Y = \sim[\sim\{ \sim(AA) \sim(BB) C \} \sim\{ \sim(AA) B \sim(CC) \} \sim\{ A \sim(BB) \sim(CC) \} \sim\{ A B C \}]$$

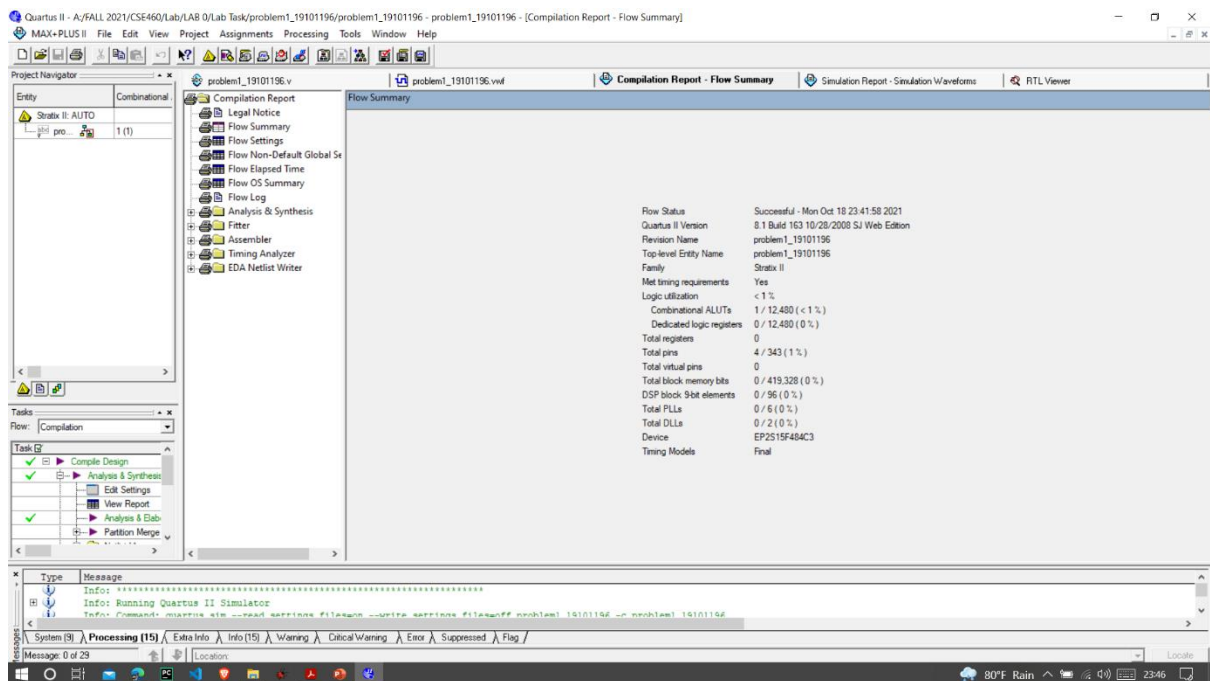
Code (using only NAND Gates):



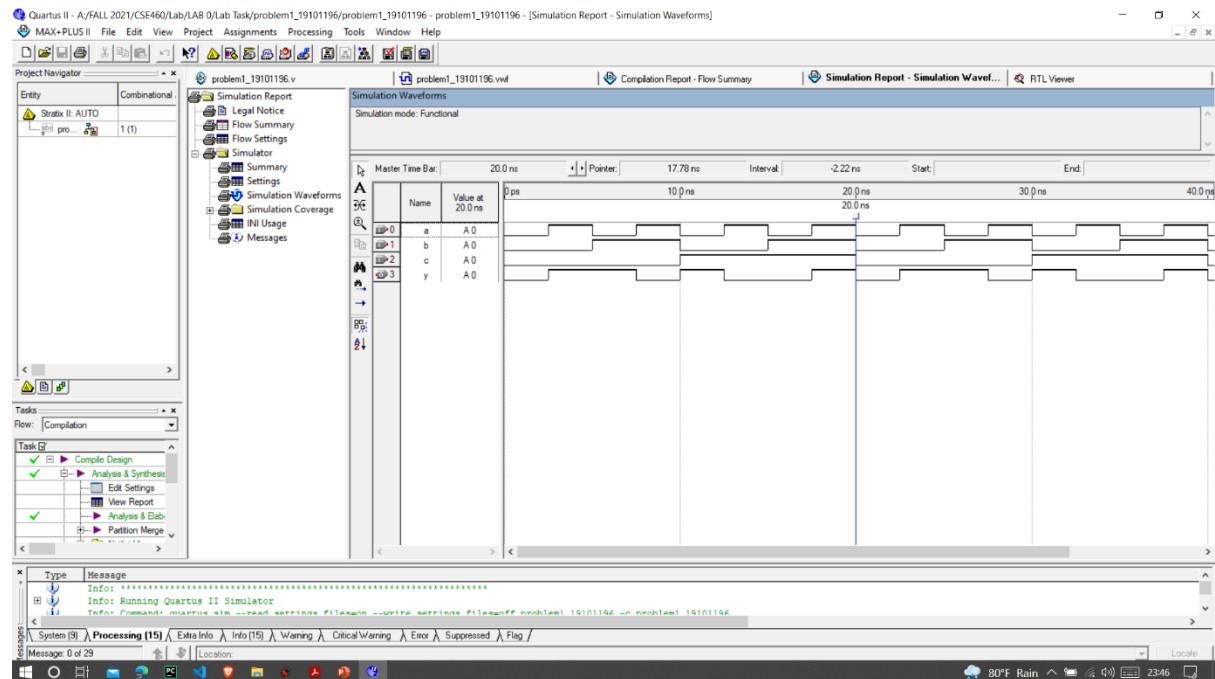
Waveform (using only NAND Gates):



Compilation Report (using only NAND Gates):



Simulation Report (using only NAND Gates):



RTL Circuit (using only NAND Gates):

