

CSE460

Lab Assignment 3

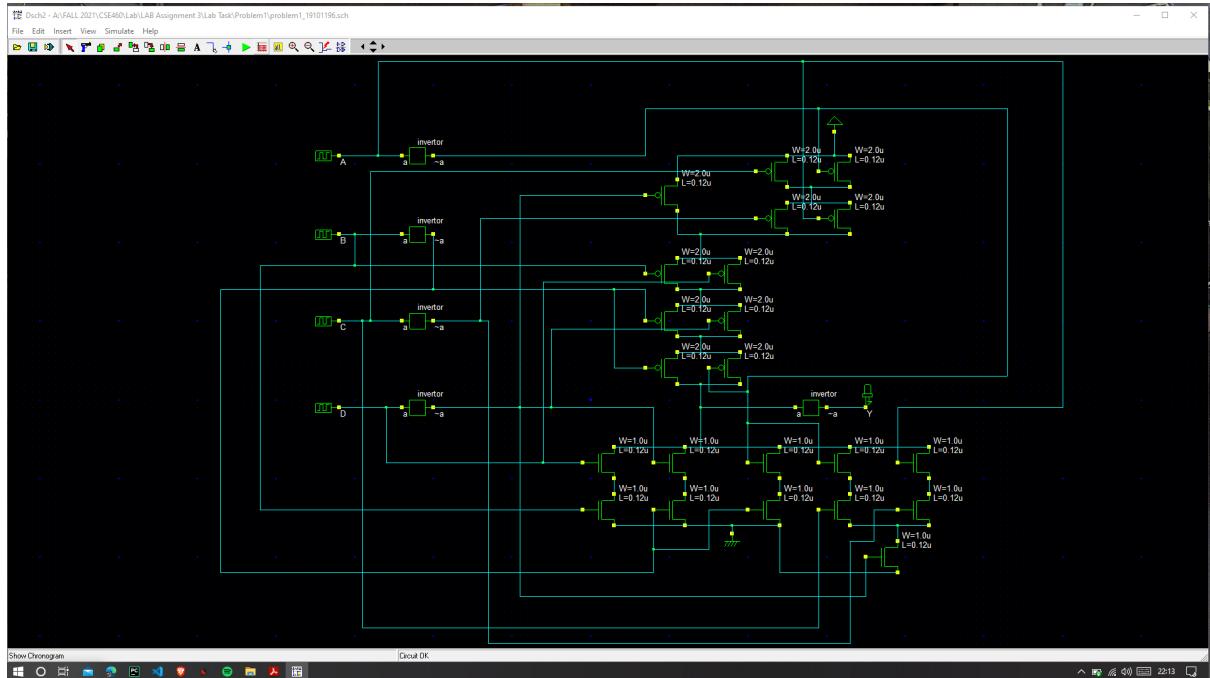
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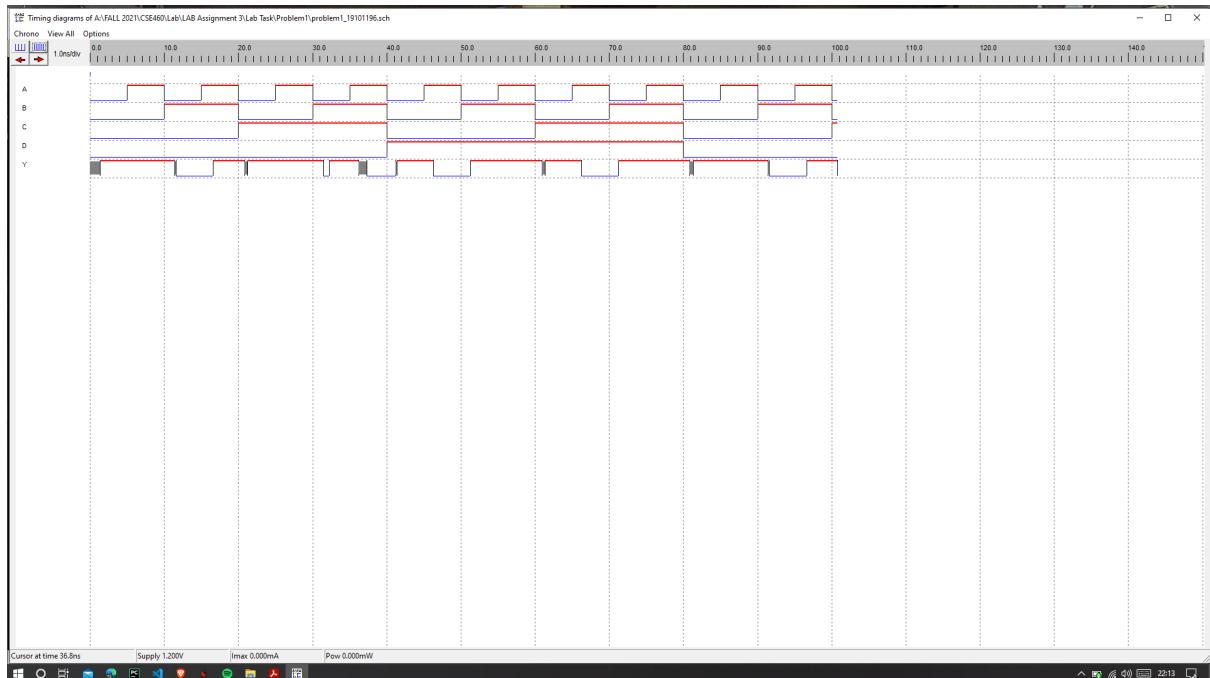
Section: 06

PROBLEM 1

Schematic:



Timing Diagram:



Problem 1

		AB	CD	Y	
		00	01	11	10
00	00	1	0	1	1
	01	1	d(1)	d(1)	0
11	11	d(1)	d(1)	1	0
	10	1	1	0	1

Considering all don't cares as 1, we get 4 1s vertically, 4 1s one each corner, 4 1s in middle, and a pair of 2 1s.

$$\begin{aligned}
 Y &= \bar{A}\bar{B} + \bar{B}\bar{D} + BD + \bar{A}\bar{C}\bar{D} + \bar{A}\bar{C}\bar{D}, \\
 &= \bar{A}\bar{B} + \bar{B}\bar{D} + BD + \bar{D}(\bar{A}\bar{C} + \bar{A}\bar{C})
 \end{aligned}$$

From timing diagram, it is TA to TA transition.

During 18.0 to 20.0, where A=1, B=1, C=0 and D=0, the timing diagram Y shows Y=1.

The output matches the theoretical value from K-map.

Since A=1, the nmos with $\bar{A}\bar{B}$ is off, so the series connection of $\bar{A}\bar{B}$ is open circuit. The same

for $\bar{A}\bar{C}$. Since B=1, nmos with $\bar{B}\bar{D}$ is off, hence an open circuit for $\bar{B}\bar{D}$ nmos. D=0, so BD is

also open circuit. A=1, C=0 and D=0, so

the nmos for \bar{D} , A and \bar{C} are on, so, the

output is short circuited to ground. This then passes through an inverter to give high output.

Since, A=1 and $\bar{C}=1$, their pmos will be off. $\bar{D}=1$ will also be off. So, the pull-up network forms an open circuit.

During 10.0 to 15.0, $A=0$, $B=1$, $C=0$, $D=0$ and output Y shows low voltage 0. This matches the theoretical value from K-map.

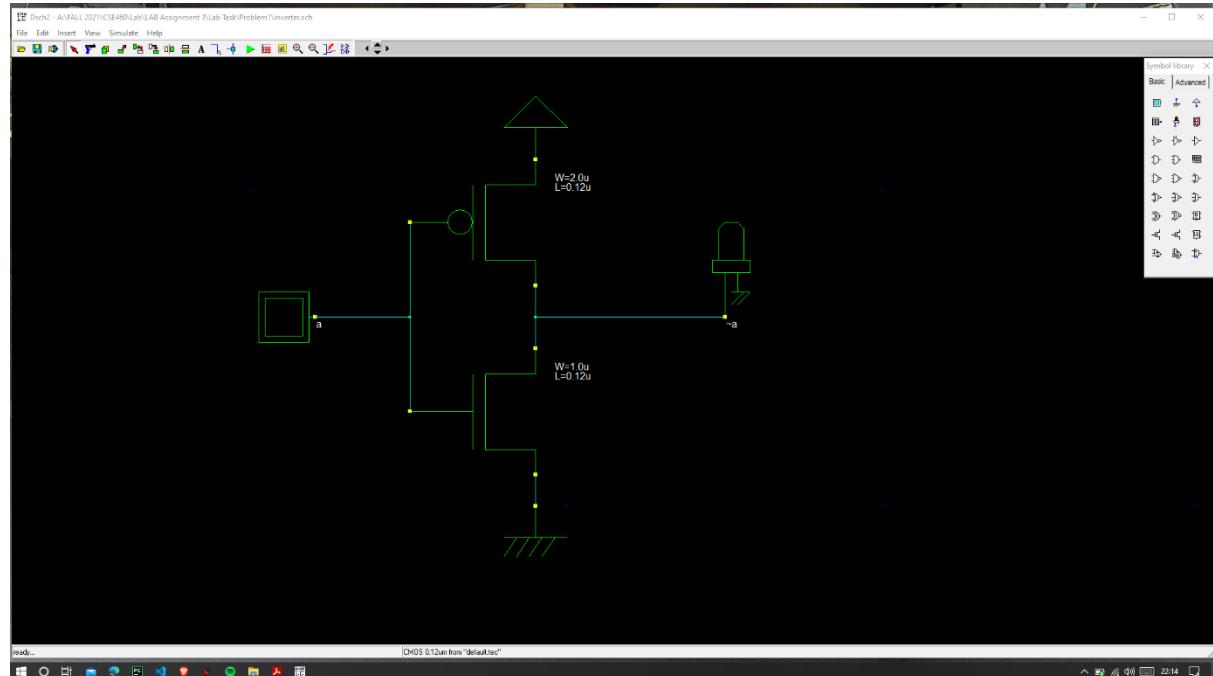
Since $D=0$, mos with D will be off. So, series connection of BD will be open circuit. $B=1$, so $\bar{B}=0$, mos are off. \bar{BD} and \bar{AC} will be open circuit. $A=0$, so \bar{AC} is open and $C=0$, so \bar{AC} is open. Hence, the pull-down network is open circuit.

Since $A=0$, mos with $\bar{A}=1$ will be on. So, parallel connection of \bar{AB} and \bar{AC} is shorted. $D=0$, so $\bar{D}=1$, hence \bar{BD} is shorted.

Since $B=1$, $\bar{B}=0$ mos will be on. So, parallel connection of \bar{AB} and \bar{BD} will be shorted circuit. $D=0$, so BD is short circuit. $C=0$ so \bar{AC} is shorted. $A=0$, so \bar{AC} is shorted. Hence the overall connection is shorted to the supply.

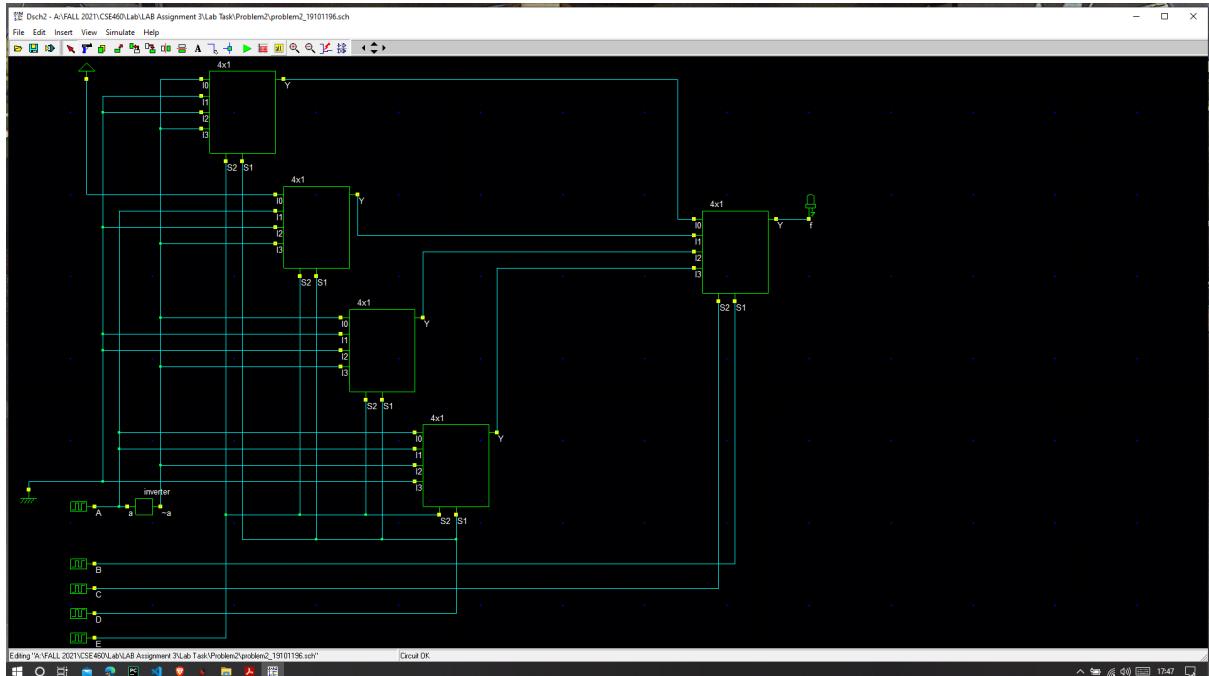
Hence, pull-up network is active and it gives high voltage. This goes through an inverter to be low voltage 0 output.

Inverter Sub-Circuit:

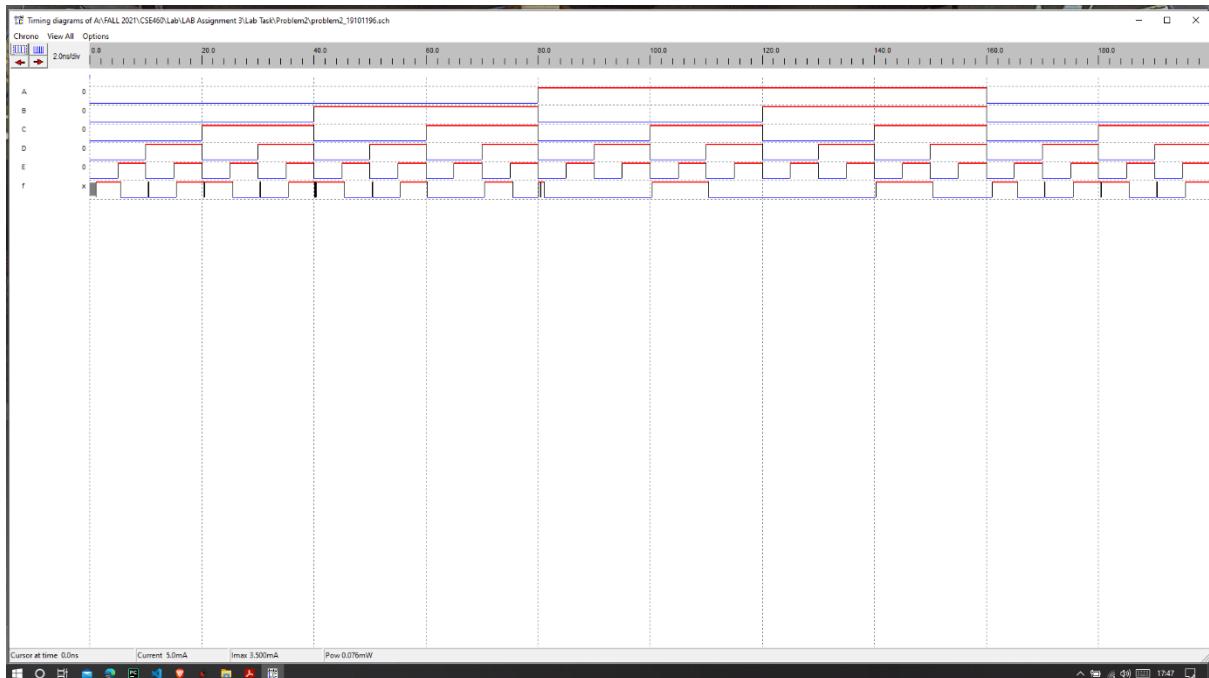


PROBLEM 2

Schematic:



Timing Diagram:



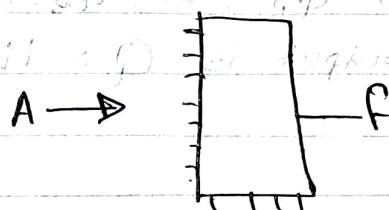
Problem 2

16) $f(A, B, C, D, E) = \sum(0, 4, 5, 8, 9, 12, 15, 21, 22, 29, 30)$; don't care?

So, A, B, C, D, E are inputs of 5-bit AND gate. So, output is 5-bit.

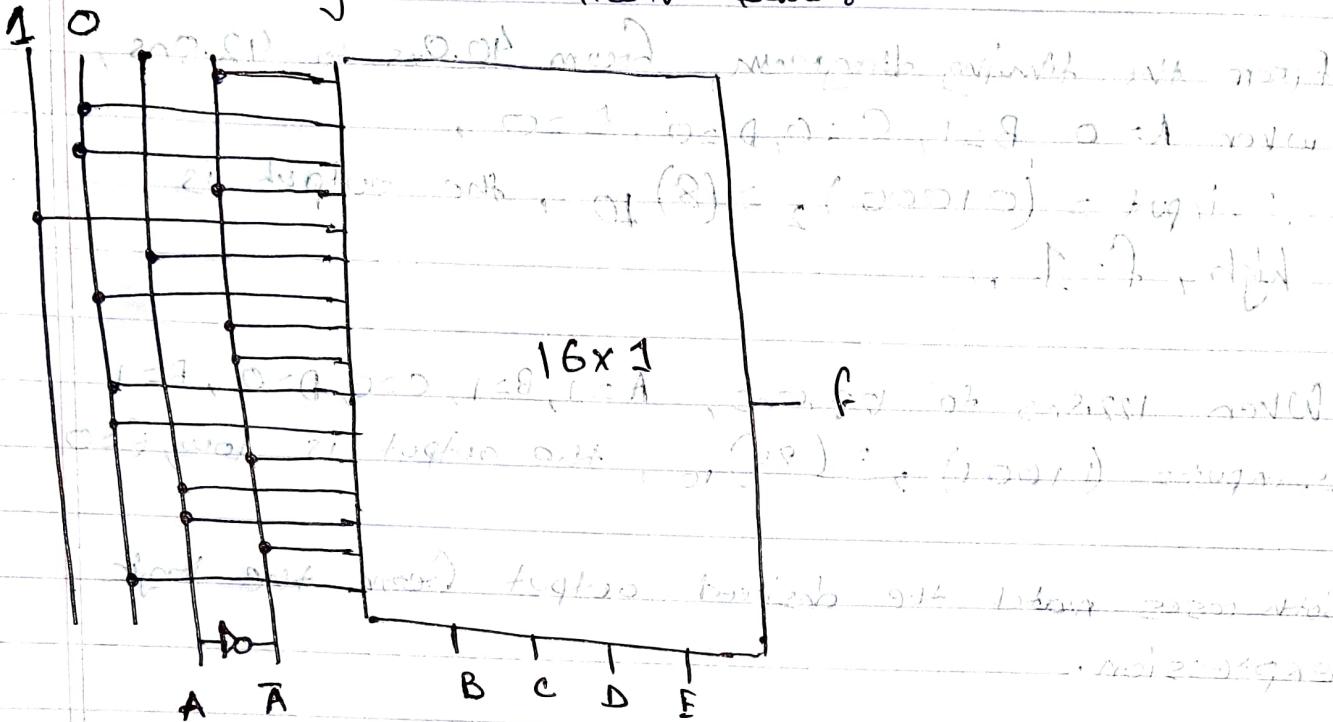
For 16x1 multiplexer, S-bit is 4-bit. So, S = 4.

So, let, B, C, D and E are 4-bit S bits.

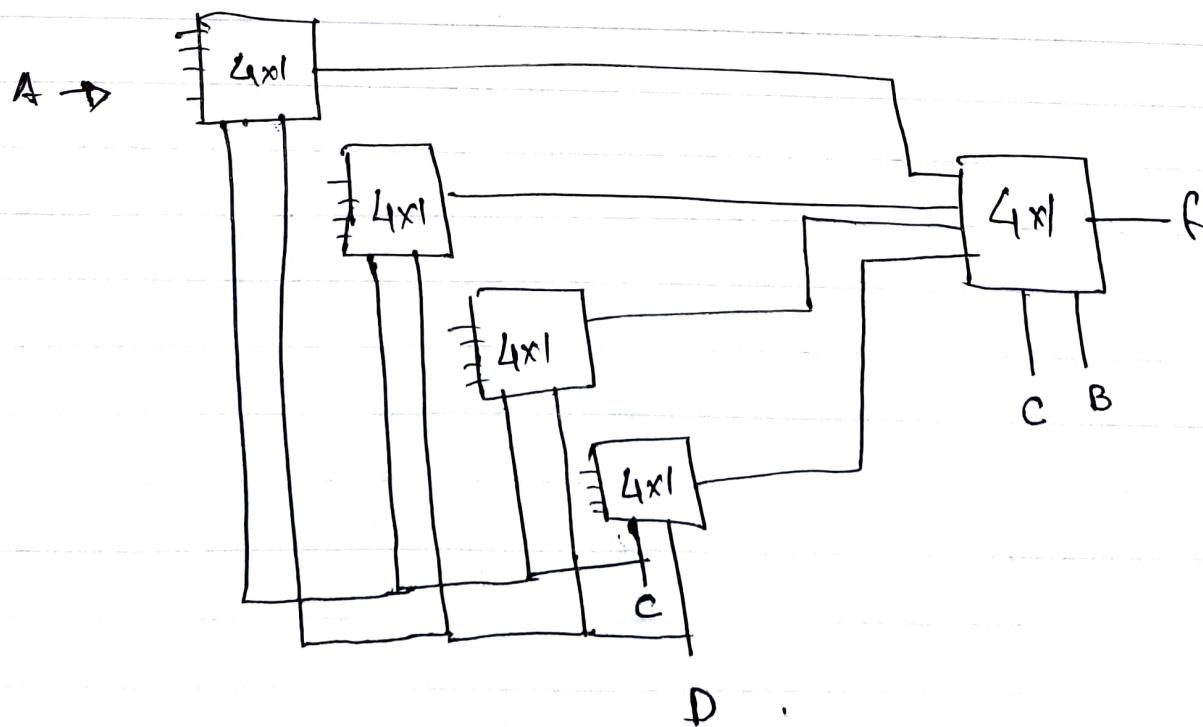


BCDE	0	1	f
0000	1	0	A
0001	0	0	0
0010	0	0	0
0011	1	0	\bar{A}
0100	1	1	1
0101	0	1	A
0110	d=0	0	0
0111	1	0	\bar{A}
1000	1	0	\bar{A}
1001	0	0	0
1010	0	0	0
1011	1	0	\bar{A}
1100	0	1	A
1101	0	1	A
1110	1	0	\bar{A}
1111	0	0	0

So, according to the fourth table:



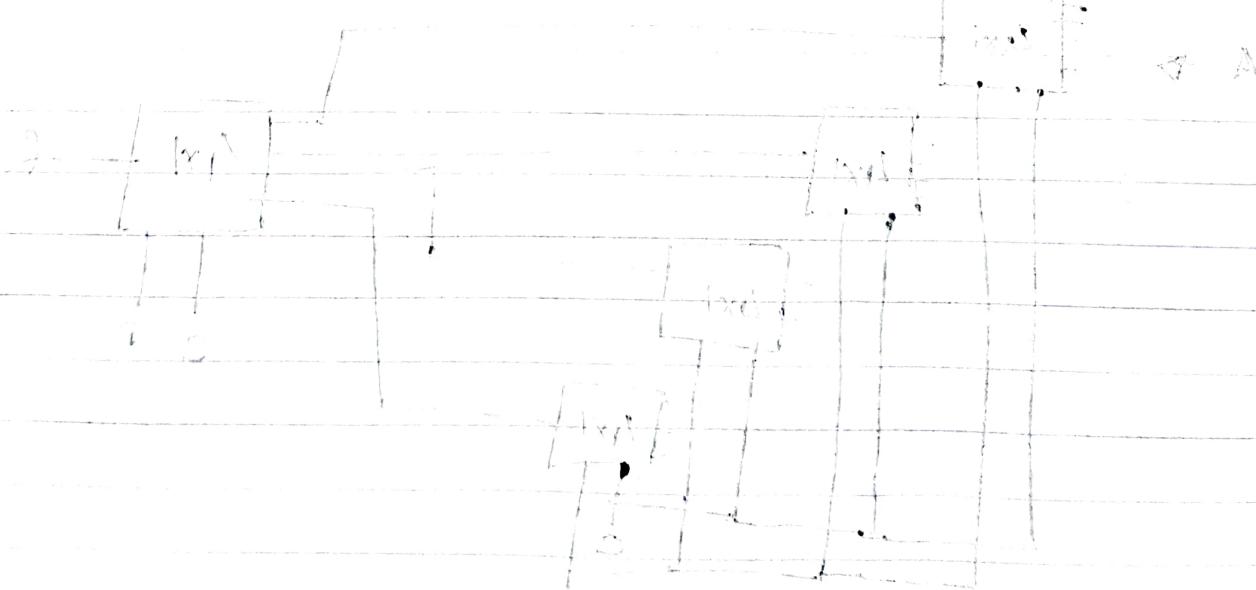
1 16×1 multiplexers can be split using 5 4×1 multiplexers.



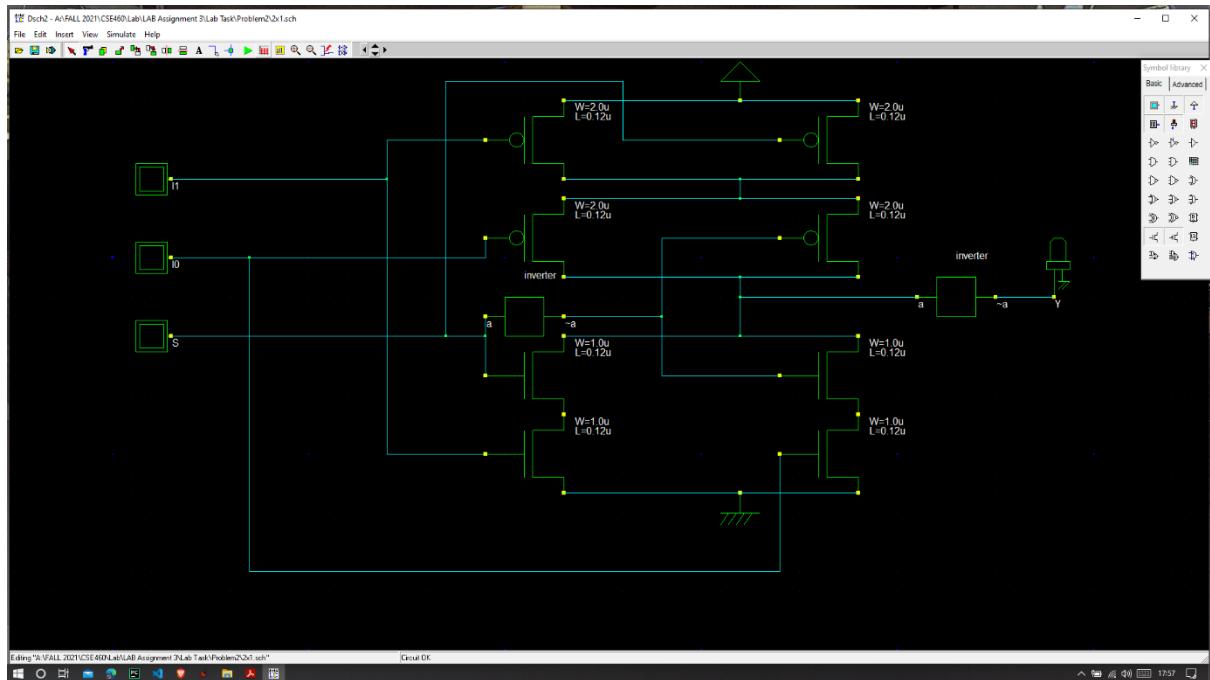
From the timing diagram, from 40.0ns to 42.5ns,
when A=0, B=1, C=0, D=0, E=0,
 \therefore input = $(01000)_2 = (8)_{10}$, the output is
high, f=1.

When 122.5ns to 128.0ns, A=1, B=1, C=0, D=0, E=1
 \therefore input = $(11001)_2 = (25)_{10}$, the output is low, f=0

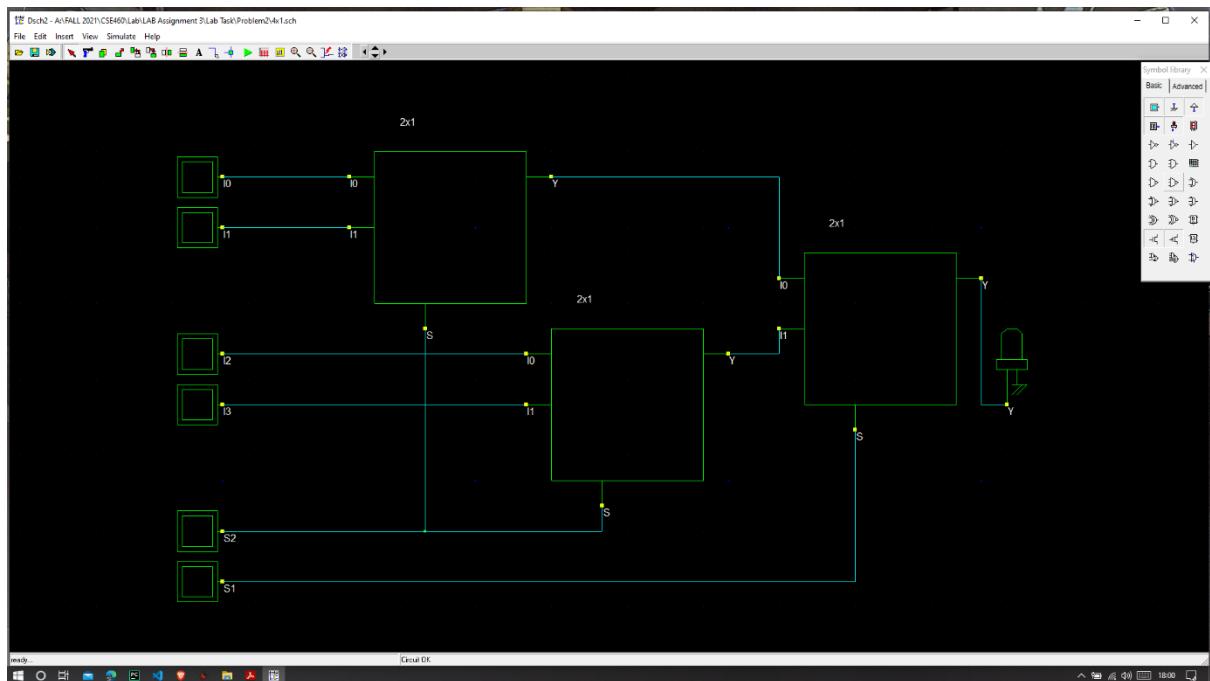
Both cases match the desired output from the logic
expression.



2x1 Sub-Circuit:

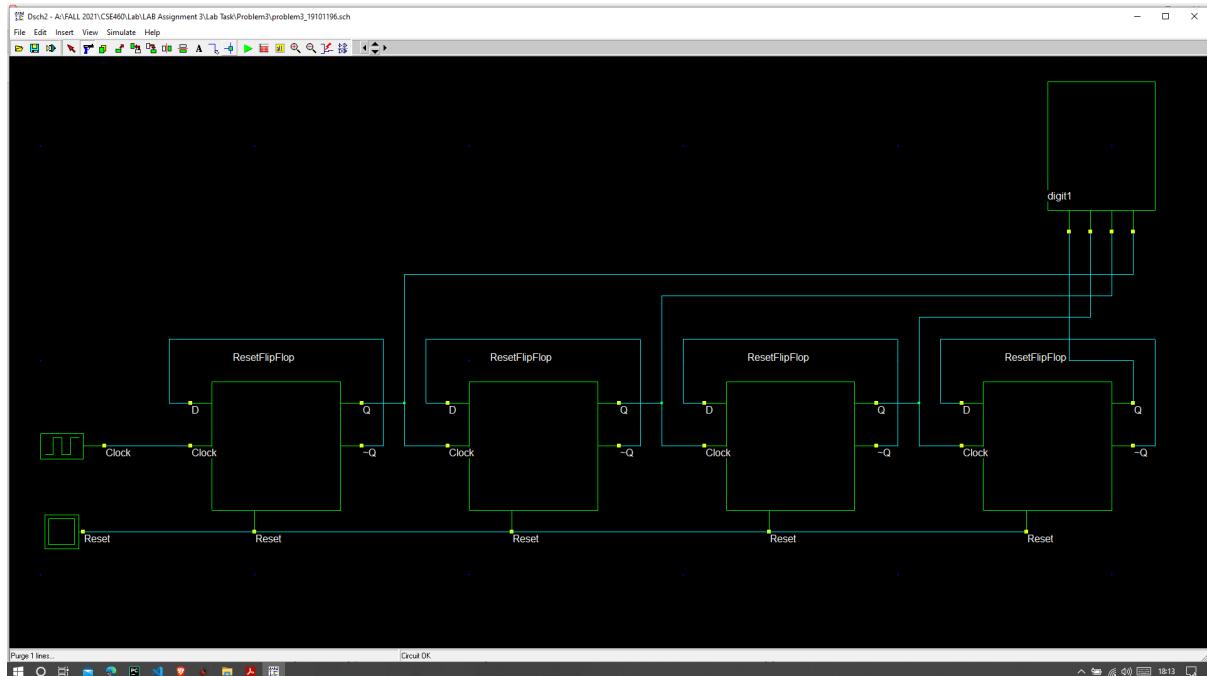


4x1 Sub-Circuit:

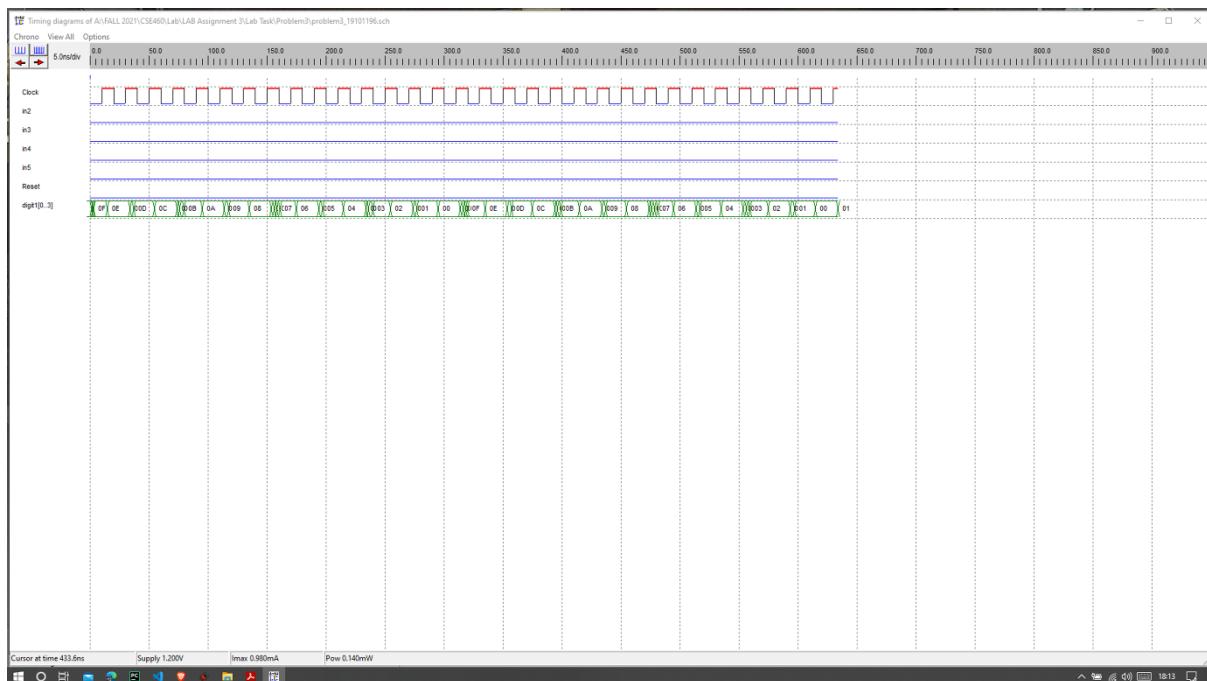


PROBLEM 3

Schematic:



Timing Diagram:



Problem 3

When Reset = 0, ~~D, \bar{D}~~ \Rightarrow Q will equal D.

When Reset = 1, ~~D, \bar{D}~~ \Rightarrow D = 0, $\bar{D} = 1$

Reset	<u>D</u>	<u>Out</u>	Reset	0	1
0	0	0	0	0	1
0	1	1	1	0	0
1	0	0			

i. Out = Reset \cdot D

Controller logical expression of Reset \cdot D

The 4 bit down counter uses 4 positive edge triggered ~~latch~~ D flip-flops.

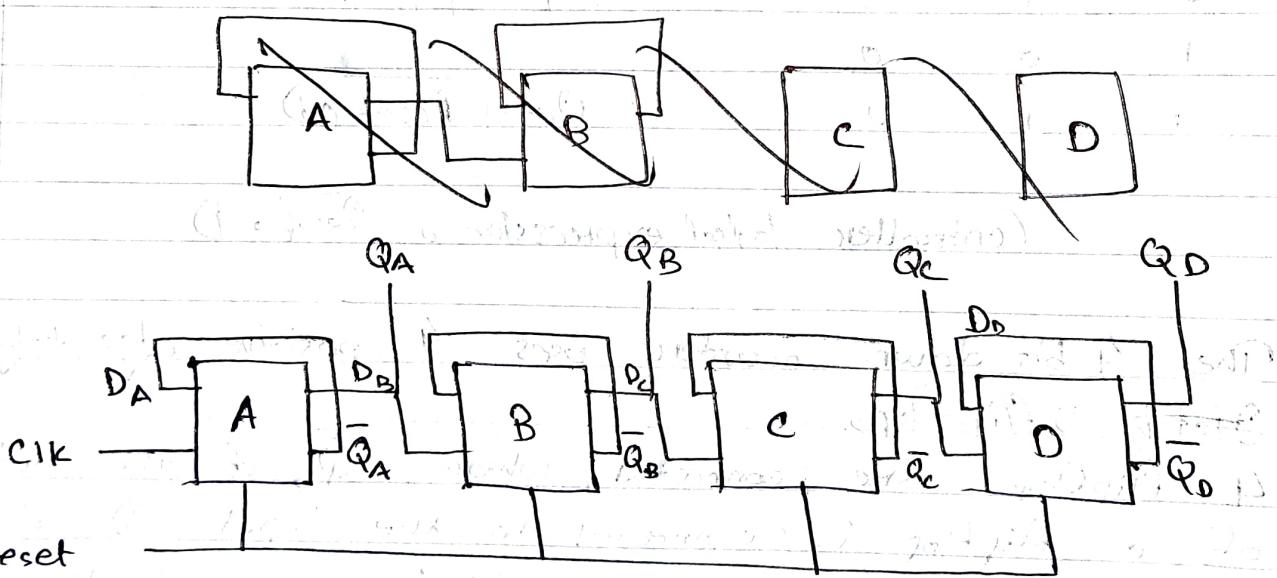
4 flip-flops are connected, where \bar{Q}_i of the output of a flip-flop is connected to the input D of the same flip-flop. The output Q is ~~com~~ of the least significant bit is connected to the clock of the flip-flop with next least significant bit output, and so on.

From the timing diagram, it is observed, the 4 bit output gives ~~1111~~ \Rightarrow 1111₍₂₎ or F(hex) is the first positive edge of clock. Then it decreases decrements by 1 bit to E(hex). It gradually

decreases to O_{hex}) at timestamp ~~300.0~~, the positive edge before the timestamp 300.0. This completes one cycle. The count then starts again from F_{hex} to O_{hex} at around 6250 timestamp from the timing diagram.

~~For each clock pulse, the output of the counter is updated.~~

~~When all bits are 1, it is a full count.~~

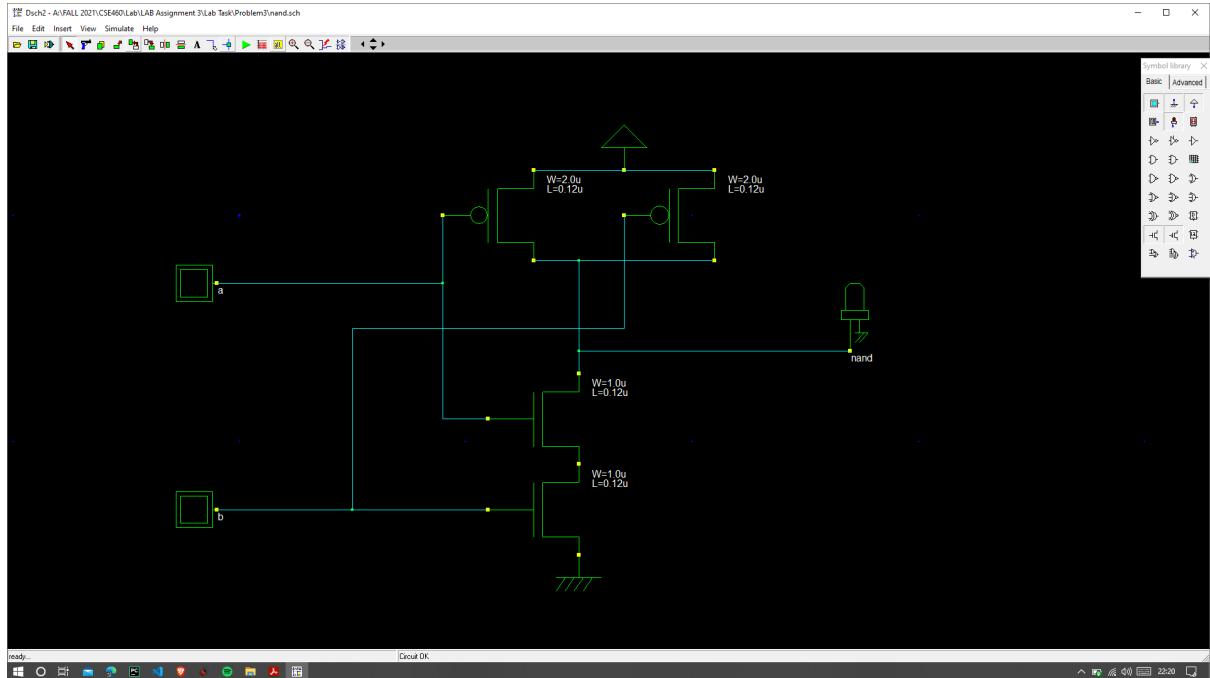


When output is F_{hex} , all bits are high. $Q = 1111$ (where Q_A is LSB and Q_D is MSB). So, $Q_A = 1$ and $\bar{Q}_A = 0$. In the next positive edge of clock, \bar{Q}_A which is connected to D_A is copied to Q_A . So, $Q_A = 0$ and hence $\bar{Q}_A = 1$. Now, the new output is $Q = 1110$, which is E_{hex} .

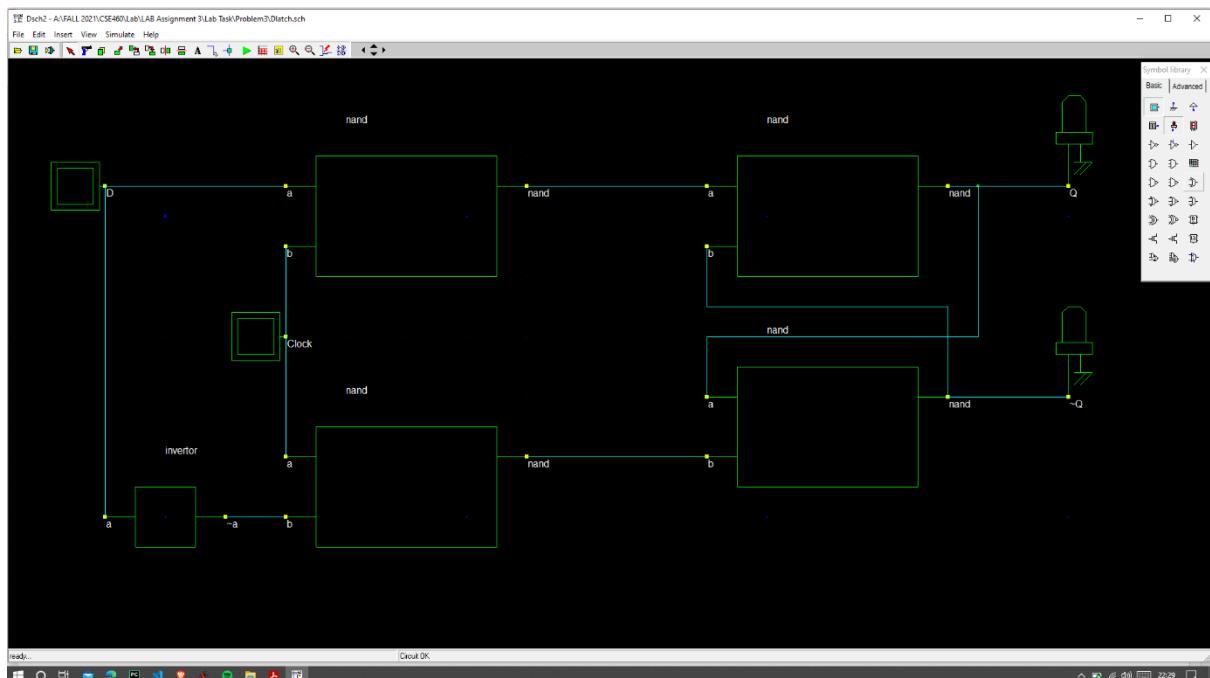
Now, $Q_A = 0$, $\bar{Q}_A = 1$, $Q_B = 1$, $\bar{Q}_B = 0$ (In next positive edge of clock, $\bar{Q}_A = D_A = 1$ is copied to Q_A . So, $Q_A = 1$ and $\bar{Q}_A = 0$. Since Q_A is connected to Clock of B, its clock faces a positive edge. So, $\bar{Q}_B = D_B = 0$ is copied to Q_B . So, $Q_B = 0$ and $\bar{Q}_B = 1$. Now, the new output is $Q = 1101$, which is D (hex).

This sequence is followed as the output Q₁ counts from F(hex) or 1111₍₂₎ to O(hex) or 0000₍₂₎.

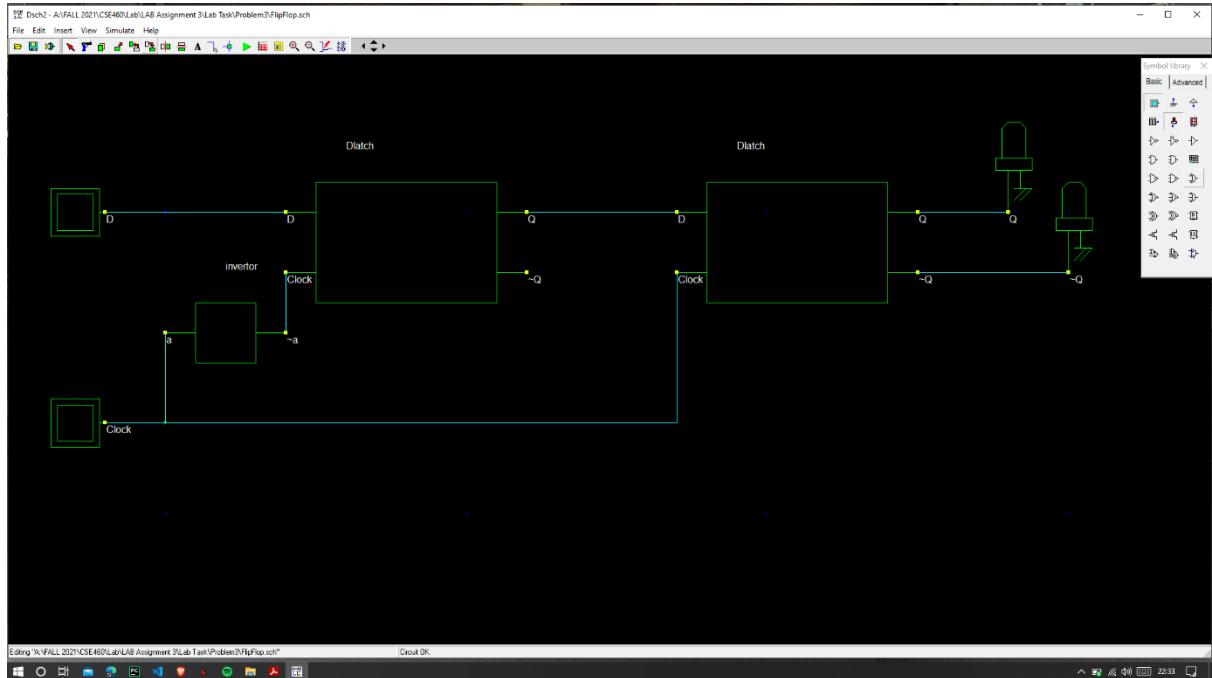
NAND Sub-Circuit:



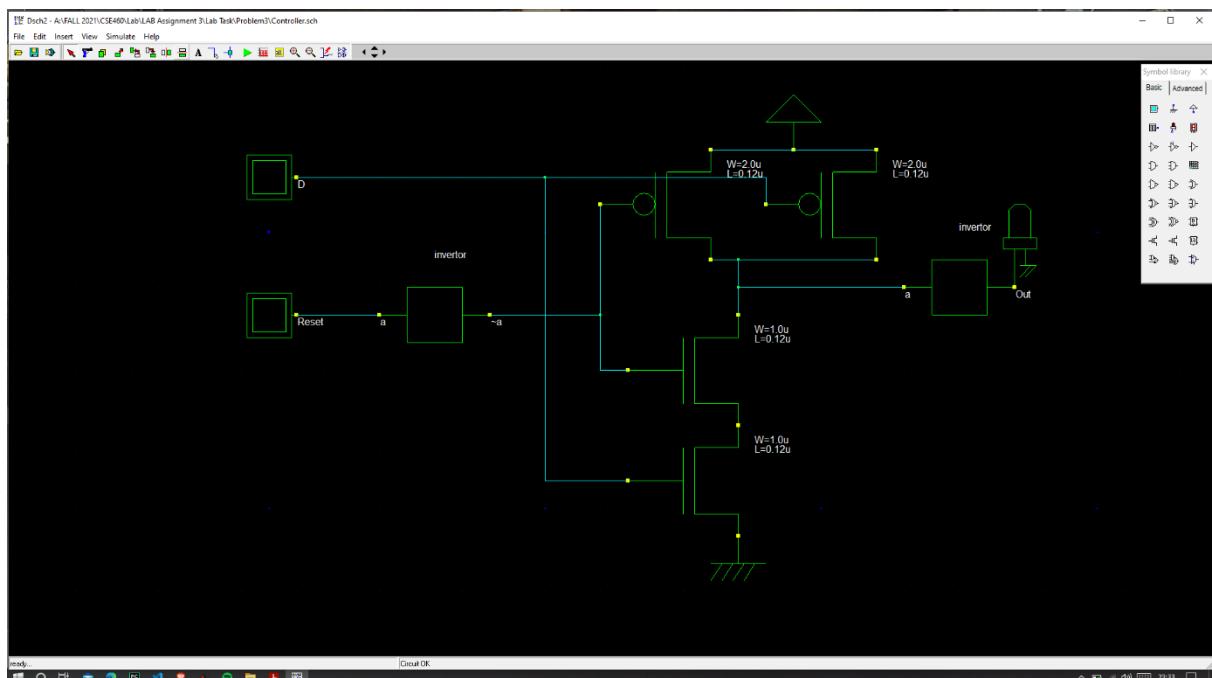
D-latch Sub-Circuit:



D-FlipFlop Sub-Circuit:



Controller Sub-Circuit:



FlipFlop with Reset Sub-Circuit:

