CSE460

Lab Assignment 4

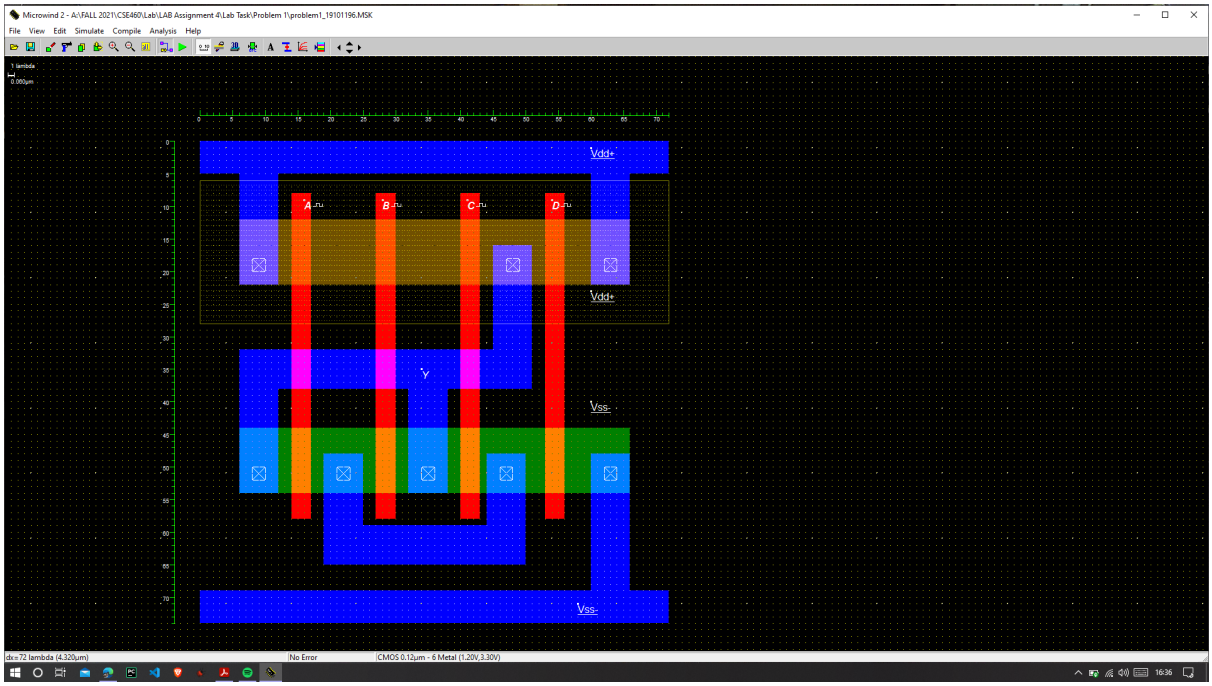
AHMAD AL ASAD

ID: 19101196

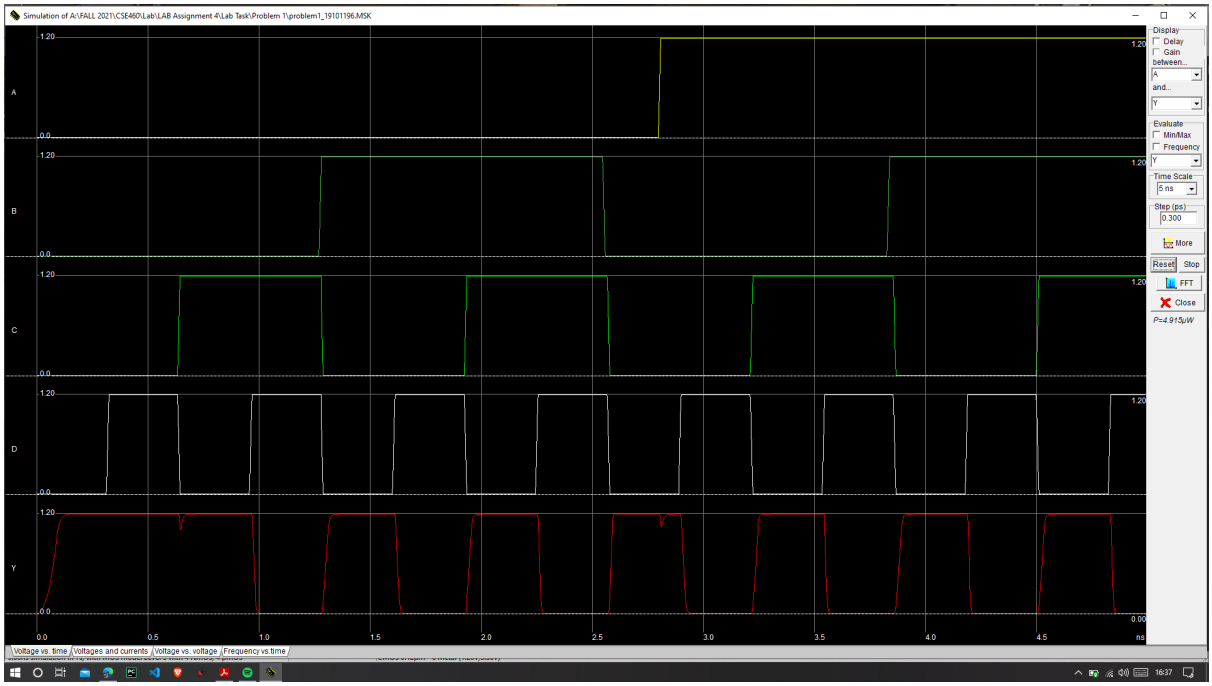
Section: 06

PROBLEM 1

Layout:

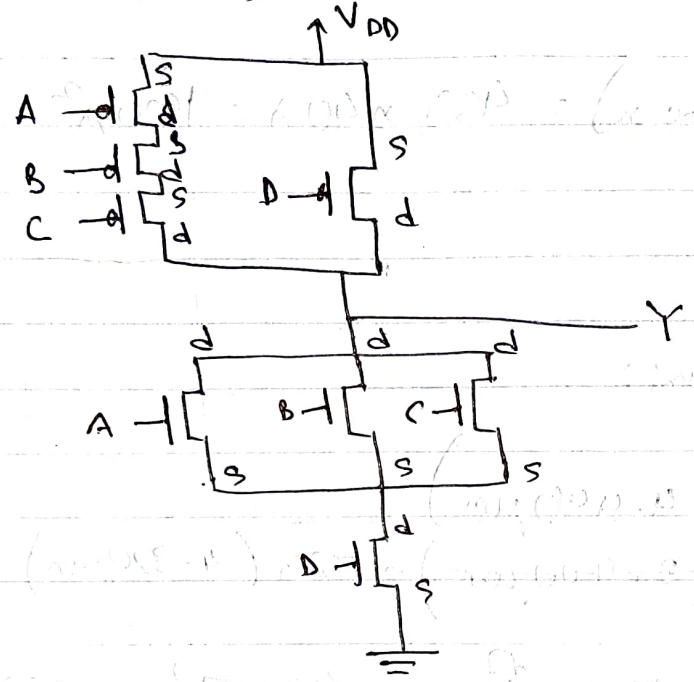


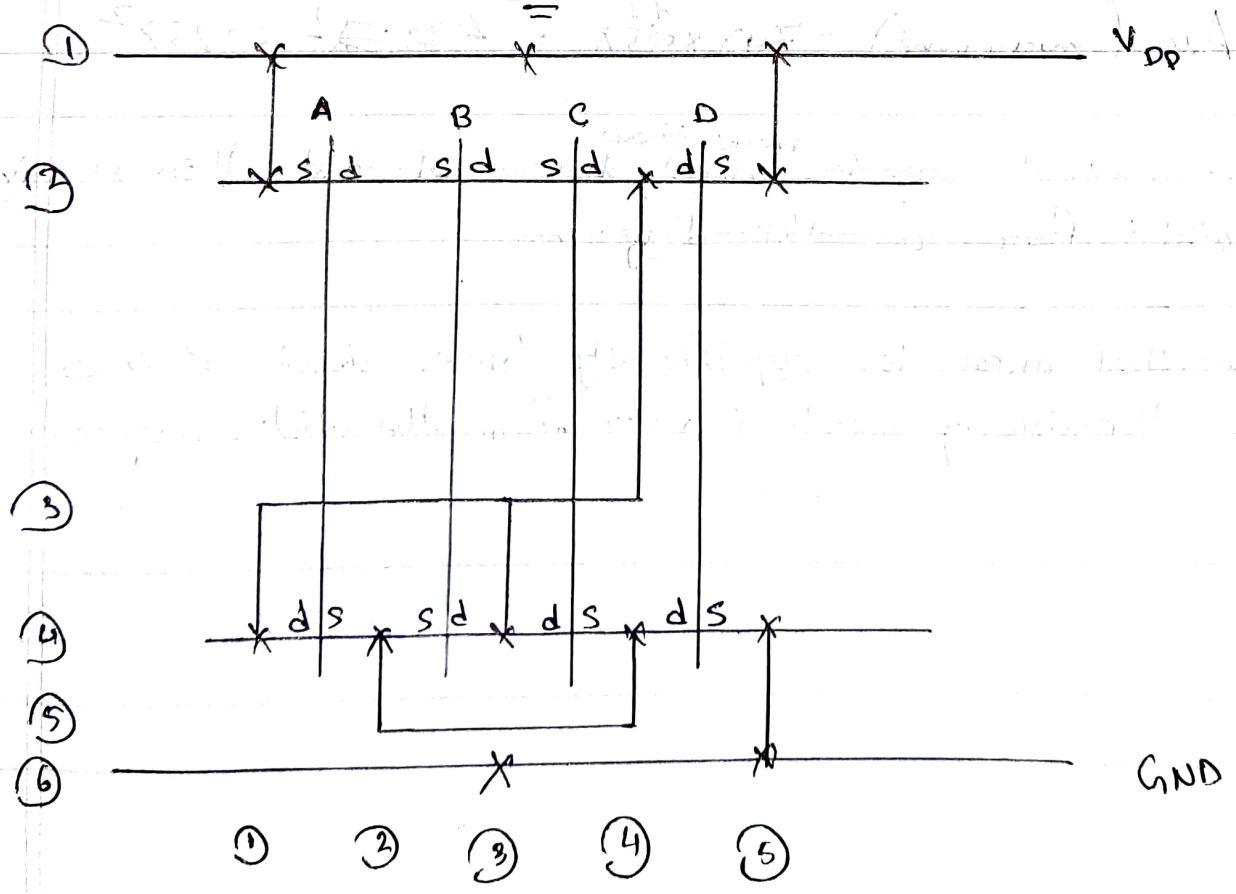
Timing Diagram:



Problem 1:

$$Y = \overline{(A+B+C)D}$$





height: 6 tracks: $6 \times 8\lambda = 48\lambda$

~~weight:~~

width: 5 tracks: $5 \times 8\lambda = 40\lambda$

~~Area~~ Area (stick diagram) $= 48\lambda \times 40\lambda = 1920\lambda^2$

From ~~microwind~~ microwind:

$d_y = 74\lambda$ (4.440 μm)

$d_x = 72\lambda$ (4.320 μm)

Area (microwind) $= 74\lambda \times 72\lambda = 5328\lambda^2$

~~The a practical area is more than almost twice of that theoretically calculated from a stick diagram.~~

The practical area is significantly large, almost 3 times of the theoretically calculated value from the stick diagram.

Truth Table

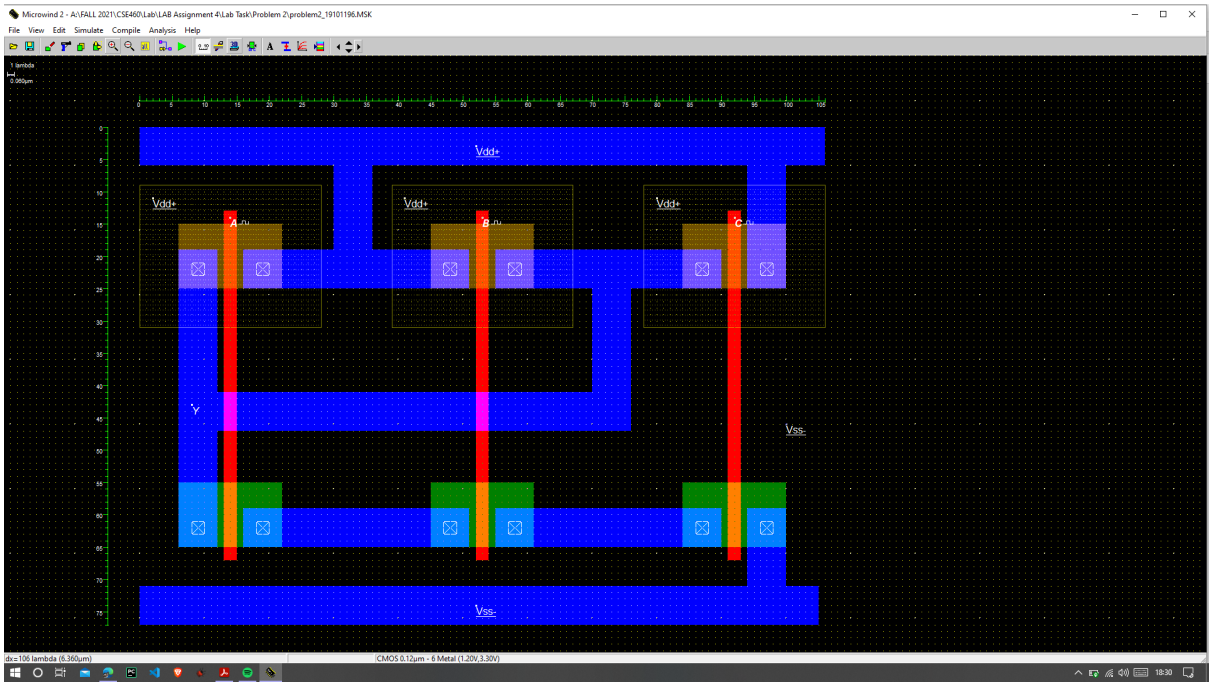
A	B	C	D	$Y = \overline{(A+B+C)D}$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

From timing diagram, between 0ns to 0.25ns, A=0, B=0, C=0, D=0. Then Y gives a high output 1. So, it matches the truth table.

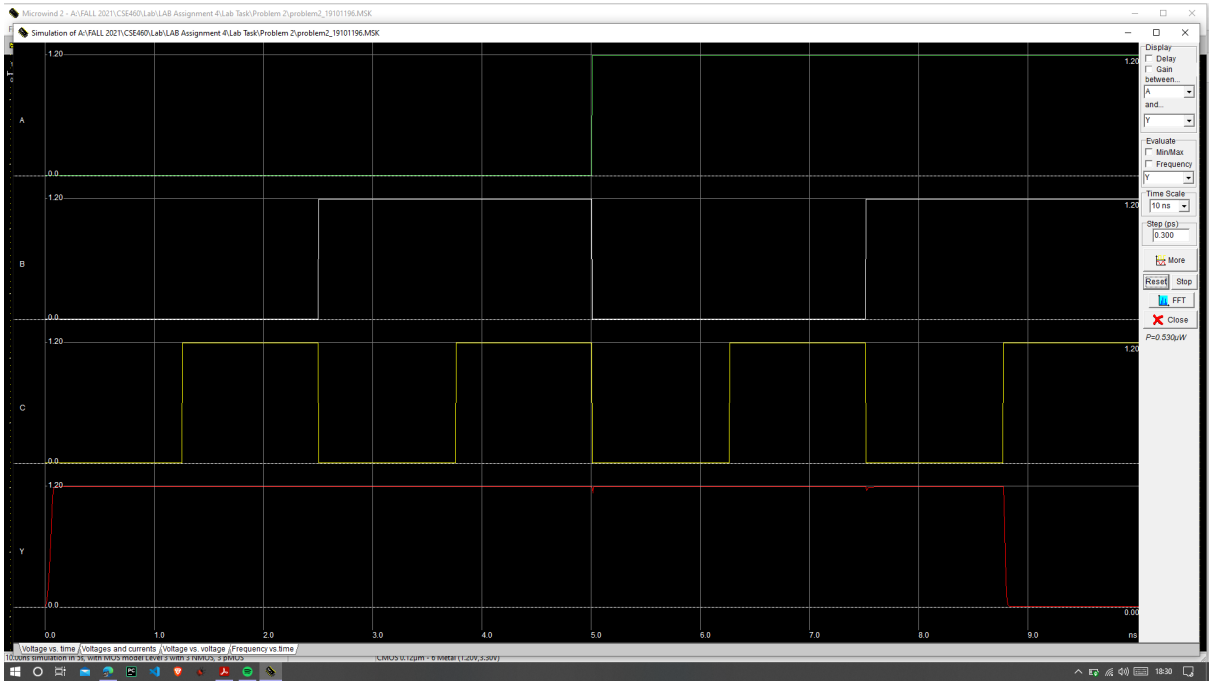
Between ~~2.0ns~~ 2.25ns to 2.5ns, A=0, B=1, C=1, D=1. Then Y gives low output 0. So, it matches the truth table.

PROBLEM 2

Layout:

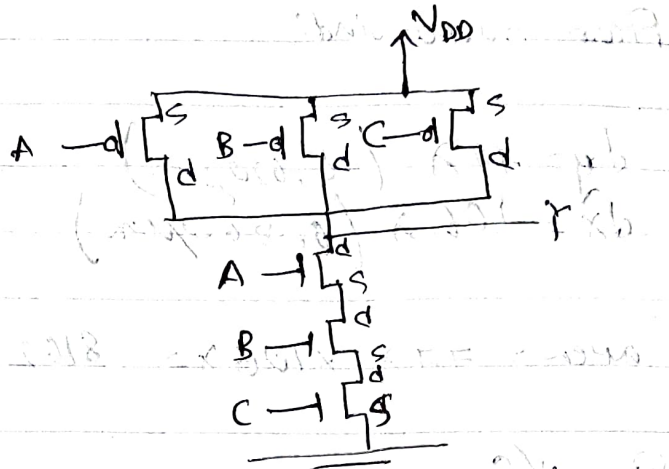


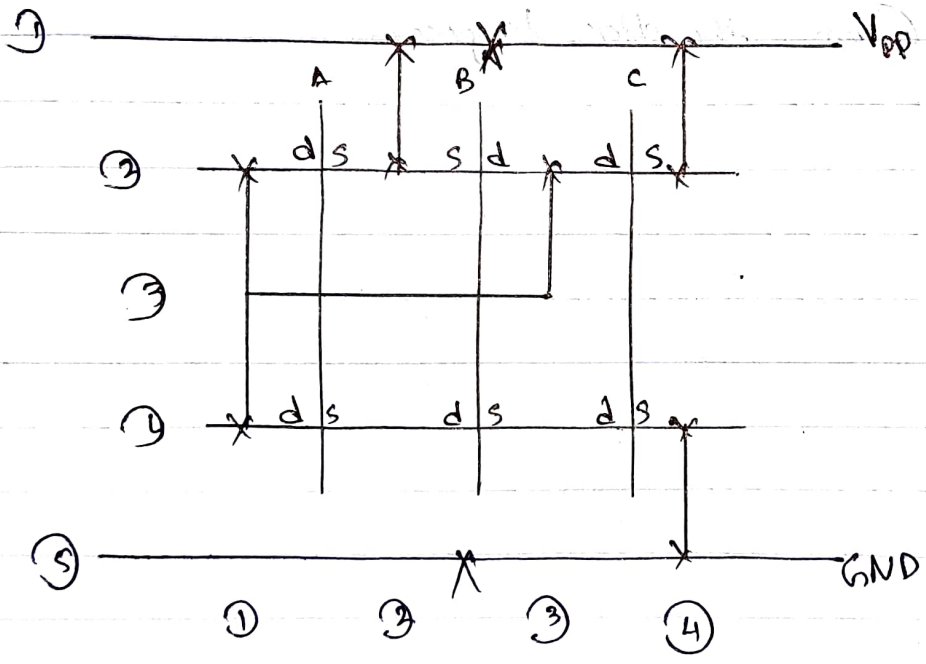
Timing Diagram:



Problem 2:

$Y = \overline{A \cdot B \cdot C}$





height: 5 tracks: $5 \times 8\lambda = 40\lambda$

width: 4 tracks: $4 \times 8\lambda = 32\lambda$

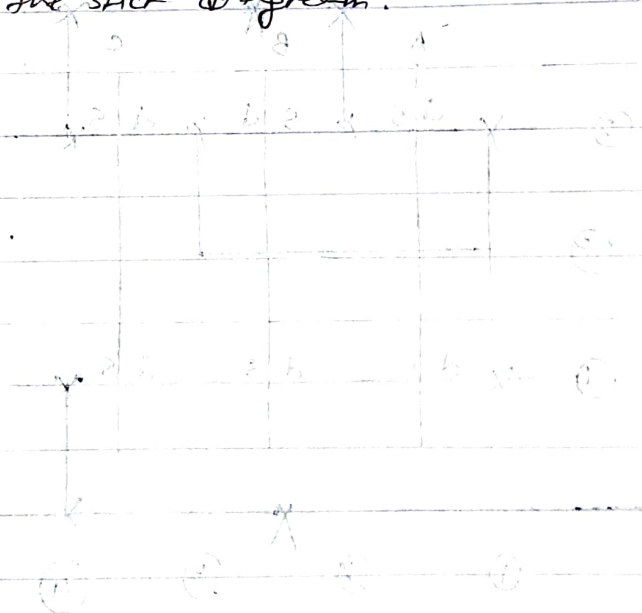
$\therefore$ area $= 40\lambda \times 32\lambda = 1280\lambda^2$

From microwind:

$dy = 77\lambda$ ($4.620\mu m$)
$dx = 106\lambda$ ($6.360\mu m$)

area $= 77\lambda \times 106\lambda = 8162\lambda^2$

The difference in area is a lot. The practical area from microwind is more than 6 times that of the theoritically calculated area from the stick diagram.



Truth table

A	B	C	$Y = \overline{A \cdot B \cdot C}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

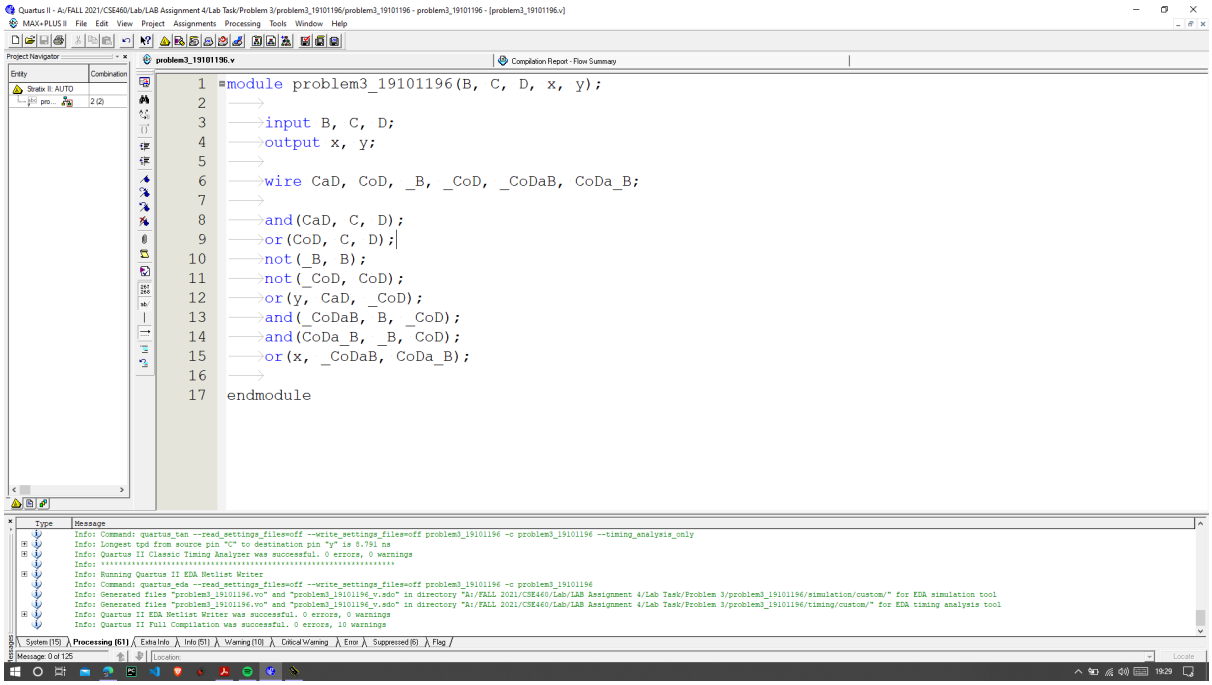
From timing diagram:

Between 1.25ns to 2.5ns, A=0, B=0, C=1. Then Y gives high output 1. So, it matches the truth table.

Between 8.75ns to 10ns, A = 1, B=1, C=1, Then Y gives low output 0. So, it matches the truth table.

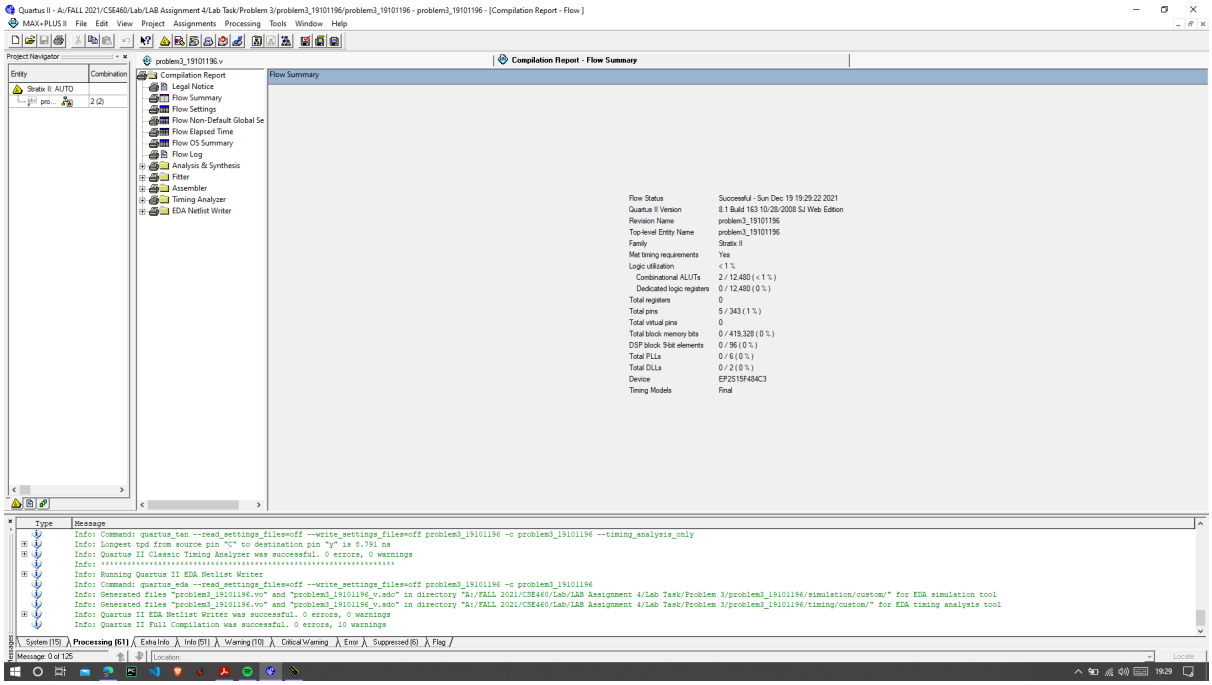
PROBLEM 3

Code:



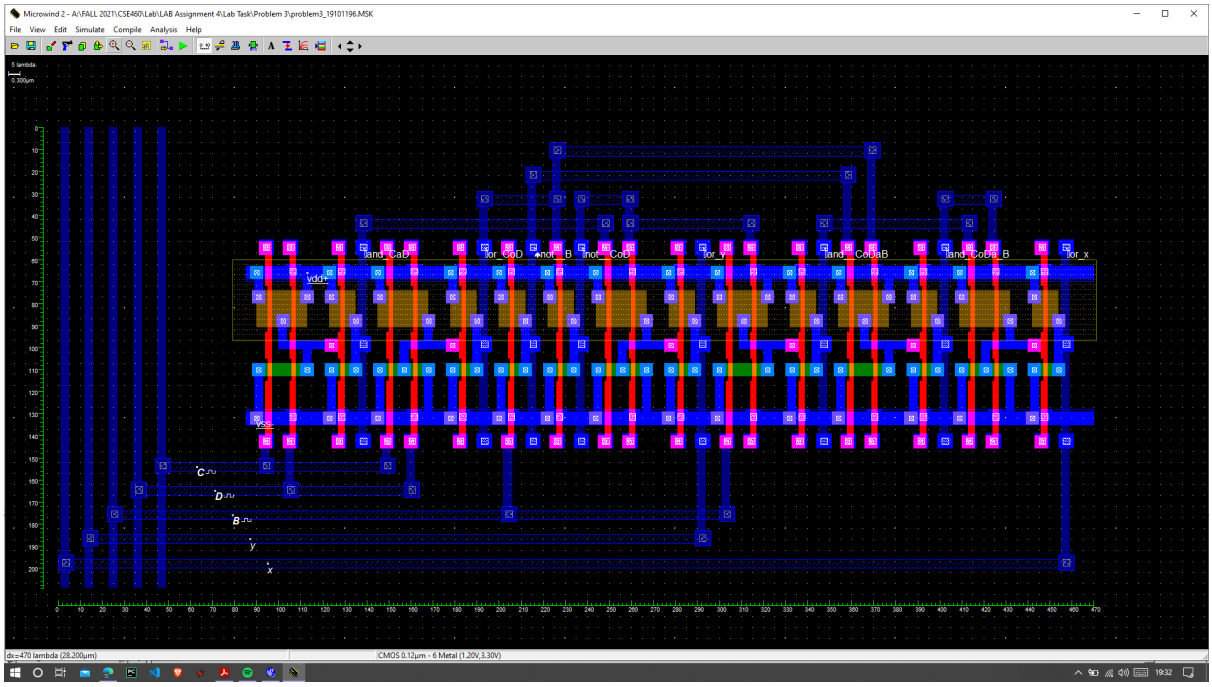
```
module problem3_19101196(B, C, D, x, y);

    input B, C, D;
    output x, y;

    wire CaD, CoD, _B, _CoD, _CoDaB, CoDa_B;

    and(CaD, C, D);
    or(CoD, C, D);
    not(_B, B);
    not(_CoD, CoD);
    or(y, CaD, _CoD);
    and(_CoDaB, B, _CoD);
    and(CoDa_B, _B, CoD);
    or(x, _CoDaB, CoDa_B);

endmodule
```

Compilation Report:

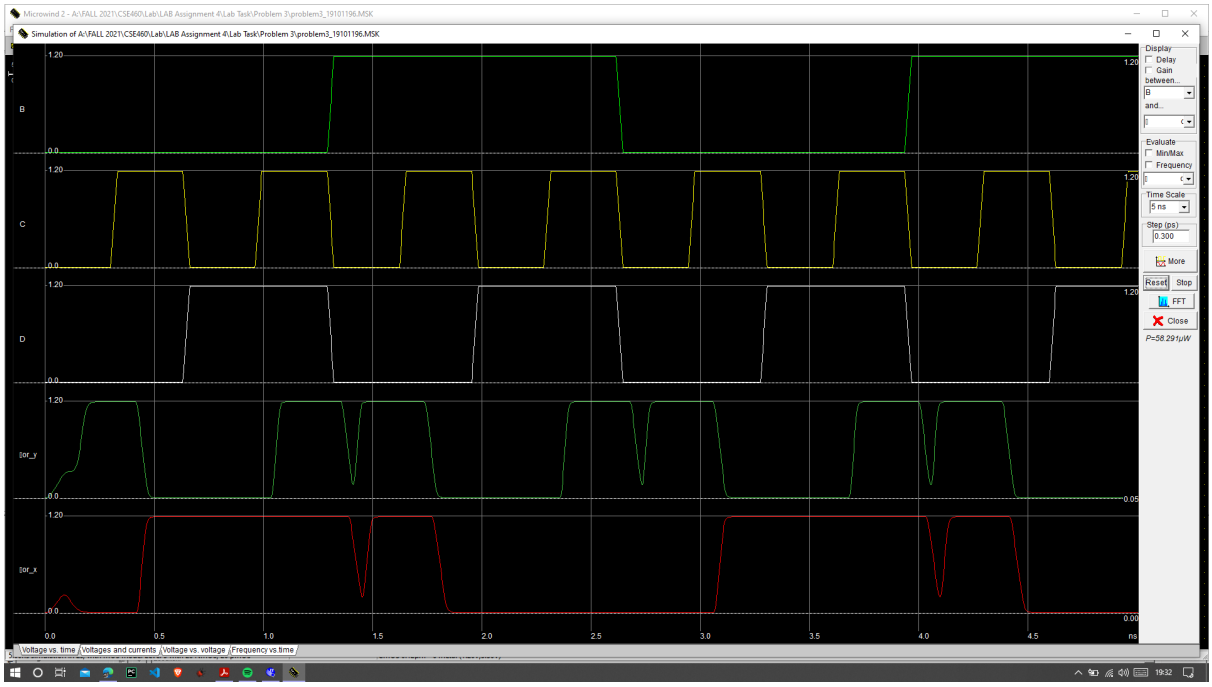


Flow Status	Successful - Sun Dec 19 19:29:22 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem3_19101196
Top-level Entity Name	problem3_19101196
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	2 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	5 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

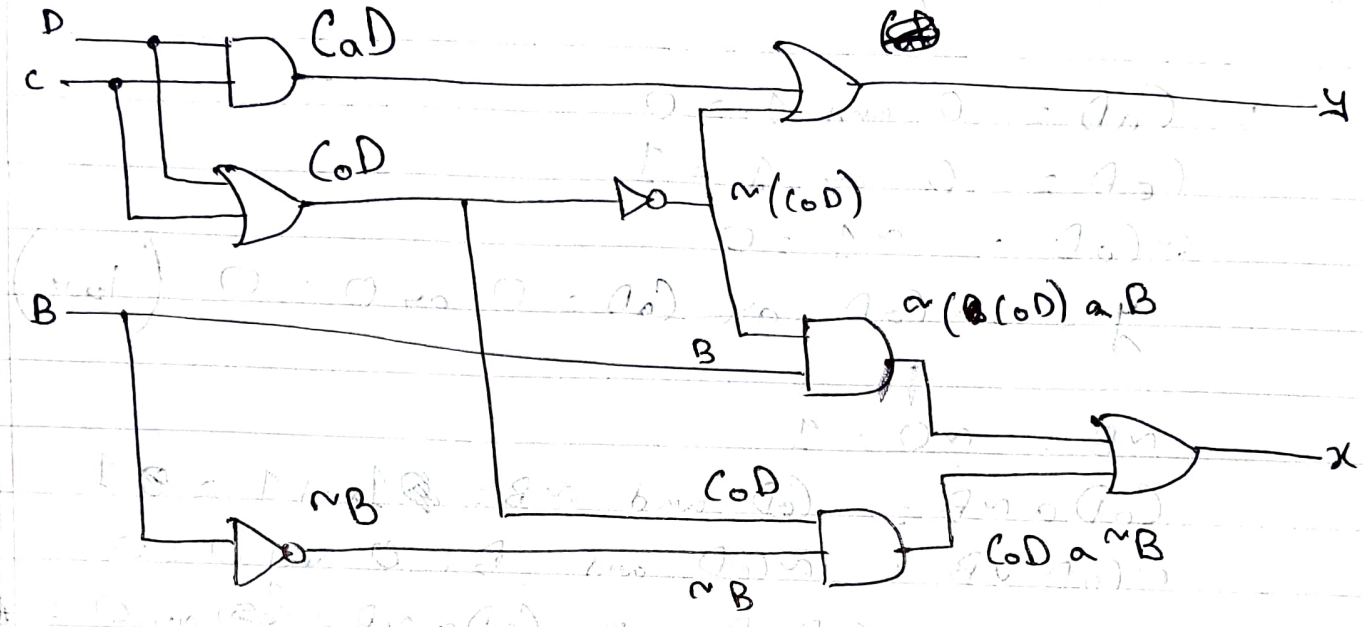
Layout:



Timing Diagram:



Problem 3



From microwind:

~~dy: 239λ (14.340 μm)~~

~~dx = 469λ (28.140μm)~~

~~Area = 239λ x 469λ = 112091λ²~~

dy = 209λ (12.540 μm)

dx = 470λ (28.200 μm)

Area = 209λ x 470λ

= 98230λ²

From timing diagram, at time stamp 0.75 ns,

B = 0, C = 0, D = 1

∴ C a D = 0 and 1 = 0

C o D = 0 or 1 = 1

~ C o D = ~ 1 = 0

y = ~ C o D or C a D = 0 or 0 = 0 (low)

~ B = ~ 0 = 1

C o D a ~ B = C o D and ~ B = 1 and 1 = 1

~ C o D a B = ~ C o D and B = 0 and 0 = 0

∴ x = ~ C o D a B or C o D a ~ B = 1 or 0 = 1 (high)

∴ When B = 0, C = 0, D = 1,

output y gives low 0 and x gives high 1

∴ The output from timing diagram matches the theoretical output.

At time stamp ~~[illegible]~~ 3.75 ns,

B = 0, C = 1, D = 1

C & D = 1 and 1 = 1

C | D = 1 or 1 = 1

~(C | D) = ~ 1 = 0

y = ~(C | D) or (C & D) = 1 or 0 = 1 (high)

~B = ~0 = 1

(C & D) & ~B = (C & D) and ~B = 1 and 1 = 1

~(C & D) & B = ~(C & D) and B = 0 and 0 = 0

x = ~(C & D) & B or (C & D) & ~B = 1 or 0 = 1 (high)

∴ when B = 0, C = 1, D = 1,

output y gives high 1 and x gives high 1.

∴ The output from the ~~timing~~ timing diagram matches the theoretical output.