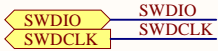
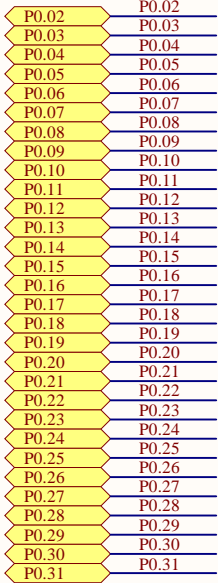
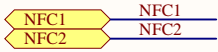


1	2	3	4
<div>Designator [02] - nRF52.SchDoc</div> <div></div>	<div>Designator [04] - SX1276.SchDoc</div> <div></div>	<div>Designator [03] - Inter-connects.SchDoc</div> <div></div>	<div>Designator [01] - Edge-connections.SchDoc</div> <div></div>
A			A
B			B
C			C
D			D
1	2	3	4

Title EE-02 nRF52 LoRa (SX1276) Module			<div><div></div><div>telenor digital</div></div>
Size: A4	Number:1	Revision 2.1	
Date: 08.03.2017	Time: 11:30:12	Sheet 1 of 5	
File: EE-02 pcbmodule.SchDoc			

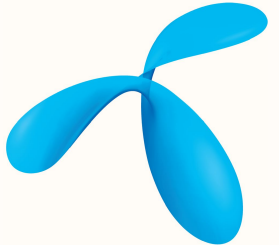
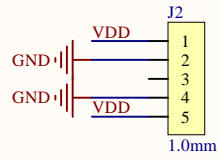
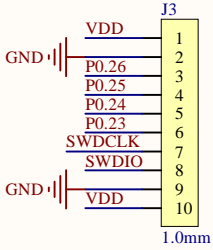
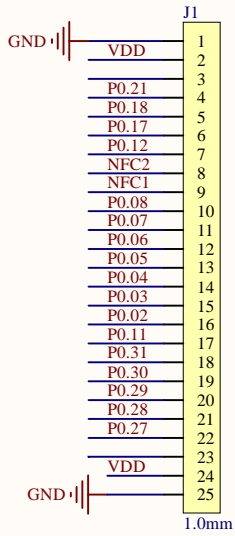


(no edge) Used as NFC1
(no edge) Used as NFC2

(no edge) DIO0
(no edge) DIO1
(no edge) DIO2
(no edge) DIO3

SX1276 nRESET
(no edge) DIO4
(no edge) DIO5
(no edge) SX1276 RXTX
(no edge) SX1276 SPI CS
SPI (MOSI)
SPI (MISO)
SPI (SCK)

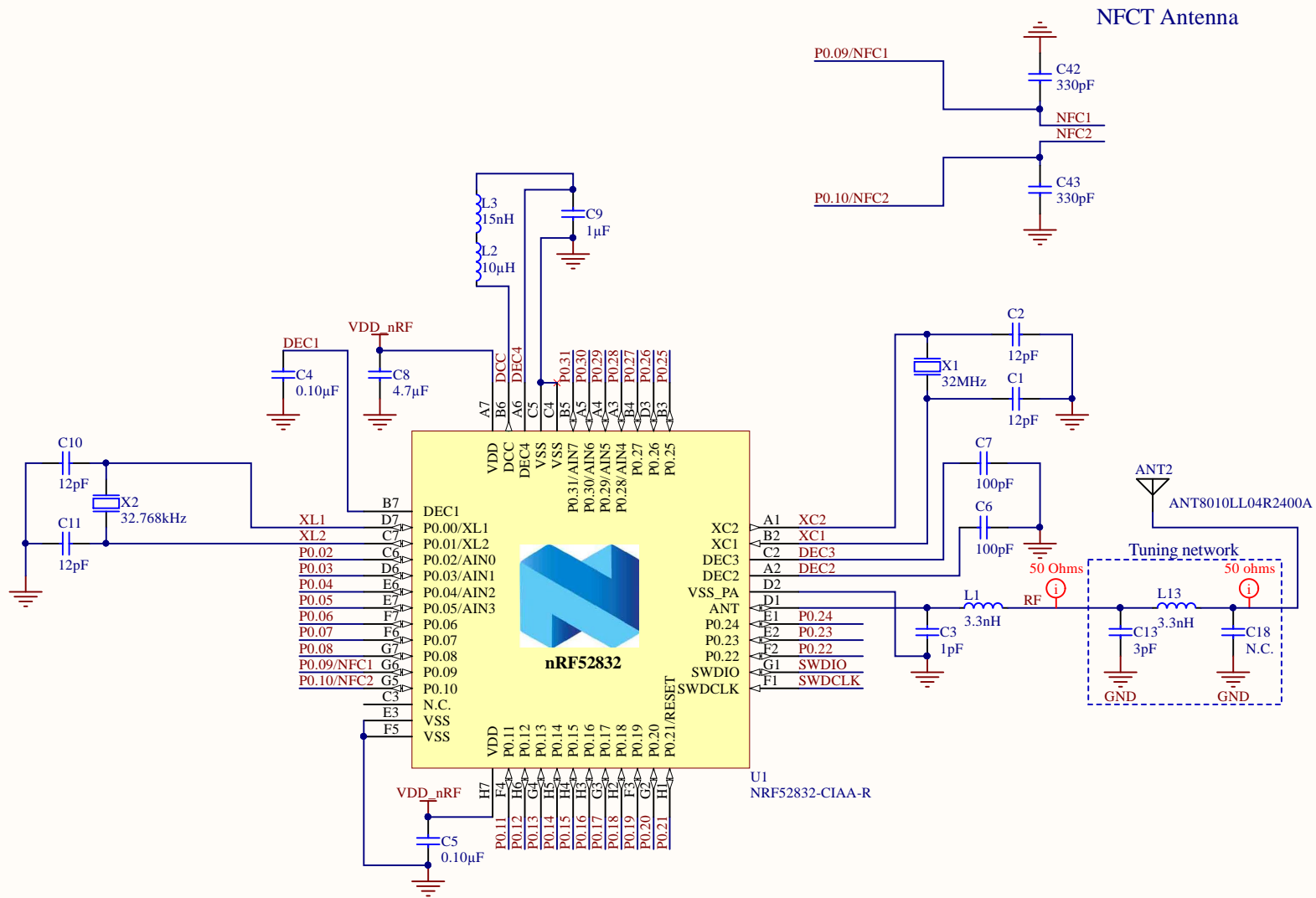
(no edge) SX1276 HF ANT SEL



P0.02	P0.02
P0.03	P0.03
P0.04	P0.04
P0.05	P0.05
P0.06	P0.06
P0.07	P0.07
P0.08	P0.08
P0.09	P0.09
P0.10	P0.10
P0.11	P0.11
P0.12	P0.12
P0.13	P0.13
P0.14	P0.14
P0.15	P0.15
P0.16	P0.16
P0.17	P0.17
P0.18	P0.18
P0.19	P0.19
P0.20	P0.20
P0.21	P0.21
P0.22	P0.22
P0.23	P0.23
P0.24	P0.24
P0.25	P0.25
P0.26	P0.26
P0.27	P0.27
P0.28	P0.28
P0.29	P0.29
P0.30	P0.30
P0.31	P0.31

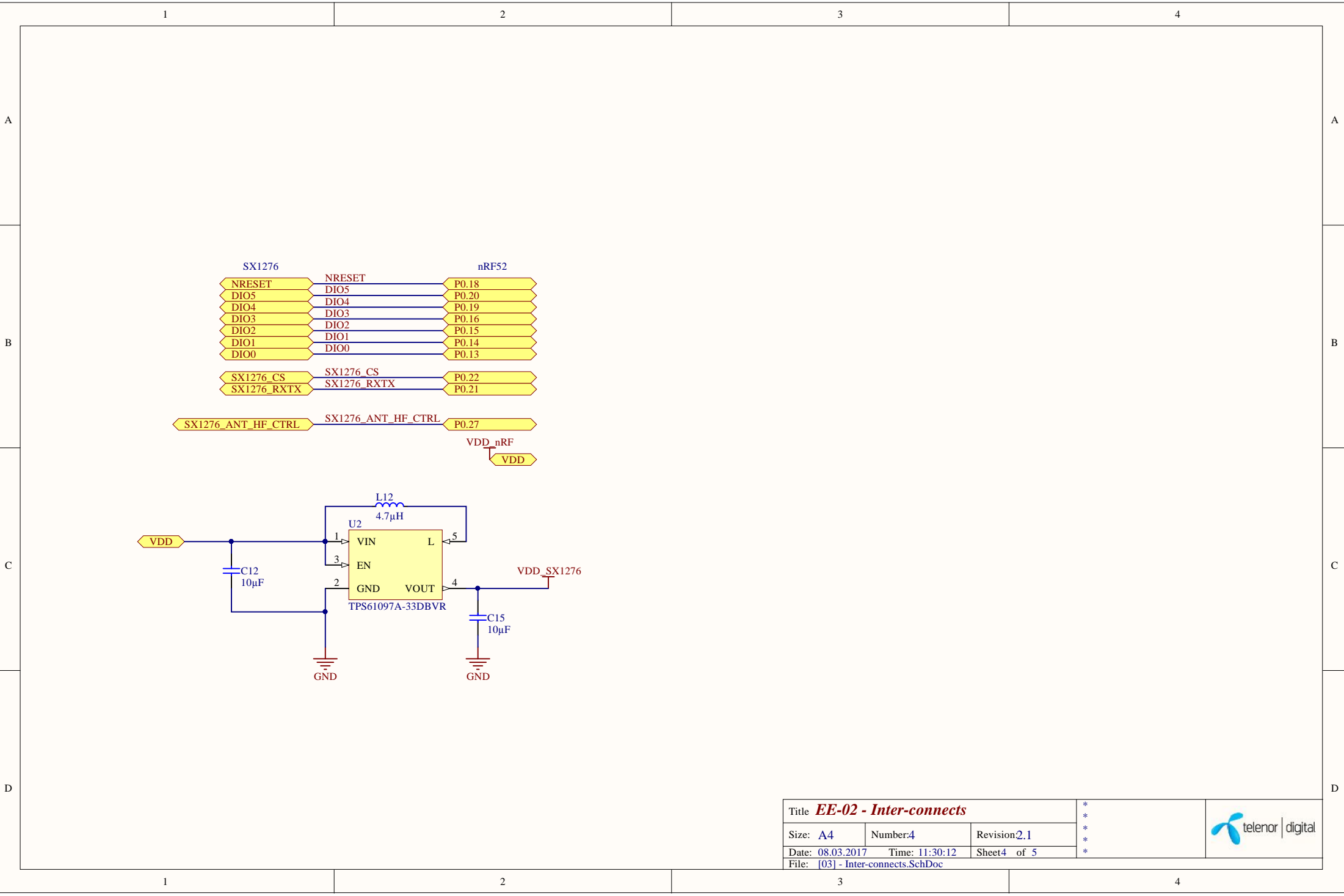
SWDIO	SWDIO
SWDCLK	SWDCLK

NFC1	NFC1
NFC2	NFC2



Title EE-02 - nRF52		
Size: A4	Number:3	Revision:2.1
Date: 08.03.2017	Time: 11:30:12	Sheet3 of 5
File: [02] - nRF52.SchDoc		





SX1276 RF Part:

