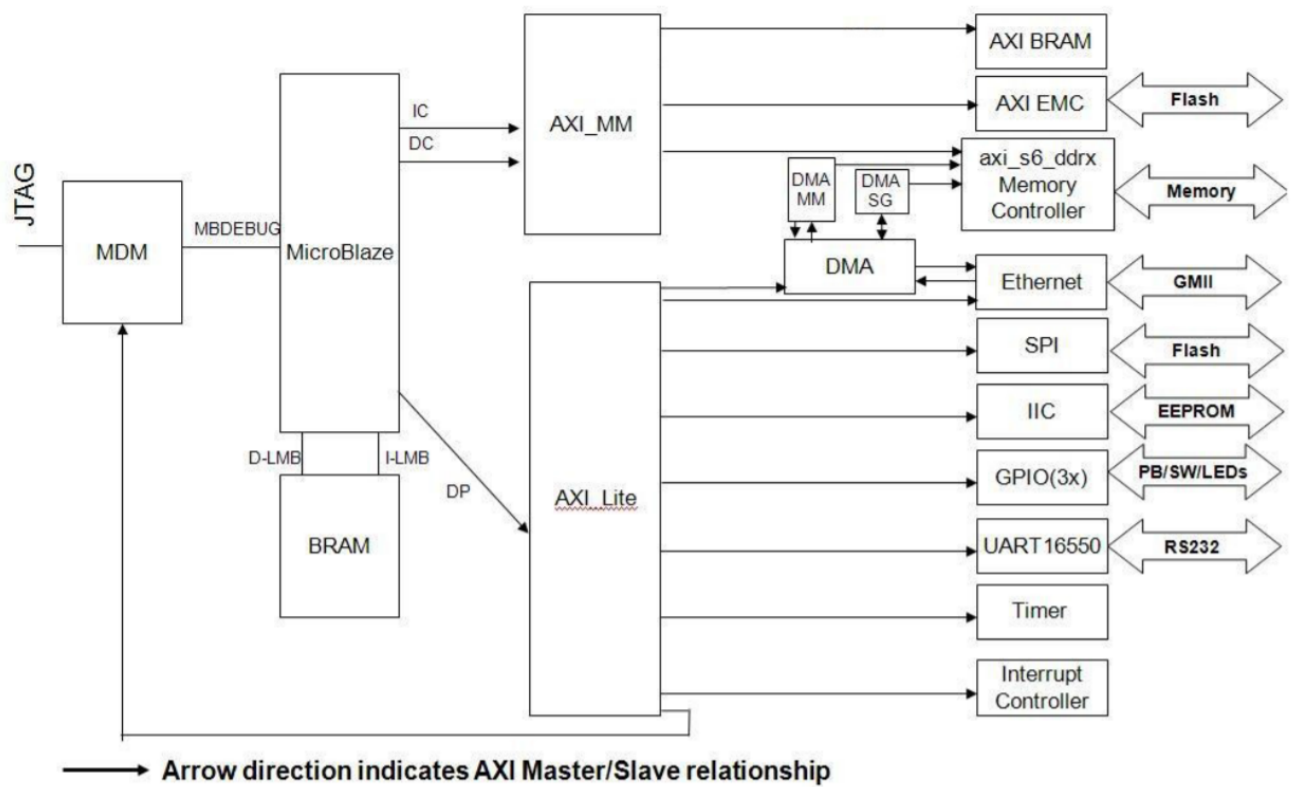
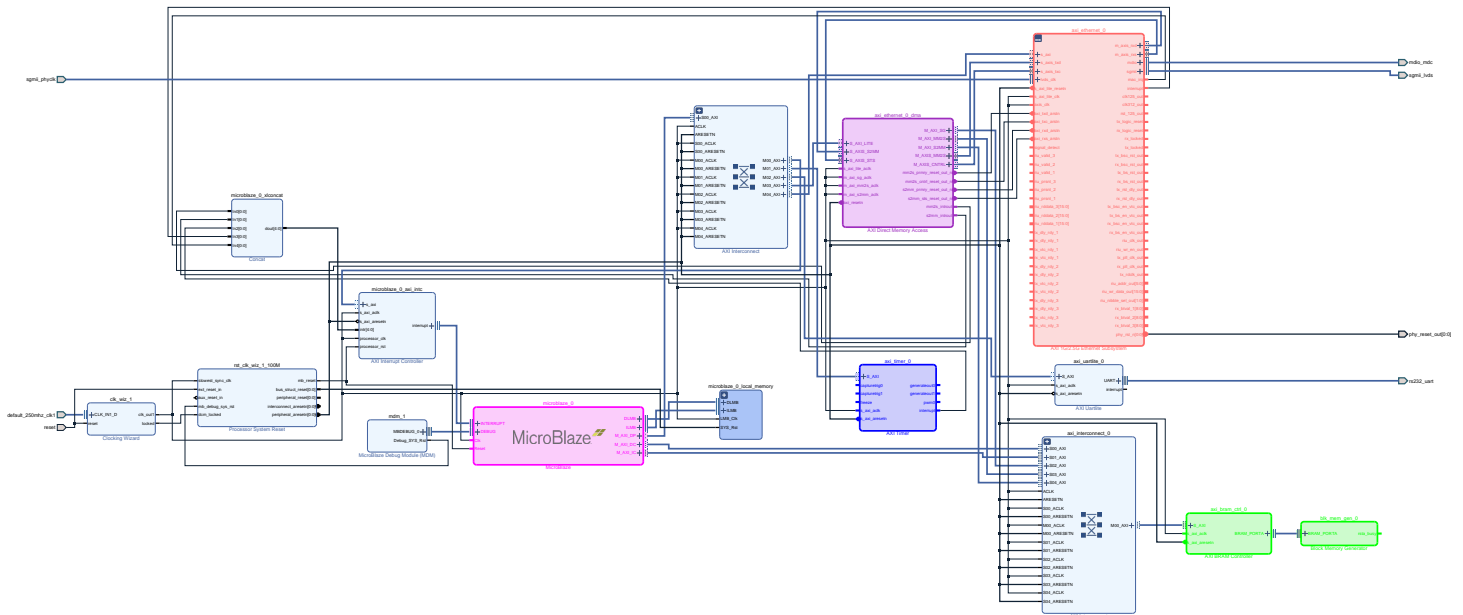


VCU118 Ethernet/lwIP Hardware Design

Block Design



Address Map

Cell	Slave Interface	Base Name	Offset Address	Range	High Address
microblaze_0					
Data (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF
axi_ethernet_0	s_axi	Reg0	0x40C0_0000	256K	0x40C3_FFFF
axi_ethernet_0_dma	S_AXI_LITE	Reg	0x41E0_0000	64K	0x41E0_FFFF
axi_timer_0	S_AXI	Reg	0x41C0_0000	64K	0x41C0_FFFF
axi_uartlite_0	S_AXI	Reg	0x4060_0000	64K	0x4060_FFFF
microblaze_0_local_memory/dlmb_bram_if_cntlr	SLMB	Mem	0x0000_0000	16K	0x0000_3FFF
microblaze_0_axi_intc	s_axi	Reg	0x4120_0000	64K	0x4120_FFFF
Instruction (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF
microblaze_0_local_memory/ilmb_bram_if_cntlr	SLMB	Mem	0x0000_0000	16K	0x0000_3FFF
axi_ethernet_0_dma					
Data_SG (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF
Data_MM2S (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF
Data_S2MM (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF

DMA Settings

AXI Direct Memory Access (7.1)

[Documentation](#) | [IP Location](#)

☐ Show disabled ports

```

+-----+
| M_AXI_SG +
| M_AXI_MM2S +
| M_AXI_S2MM +
| M_AXIS_MM2S +
| M_AXIS_CNTRL +
+-----+
+ S_AXI_LITE
+ S_AXIS_S2MM
+ S_AXIS_ST2S
- s_axi_lite_aclk mm2s_prry_reset_out_n
- m_axi_sg_aclk mm2s_cntrl_reset_out_n
- m_axi_mm2s_aclk s2mm_prry_reset_out_n
- m_axi_s2mm_aclk s2mm_sts_reset_out_n
- axi_resetn mm2s_introut
axi_dma_tstvec[31:0]
          
```

Component Name

☐ Enable Asynchronous Clocks (Auto)

☒ Enable Scatter Gather Engine

☐ Enable Micro DMA

☐ Enable Multi Channel Support

☒ Enable Control / Status Stream

Width of Buffer Length Register (8-26) bits

Address Width (32-64) bits

☒ Enable Read Channel

Number of Channels

Memory Map Data Width

Stream Data Width

Max Burst Size

☒ Allow Unaligned Transfers

☒ Enable Write Channel

Number of Channels

Memory Map Data Width

Stream Data Width (Auto)

Max Burst Size

☒ Allow Unaligned Transfers

☒ Use Rlength In Status Stream

☐ Enable Single AXI4 Data Interface

OK
Cancel

AXI 1G/2.5G Ethernet Subsystem (7.1)

Documentation IP Location

☐ Show disabled ports

Component Name	axi_ethernet_0
Board	Physical Interface MAC Features Network Timing Shared Logic OOC Settings Locations
<input checked="" type="checkbox"/> Generate Board based IO Constraints	
Associate IP interface with XILINX.COM:VCU118:PART0:2.1 Board interface	
IP Interface	Board Interface
ETHERNET	sgmii lvds
MDIO	mdio mdc
DIFFCLK	sgmii physclk
PHYRST_N	phy reset out

Re-customize IP

AXI 1G/2.5G Ethernet Subsystem (7.1)

Documentation IP Location

☐ Show disabled ports

m_axi_rst_d	+ m_axi_rst_d +
+ s_axi	m_axi_rst +
+ s_axi_bsd	mdio +
+ s_axi_btc	sgmii +
+ lrdv_clk	mac_irq
s_axi_lite_resen	interrupt
s_axi_lite_clk	clkf25_out
axi_clk	clkf12_out
axi_brd_arstn	rst_125_out
axi_btc_arstn	tx_logic_reset
axi_rst_arstn	rx_logic_reset
axi_rst_arstn	rx_locked
signal_detect	tx_locked
riu_valld_3	tx_bsc_rst_out
riu_valld_2	rx_bsc_rst_out
riu_valld_1	tx_bsc_rst_out
riu_psrnt_3	rx_bk_rst_out
riu_psrnt_2	tx_rst_dly_out
riu_psrnt_1	rx_rst_dly_out
riu_rddata_3[15:0]	tx_bsc_en_vtc_out
riu_rddata_2[15:0]	tx_bs_en_vtc_out
riu_rddata_1[15:0]	rx_bsc_en_vtc_out
tx_dly_rdy_1	rx_bs_en_vtc_out
tx_vtc_rdy_1	riu_clk_out
tx_vtc_rdy_2	riu_wer_en_out
tx_dly_rdy_2	tx_pll_clk_out
tx_dly_rdy_2	rx_pll_clk_out
tx_dly_rdy_2	tx_ddck_out
tx_vtc_rdy_2	riu_addt_out[15:0]
tx_vtc_rdy_2	riu_wer_data_out[15:0]
tx_dly_rdy_3	riu_nibble_sel_out[15:0]
tx_dly_rdy_3	rx_hlval_1[8:0]
tx_vtc_rdy_3	rx_hlval_2[8:0]
tx_vtc_rdy_3	rx_hlval_3[8:0]
	phy_rst_n[0:0]

Component Name

Board

Physical Interface

MAC Features

Network Timing

Shared Logic

OOC Settings

Locations

Ethernet Speed

☒ 1 Gbps ☐ 2.5 Gbps

Physical Interface Selection

☐ MII ☐ GMII ☐ RGMII ☒ SGMII ☐ 1000BaseX

This mode would instantiate an on-chip PHY. Data rate is 10/100/1000 Mbps for SGMII and 1G for 1000BASEX modes of operation.

Transceiver Options

LVDS Option

☒ Enable Standard I/O (LVDS) for 1000BASE-X/SGMII instead of a transceiver.

MDIO Phy Address of internal 1000BASE-X/SGMII

MDIO PHY Address [0 - 31]

Transceiver Debug

☐ Enable TransceiverControl Debug Interface

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