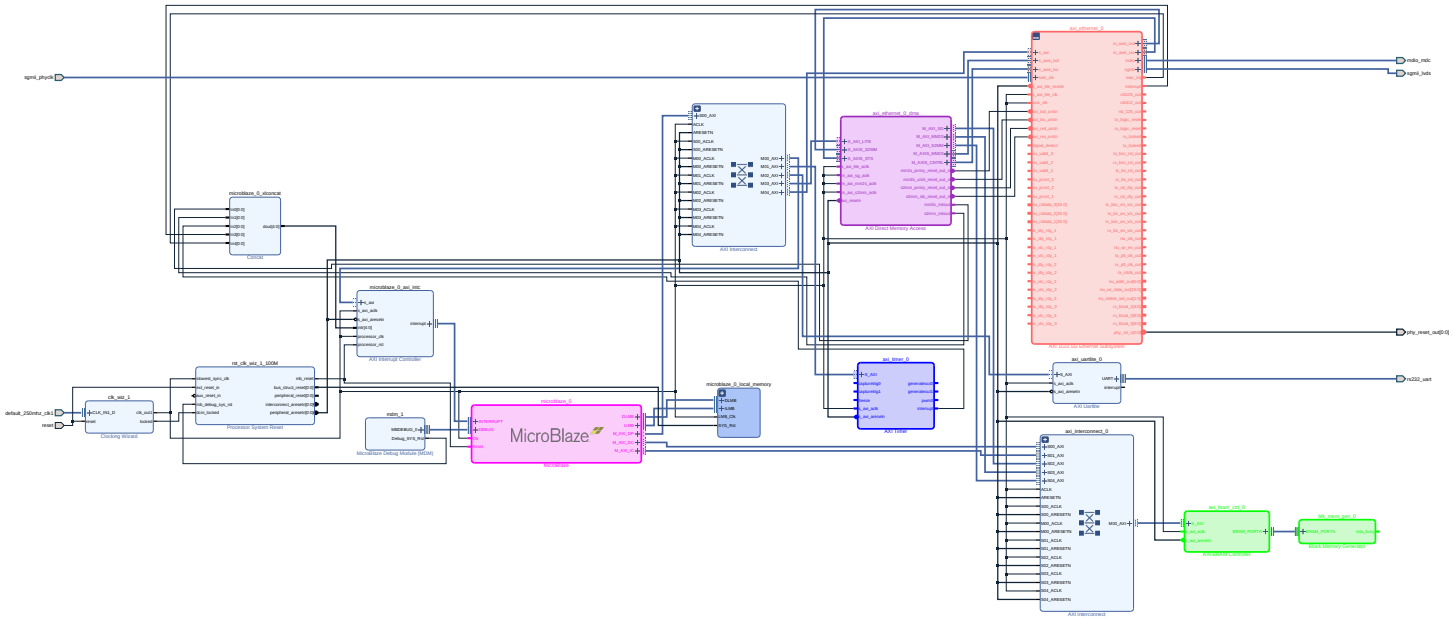
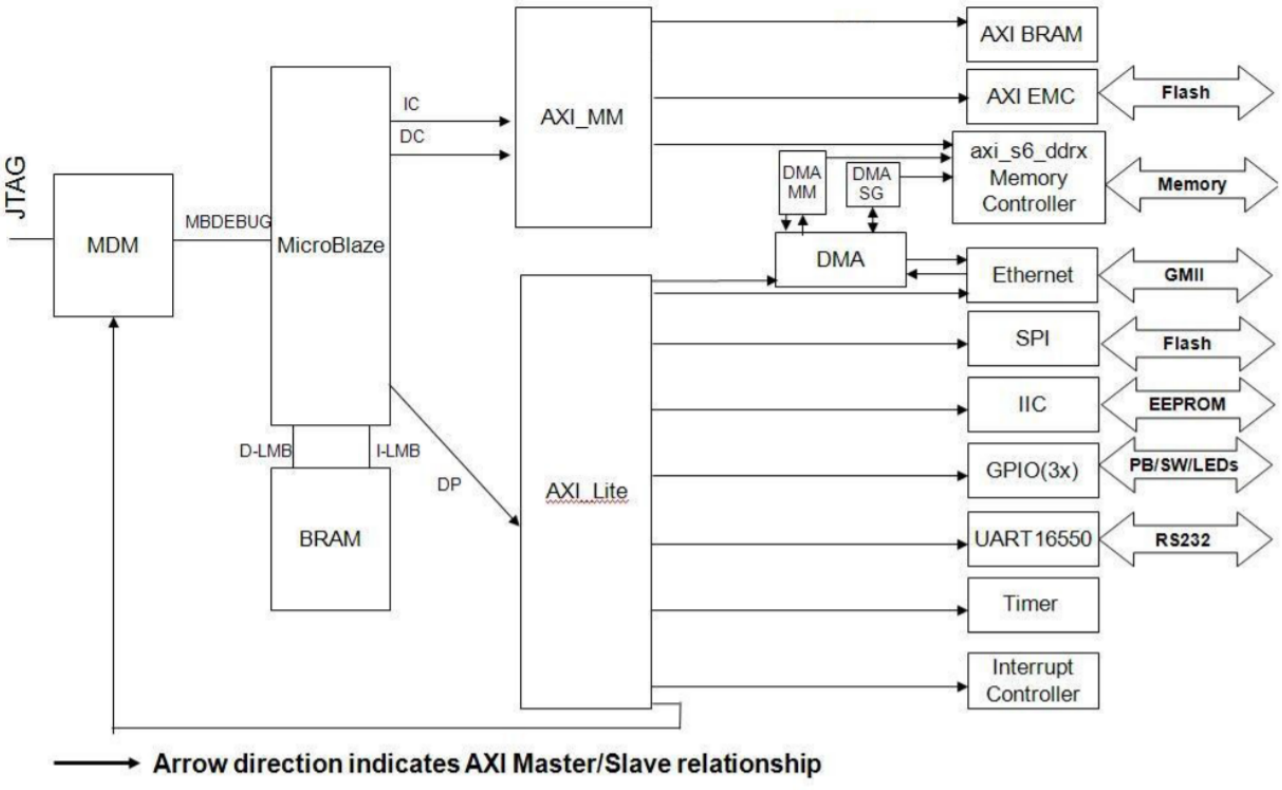
VCU118 Ethernet/lwIP Hardware Design

Block Design





Address Map

Diagram | Address Editor

Cell	Slave Interface	Base Name	Offset Address	Range	High Address
microblaze_0					
Data (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF
axi_ethernet_0	s_axi	Reg0	0x40C0_0000	256K	0x40C3_FFFF
axi_ethernet_0_dma	S_AXI_LITE	Reg	0x41E0_0000	64K	0x41E0_FFFF
axi_timer_0	S_AXI	Reg	0x41C0_0000	64K	0x41C0_FFFF
axi_uartlite_0	S_AXI	Reg	0x4060_0000	64K	0x4060_FFFF
microblaze_0_local_memory/dlmb_bram_if_cntlr	SLMB	Mem	0x0000_0000	16K	0x0000_3FFF
microblaze_0_axi_intc	s_axi	Reg	0x4120_0000	64K	0x4120_FFFF
Instruction (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF
microblaze_0_local_memory/ilmb_bram_if_cntlr	SLMB	Mem	0x0000_0000	16K	0x0000_3FFF
axi_ethernet_0_dma					
Data_SG (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF
Data_MM2S (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF
Data_S2MM (32 address bits : 4G)					
axi_bram_ctrl_0	S_AXI	Mem0	0xC000_0000	4M	0xC03F_FFFF

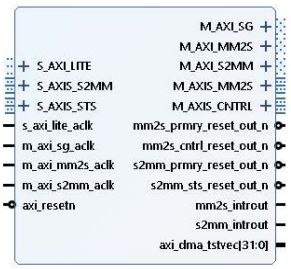
DMA Settings

Re-customize IP

AXI Direct Memory Access (7.1)

Documentation | IP Location

Show disabled ports



Component Name: axi_ethernet_0_dma

- [ ] Enable Asynchronous Clocks (Auto)
- [x] Enable Scatter Gather Engine
- [ ] Enable Micro DMA
- [ ] Enable Multi Channel Support
- [x] Enable Control / Status Stream

Width of Buffer Length Register (8-26): 16 bits

Address Width (32-64): 32 bits

Enable Read Channel		Enable Write Channel	
Number of Channels	1	Number of Channels	1
Memory Map Data Width	32	AUTO Memory Map Data Width	32
Stream Data Width	32	Stream Data Width (Auto)	32
Max Burst Size	32	Max Burst Size	32
Allow Unaligned Transfers		Allow Unaligned Transfers	
		Use Rxlength In Status Stream	

AUTO Enable Single AXI4 Data Interface

OK | Cancel

Ethernet Settings