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Lab 1: Implementation of the ARCCOS Function

The ARCCOS circuit takes an 8-bit unsigned value X and a clock signal as the inputs. The output ANGLE is a 10-bit unsigned value computed from 10*arccos(X/256) using an approximation based on the Taylor series expansion of the function. The VHDL description is shown below in Figure 1.

```
1   --
2   -- entity name: g44_ARCCOS
3   --
4   -- Version 1.0
5   -- Authors: William Zhang and Qin Xuan Xu
6   -- Date: March ??, 2023 (enter the date of the latest edit to the file)
7   library ieee; -- allows use of the std_logic_vector type
8   use ieee.std_logic_1164.all;
9   use ieee.numeric_std.all; -- needed since you are using unsigned numbers
10  entity g44_ARCCOS is
11  port ( X : in std_logic_vector(7 downto 0);
12  CLOCK : in std_logic;
13  ANGLE : out std_logic_vector(9 downto 0));
14  end g44_ARCCOS;
15
16  architecture arch of g44_ARCCOS is
17  signal X2: unsigned(15 downto 0);
18  signal P1: unsigned(31 downto 0);
19  signal S1: unsigned(8 downto 0);
20  signal P2: unsigned(24 downto 0);
21  signal S2: unsigned(10 downto 0);
22  signal P3: unsigned(18 downto 0);
23
24
25  begin
26
27     process(CLOCK)
28     begin
29        if rising_edge(CLOCK) then
30           X2 <= unsigned(X) * unsigned(X);
31           P1 <= 86 * X2;
32           S1 <= 191 + ("00" & P1(22 downto 16));
33           P2 <= S1 * X2;
34           S2 <= 1144 + ("00" & P2(24 downto 16));
35           P3 <= S2 * unsigned(X);
36           ANGLE <= std_logic_vector(900 - P3(18 downto 9));
37     end if;
38     end process;
39  end arch;
```

Figure 1: VHDL description of the ARCCOS circuit

The circuit is first tested using three specific inputs: 128, 0 and 181. The VHDL code for this test bench was given in the assignment handout. The simulation results are shown in Figure 2.

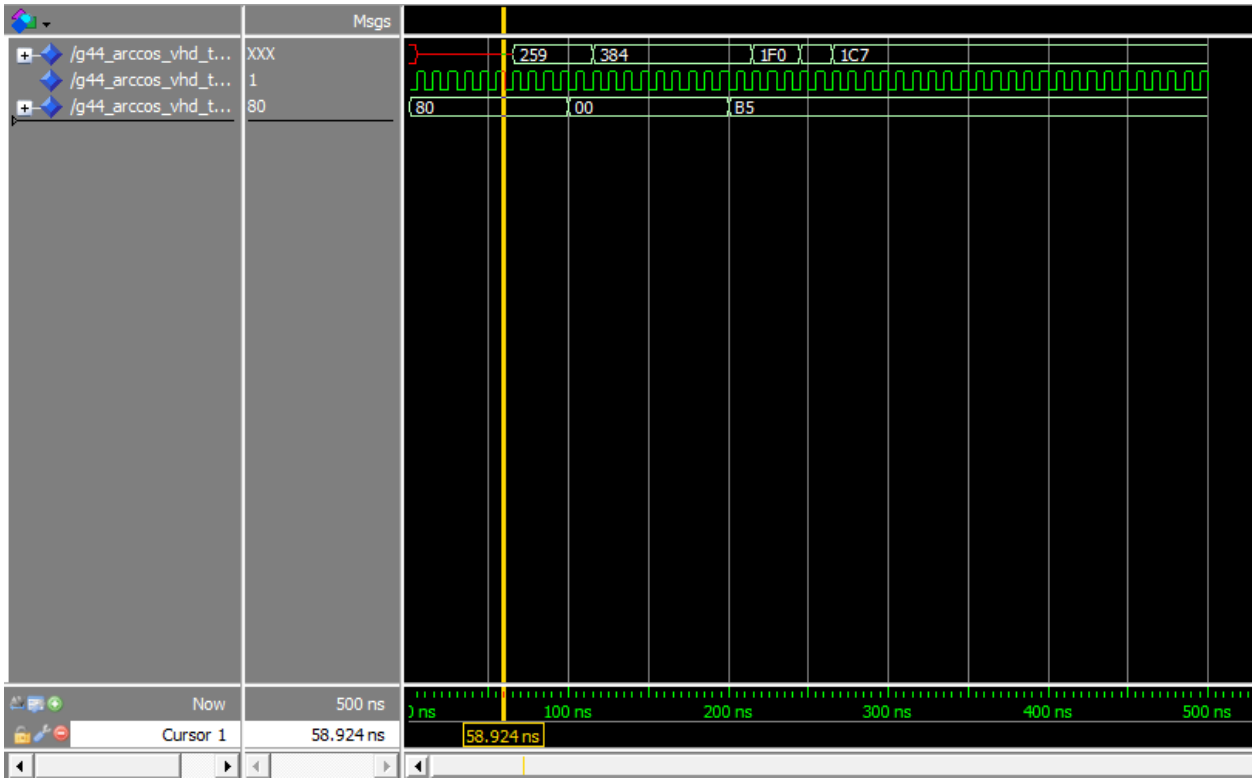

Figure 2: Simulation results of the first test

The following table compares the results of this test with the actual values. We can see that the values are fairly close.

Input X (decimal)	Result (decimal)	Expected Value (decimal)
80 (128)	259 (601)	258 (600)
0 (0)	384 (900)	384 (900)
B5 (181)	1C7 (455)	1C2 (450)

The circuit is then tested with inputs ranging from 0 to 255, which represents all the possible values that an 8-bit unsigned integer can be. The VHDL code for this test bench is shown in Figure 3.

```
23  --
24  -- Simulation tool : ModelSim-Altera (VHDL)
25  --
26
27  LIBRARY ieee;
28  USE ieee.std_logic_1164.all;
29  use ieee.numeric_std.all;
30
31  ENTITY g44_ARCCOS_vhd_tst IS
32  END g44_ARCCOS_vhd_tst;
33  ARCHITECTURE g44_ARCCOS_arch OF g44_ARCCOS_vhd_tst IS
34  -- constants
35  -- signals
36  SIGNAL ANGLE : STD_LOGIC_VECTOR(9 DOWNTO 0);
37  SIGNAL CLOCK : STD_LOGIC := '0';
38  SIGNAL X : STD_LOGIC_VECTOR(7 DOWNTO 0);
39  COMPONENT g44_ARCCOS
40      PORT (
41      ANGLE : OUT STD_LOGIC_VECTOR(9 DOWNTO 0);
42      CLOCK : IN STD_LOGIC;
43      X : IN STD_LOGIC_VECTOR(7 DOWNTO 0)
44      );
45  END COMPONENT;
46  BEGIN
47      i1 : g44_ARCCOS
48      PORT MAP (
49  -- list connections between master ports and signals
50      ANGLE => ANGLE,
51      CLOCK => CLOCK,
52      X => X
53      );
54
55
56  always : PROCESS
57  -- optional sensitivity list
58  -- (        )
59  -- variable declarations
60  BEGIN
61          -- code executes for every event on sensitivity list
62          for i in 0 to 255 loop
63              X <= std_logic_vector(to_unsigned(i,8));
64              wait for 8 ns;
65          end loop;
66
67          WAIT;
68  END PROCESS always;
69
70  clock2: PROCESS
71  BEGIN
72          wait for 4 ns;
73          CLOCK <= not CLOCK;
74
75  END PROCESS clock2;
76  END g44_ARCCOS_arch;
77
```

Figure 3: Testbench for the ARCCOS circuit

The simulation results for the first 500 ns of this test are shown in Figure 4.

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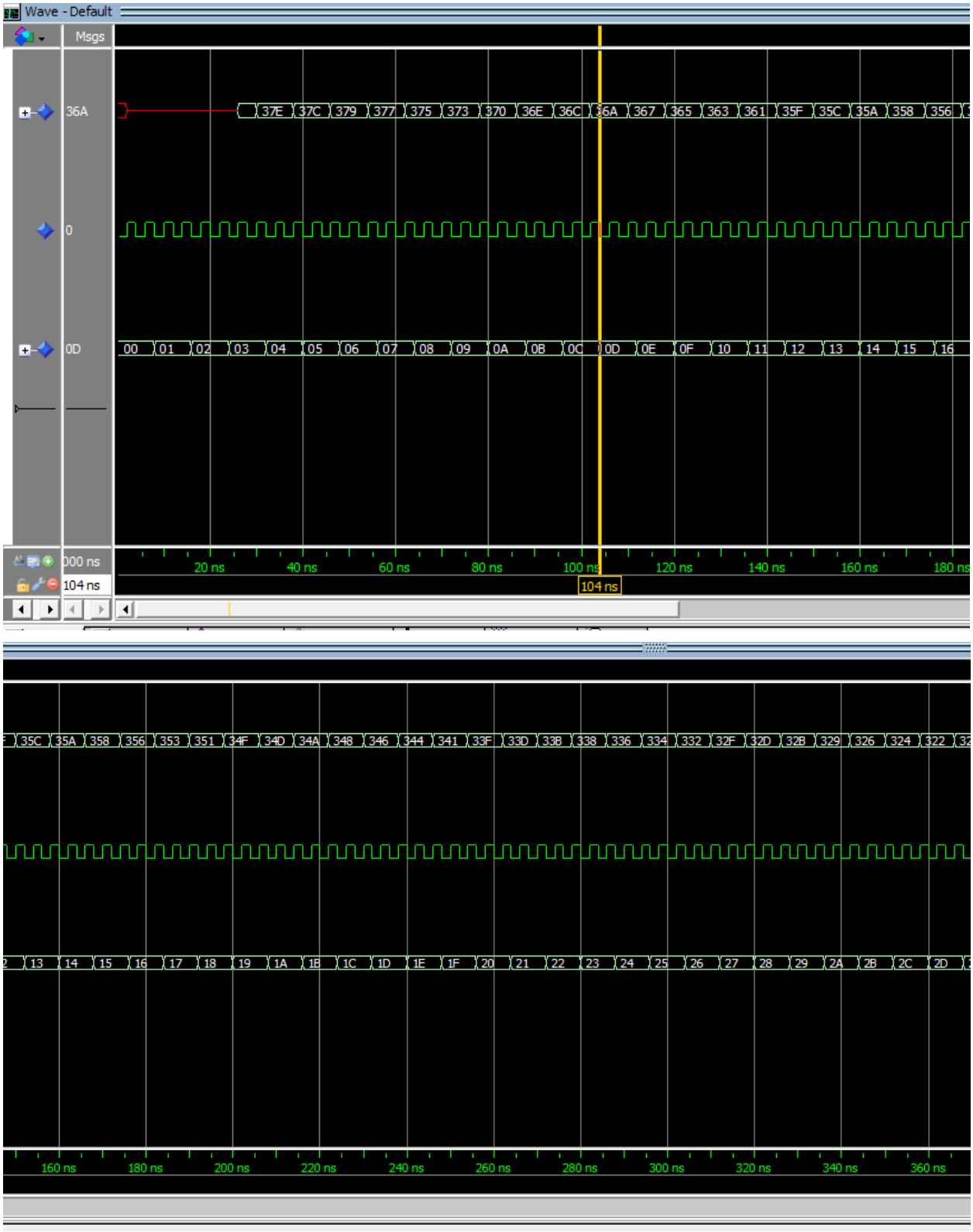

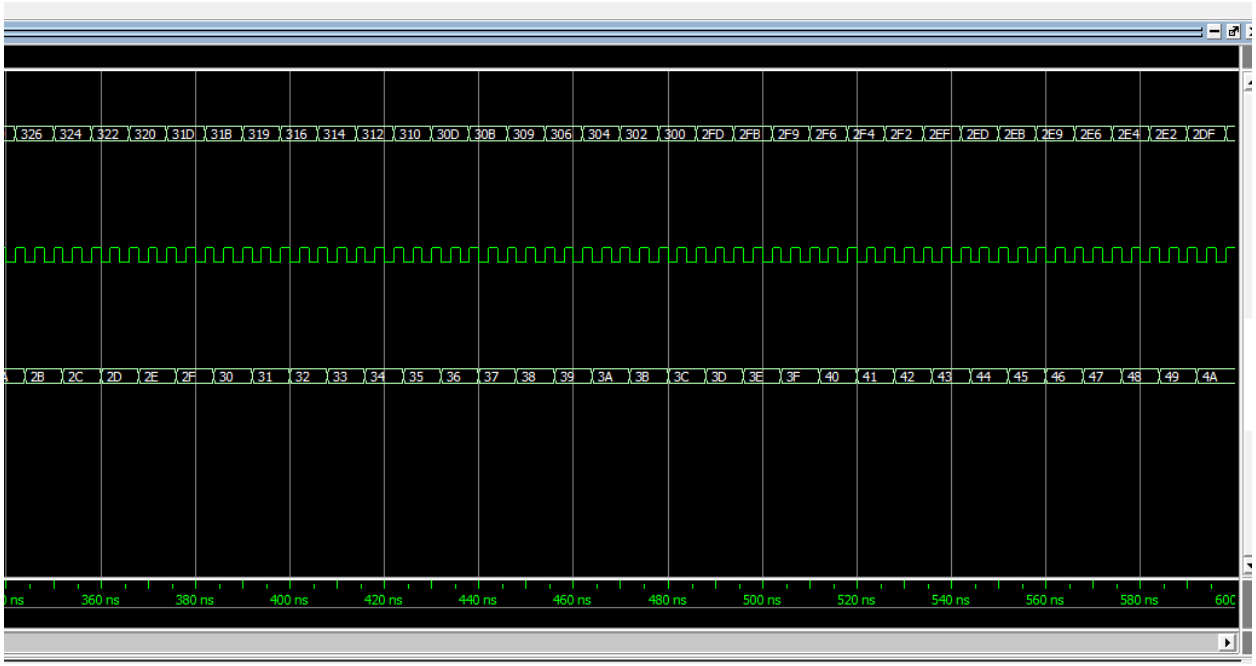

Figure 4: Simulation results for the second test

The following table compares the results of this test with the actual values. We can see that the values are fairly close for smaller values of X, and this difference gets bigger as X gets larger.

Input X (decimal)	Result (decimal)	Expected Value (decimal)
1	384 (900)	384 (900)
80 (128)	259 (601)	258 (600)
B5 (181)	1C7 (455)	1C2 (450)
E6 (230)	127 (295)	104 (260)

Figure 5 shows the content of the sdc file that was used. We found that the clock period of 4 passes the timing analysis.

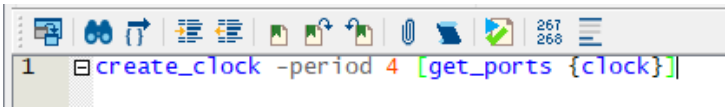

Figure 5: Content of g44_ARCCOS.sdc

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The following values of the timing analysis were reported.

Requested Fmax = 250 MHz
Fast 1100mV 0C Model Hold Slack Value = 0.232
Slow 1100 mV 85C Model Setup Slack Value = 0.469
Slow 1100 mV 85C Model Fmax = 283.21 MHz
"No paths fail setup timing."
The worst-case slack is 0.426 ns.
Logic utilization: 14/32070

Chip Planner: