Extensible Homebrew Computer System Architecture Whitepaper

Detailed System Manual

2024. 9. 29.

Revision

License Information

All files in this project archive (or repository) excluding documents which specifies any other license in its header or “LICENSE” file of its parent directory follow BSD-2-Clause, except for the that the font data of documentations using template which is used in this documentation: The contents of this repository do not warrant its proper operation, and does not warrant its correct documentation. Reading this document, it is recommended to check its desired operation from code or binary files on your own.

Trademarks

* IBM-PC is a registered trademark of International Business Corporation.
* Macintosh is a trademark of Apple Inc.
* UNIX is a registered trademark of AT&T.
* FLEX, MAX, and Altera is a registered trademark of Altera Corp. acquired by Intel Corp.
* AVR is a registered trademark of Atmel Corp. acquired by Microchip Technology Inc.

BSD-2-Clause LICENSE

Copyright 2024

Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met:

1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer.

2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution.

THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS “AS IS” AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT HOLDER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Before You Read This Document…

This document is detailed system manual of the homebrew computer powered by Motorola MC68030 Microprocessor. Its coverage is from low-level hardware structures and electrical characteristics to firmware operation calls to create your own bootloader and operating system or port existing applications or operating systems to this architecture.

Due to the educational purpose of this system architecture, you can freely create, modify, and delete any contents of it without almost every limitation. To read detailed information, see the license text inside of a box in the previous page.

Contacts

You can visit <https://github.com/kms1212/68k30-hbc> to create an issue to this repository.

Related Documents

More detailed informations of each components/standard used in this architecture may be needed to comprehend their operation, referencing documents in following table is recommended.

|  |  |
| --- | --- |
| Title | Contents |
| MC68030 User’s Manual | Detailed description of MC68030 Microprocessor |
| MC68882 User’s Manual | Detailed description of MC68882 Floating-point coprocessor |
| FLEX® 6000 PLD Family Datasheet | Electrical characteristics, device architecture, timing parameters, etc. of Altera® FLEX® 6000 FPGA Family |
| MAX® 7000 PLD Family Datasheet | Electrical characteristics, device architecture, ISP programming methods, timing parameters, etc. of Altera® MAX® 7000 CPLD Family |
| Altera® Configuration Handbook | Configuration methods for Altera® FPGA Families. |
| JEDEC Standard No.21-C Page 4.4.2 | Description of JEDEC 72-pin SIMM Memory module standard. |
| 030HBC Software Development Supplement Manual | Considerations and detailed information regarding software (Bootloader/OS/Application) development (TBD) |
| TBD |  |

Most of these documents will be archived into a single site soon.

Note that this list of related documents can be updated without noticing.

Notes and Warnings

Warning

Contents described inside this box are warnings about the factors which can cause misoperation of the system.

Note

Contents described inside this box can be an useful trick and shortcut to utilize this documentation.

Table of Contents

[Chapter 1. Overview 8](#_Toc178495579)

[1.1 Features 9](#_Toc178495580)

[1.2 System Performance 9](#_Toc178495581)

[Chapter 2. Processor & Coprocessor 13](#_Toc178495582)

[2.1 The Main Processor 14](#_Toc178495583)

[2.2 The Coprocessor 15](#_Toc178495584)

[Chapter 3. Memory Subsystem 16](#_Toc178495585)

[3.1 System Memory Map 17](#_Toc178495586)

[3.1.1 Boot Vector 17](#_Toc178495587)

[3.1.2 System Memory 17](#_Toc178495588)

[3.1.3 Boot Firmware Area 17](#_Toc178495589)

[3.1.4 ISA Areas 17](#_Toc178495590)

[3.1.5 MMIO Area 17](#_Toc178495591)

[3.2 Dynamic RAM Modules 18](#_Toc178495592)

[3.3 Memory-Mapped I/O 19](#_Toc178495593)

[3.4 Direct Memory Access 20](#_Toc178495594)

[Chapter 4. System Controller Unit 21](#_Toc178495595)

[4.1 Register Description 22](#_Toc178495596)

[4.1.1 Register 00h: CPU Configuration Register 22](#_Toc178495597)

[4.1.2 Register 01h: DRAM Configuration Register 22](#_Toc178495598)

[4.1.3 Register 02h: Firmware ROM Configuration Register 23](#_Toc178495599)

[4.1.4 Register 03h: Power Management Configuration Register 23](#_Toc178495600)

[4.1.5 Registers 04h-05h: IDE Bus Controller Configuration Register 0-1 24](#_Toc178495601)

[4.1.6 Register 06h: ISA Bus Controller Configuration Register 24](#_Toc178495602)

[4.1.7 Registers 08h-0Fh: DRAM Address Boundary Register 0-7 25](#_Toc178495603)

[Chapter 5. System Bus 27](#_Toc178495604)

[Chapter 6. Bootstrap Firmware 28](#_Toc178495605)

[6.1 Firmware System Calls 29](#_Toc178495606)

[6.1.1 Category 0000h: Boot Services 29](#_Toc178495607)

[6.1.2 Category 0001h: Async I/O Services 29](#_Toc178495608)

[6.1.3 Category 0002h: Video Services 30](#_Toc178495609)

[6.1.4 Category 0003h: Keyboard / Pointing Device Services 31](#_Toc178495610)

[6.1.5 Category 0004h: Storage Devices 32](#_Toc178495611)

[6.1.6 Category FFFFh: Miscellaneous Features 33](#_Toc178495612)

[Chapter 7. External Interfaces 35](#_Toc178495613)

[Chapter 8. Power Supply 36](#_Toc178495614)

[Chapter 9. System Initialization 37](#_Toc178495615)

[Chapter 10. Debugging Interfaces 38](#_Toc178495616)

[Appendix A. Brief Description of System Controller FPGA IP 39](#_Toc178495617)

[A.1 Appendix Heading 2 39](#_Toc178495618)

[A.1.1 Appendix Heading 3 39](#_Toc178495619)

Figures

[Figure 1‑1 System Block Diagram 7](#_Toc176764799)

[Figure 3‑1 System Memory Map 16](#_Toc176764800)

Tables

**No table of figures entries found.**

# Overview

SCSI Devices

(Daisy-chained)

System Board

External Devices

LAN Connection

Monitor

External

Speaker

SCSI Adapter

Network Adapter

IBM VGA

Compatible

3x 16-bit ISA Expansion Slots

ATA/ATAPI-Compliant Drives

Internal 5¼” or 3½” Diskette Drives

IDE Port

IRQC

FDD Controller

Audio Controller

RTC

2x RS232

Keyboard & Mouse

OSC

CNTL

MC68030 CPU

&

MC68882 FPU

72P

SIMM

72P

SIMM

72P

SIMM

72P

SIMM

4CH

32BIT

DMA

Power Supply

ATX Compatible

Figure 1‑1 System Block Diagram

Contents in this chapter roughly explains about the entire architecture of the `030 Extensible Homebrew Computer. The architecture of this system is designed to provide flexible operations, rich system functions, and large expansion capabilities.

## Features

The features and characteristics of the `030 Extensible Homebrew Computer (hereafter ‘030EHBC’) are listed as follows:

* Powered by a Motorola MC68030 microprocessor and a MC68882 coprocessor
  + 32-bit microprocessor up to 50 MHz of operation clock
  + Integrated 256-byte data cache and 256-byte instruction cache
  + Paged Memory-Management Unit (MMU) integrated for memory protection
  + 7 levels of interrupt autovector
  + A MC68882 floating-point coprocessor which accelerates real-number arithmetic is installable
* Configurable processor frequency up to 50MHz and two fixed clocks at 24MHz and at 14.61818MHz
* Four 72-pin SIMMs for DRAM capacity up to 128MiB
* A System Controller Unit (SCU) implemented on FPGA
  + Configurable CPU clock
  + CPU Burst Cache Fill operation
  + DRAM controller
  + IDE/ISA Bus controller
  + Power management features
* 4 DMA channels
* Full support of IRQ signals driven by ISA bus devices
* 8 programmable timers including refresh counter
* Rich capabilities of peripheral buses and external devices:
  + 1 floppy drive interface
  + 1 USB host interface
  + PS/2 keyboard and mouse interface
  + 1 RS232 serial port
  + 1 10Base-T 10Mbps ethernet port
  + Speaker/Microphone/Line-in audio jack
  + I2C, SPI
* 3 sets of 16-bit ISA card-edge connector
* Coin cell battery backup for a RTC and a NVSRAM
* 1MiB Flash Memory for Firmware
* A 24-pin ATX power supply connector for power inputs

## System Performance

Default

Bold

Italic

Bold Italic

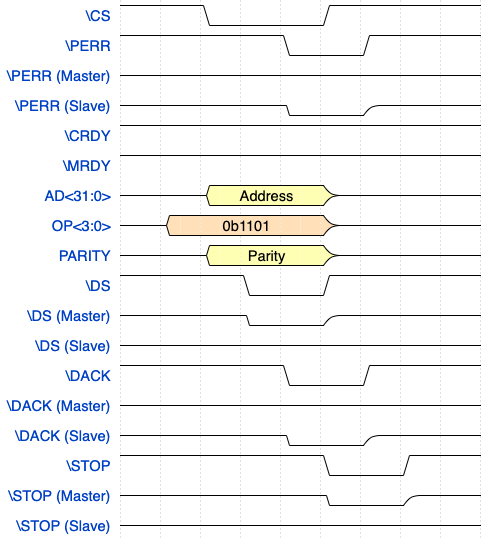
Monospaced

Bold Monospaced

|  |  |
| --- | --- |
| Field | Description |
| Data | Data |
| Data | Data |
| Data | Data |
| Data | Data |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Offset | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0000h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0010h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0020h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0030h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0040h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0050h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0060h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Code



Footnote[[1]](#footnote-1)

* Item1
* Item2
* Item3
* Item4
* Item5
* Item6
* Item7
* Item8
* Item9
* Item10
  + Subitem1
  + Subitem2
  + Subitem3

Note

Note Content

1. Item1
2. Item2
3. Item3
4. Item4
5. Item5
6. Item6
7. Item7
   1. Subitem1
   2. Subitem2
   3. Subitem3

Warning

Warning Content

# Processor & Coprocessor

## The Main Processor

## The Coprocessor

# Memory Subsystem

Figure 3‑1 System Memory Map

## System Memory Map

|  |  |  |
| --- | --- | --- |
| FFFFFFFF |  | MMIO Area |
| FF000000 |
| FEFFFFFF |  | ISA SMEM Area |
| FE100000 |
| FE0FFFFF |  | ISA MEM Area |
| FE000400 |
| FE0003FE |  | ISA I/O Area |
| FE000000 |
| FDFFFFFF |  | Boot Firmware Area  (Max. 16 MiB) |
| FD000000 |
| FCFFFFFF |  | Reserved |
| FC000000 |
| FBFFFFFF |  | System Memory  (Max. 4,032 MiB) |
| 00000008 |
| 00000007 |  | Boot Vector or System Memory |
| 00000000 |

### Boot Vector

### System Memory

### Boot Firmware Area

### ISA Areas

### MMIO Area

## Dynamic RAM Modules

## Memory-Mapped I/O

## Direct Memory Access

# System Controller Unit

## Register Description

### Register 00h: CPU Configuration Register

Default Value: 00h

Operation: Read / Write

Bit 7 Force CPU Clock to 8MHz

0 Enable

1 Disable

Bits 6-4 CPU Clock

000 33.33MHz

001 80MHz

010 66.67MHz

011 50MHz

100 40MHz

101 60MHz

110 25MHz

111 20MHz

Bits 3-2 Reserved

Bit 1 Disable Boot Interrupt Vector

0 Enable

1 Disable

Bit 0 Enable CPU Burst Operation

0 Disable

1 Enable

### Register 01h: DRAM Configuration Register

Default Value: 00h

Operation: Read / Write

Bit 7 Reserved

Bits 6-4 Address Mapping Mode

000 Mapping mode 0

001 Mapping mode 1

010 Mapping mode 2

011 Reserved

100 Mapping mode 4

101 Mapping mode 5

110 Mapping mode 6

111 Reserved

Bit 3 RAS to CAS Delay

0 3 CPU clocks

1 2 CPU clocks

Bit 2 Reserved

Bit 1 Write Cycle CAS Pulse Width

0 2 CPU clocks

1 1 CPU clock

Bit 0 RAS Precharge Time

0 2 CPU clocks

1 1 CPU clock

### Register 02h: Firmware ROM Configuration Register

Default Value: 00h

Operation: Read / Write

Bits 7-3 Reserved

Bits 2-0 ROM Latency

000 8 CPU clocks

001 1 CPU clock

010 2 CPU clocks

011 3 CPU clocks

100 4 CPU clocks

101 5 CPU clocks

110 6 CPU clocks

111 7 CPU clocks

### Register 03h: Power Management Configuration Register

Default Value: 00h

Operation: Read / Write

Bit 7 Power Off System (Read: ‘0’)

0 No operation

1 Power off system immediately

Bit 6 Reset NMI Status (Read: ‘0’)

0 No operation

1 Reset NMI raised by power switch if the switch is not pressed

Bits 5-2 Reserved

Bit 1 Power Switch Operation

0 Power off system immediately

1 Raise NMI

Bit 0 Power Switch Status (Read Only)

0 Not pressed

1 Pressed

### Registers 04h-05h: IDE Bus Controller Configuration Register 0-1

#### Register 04h

Default Value: 00h

Operation: Read / Write

Bit 7 Enable IDE Controller

Bits 3-0 Command Delay Time

0000 16 CPU clocks

0001 1 CPU clock

0010 2 CPU clocks

0011 3 CPU clocks

0100 4 CPU clocks

0101 5 CPU clocks

0110 6 CPU clocks

0111 7 CPU clocks

1000 8 CPU clocks

1001 9 CPU clocks

1010 10 CPU clocks

1011 11 CPU clocks

1100 12 CPU clocks

1101 13 CPU clocks

1110 14 CPU clocks

1111 15 CPU clocks

#### Register 05h

Default Value: 00h

Operation: Read / Write

Bits 7-4 8-Bit Transfer Wait States

Bits 3-0 16-Bit Transfer Wait States

### Register 06h: ISA Bus Controller Configuration Register

Default Value: 00h

Operation: Read / Write

Bits 7-6 16-bit I/O Command Delay

00 5 BUSCLK

01 2 BUSCLK

10 3 BUSCLK

11 4 BUSCLK

Bits 5-4 8-bit I/O Command Delay

Bit 3 Reserved

Bit 2 Enable ISA Bus Region

0 Disable

1 Enable

Bit 1 16-bit I/O Wait States

0 2 wait state

1 1 wait states

Bit 0 8-bit I/O Wait States

0 5 wait states

1 4 wait states

### Registers 08h-0Fh: DRAM Address Boundary Register 0-7

Default Value: 00h

Operation: Read / Write

Bit 7 Reserved

Bit 6-4 Bank Boundary 1

Bit 3 Reserved

Bit 2-0 Bank Boundary 0

000 128kiB

001 256kiB

010 512kiB

011 1MiB

100 2MiB

101 4MiB

110 8MiB

111 16MiB

# System Bus

# Bootstrap Firmware

## Firmware System Calls

### Category 0000h: Boot Services

#### Function 0000h: Try to boot from next device

#### Function 0001h: Deinitialize firmware and hide ROM from address space

Return

D0 Deinitialization error code

### Category 0001h: Async I/O Services

Asynchronous input / output services for Serial port, Line printer, etc.

#### Function 0000h: Initialize Port

Parameters

D1(31:20) Baud Rate

0h 75 baud

1h 110 baud

2h 135 baud

3h 150 baud

4h 300 baud

5h 600 baud

6h 1200 baud

Ah 1800 baud

7h 2000 baud

8h 2400 baud

9h 4800 baud

Bh 9600 baud

Ch 19200 baud

Dh-Fh Reserved

D1(19) Break

0 No break

1 Break

D1(18:16) Parity Mode

0xx No parity

100 Odd

101 Even

110 Stick parity odd

111 Stick parity even

D1(15:14) Stop Bit

00 1 stop bit

01 1.5 stop bits

10 2 stop bits

11 2 stop bits if word length is 6, 7, or 8 otherwise 1.5 stop bits

D1(13:12) Word Length

00 5 bits

01 6 bits

10 7 bits

11 8 bits

D1(7:0) Port Identifier

Return

D0(31:16) Port Status

D0(15:0) Error Code

#### Function 0002h: Wait and Transmit Character

Parameters

D1(15:8) Character to send

D1(7:0) Port Identifier

Return

D0(31:16) Port Status

D0(15:0) Error Code

#### Function 0003h: Transmit Character

Parameters

D1(15:8) Character to send

D1(7:0) Port Identifier

Return

D0(31:16) Port Status

D0(15:0) Error Code

#### Function 0004h: Wait and Receive Character

Parameters

D1(7:0) Port Identifier

Return

D0(31:16) Port Status

D0(15:0) Error Code

D1 Received Character

#### Function 0005h: Wait and Receive Character

Parameters

D1(7:0) Port Identifier

Return

D0(31:16) Port Status

D0(15:0) Error Code

D1 Received Character

#### Function 0006h: Read Status

Parameters

D1(7:0) Port Identifier

Return

D0(31:16) Port Status

D0(15:0) Error Code

### Category 0002h: Video Services

#### Function 0000h: Set Video Mode

Parameters

D1(15:0) Video mode

Return

A0 Video Mode Paramter Table pointer when success, 0 when fail

#### Function 0001h: Get Video Mode Parameters

Parameters

D1(15:0) Video Mode

Return

A0 Video Mode Paramter Table pointer when success, 0 when fail

#### Function 0002h: Get Video Adapter Status

Return

D0(15:0) Current Video Mode

A0 Video Mode Paramter Table pointer

#### Function 0003h: Set Text Cursor Shape

Parameters

D1(15:8) Scan Row Start

D1(7:0) Scan Row End

#### Function 0004h: Set Text Cursor Position

Parameters

D1(15:8) Row

D1(7:0) Column

#### Function 0005h: Get Text Cursor Position and Shape

Return

D0(31:24) Cursor Scan Row Start

D0(23:16) Cursor Scan Row End

D0(15:8) Row

D0(7:0) Column

#### Function 0006h: Scroll Text Area

Parameters

D1(15:0) Lines to scroll (scroll up if positive, scroll down if negative, clear if 0)

D2 Text Color Attribute

D3(31:24) Upper Row Index

D3(23:16) Lower Row Index

D3(15:8) Left Column Index

D3(7:0) Right Column Index

#### Function 0007h: Read Character and Attribute at Cursor Position

Return

D0(15:8) Attribute

D0(7:0) Character

#### Function 0008h: Write Character and Attribute at Cursor Position

Parameters

D1(15:8) Attribute

D1(7:0) Character

#### Function 0009h: Write String

Parameters

D1(15:0) String Length

D2(9) String contains attribute

D2(8) Update Cursor

D2(7:0) Attribute

A0 String Pointer

#### Function 000Ah: Write ANSI Teletype String

Parameters

D1(15:0) String Length

A0 String Pointer

#### Function 000Bh: Set Text Font Data

Parameters

A0 Glyph data pointer

#### Function 000Ch: Set Palette

Parameters

D1(15:0) Palette size in 3-byte unit

A0 Palette pointer

### Category 0003h: Keyboard / Pointing Device Services

#### Function 0000h: Wait and Get Keyboard Stroke

Return

D0(31:24) Device Identifier

D0(7:0) ASCII Character

#### Function 0001h: Get Keyboard Stroke

Return

D0(31:24) Device Identifier

D0(7:0) ASCII Character

#### Function 0003h: Check Keyboard Status

Parameters

D1(7:0) Device Identifier

Return

D0(11) Insert active

D0(10) CapsLock active

D0(9) NumLock active

D0(8) ScrollLock active

D0(7) Left Alt pressed

D0(6) Right Alt pressed

D0(5) Left Ctrl pressed

D0(4) Right Ctrl pressed

D0(3) Left Meta pressed

D0(2) Right Meta pressed

D0(1) Left Shift pressed

D0(0) Right Shift pressed

#### Function 0004h: Flush Keyboard Buffer

#### Function 0006h: Set Mouse Parameter

#### Function 0005h: Get Mouse Status

#### Function 0007h: Get Mouse Movement

### Category 0004h: Storage Devices

#### Function 0000h: Reset Storage System

Parameters

D1(7:0) Drive Identifier

#### Function 0001h: Get Drive Status

Parameters

D1(7:0) Drive Identifier

Return

D0(31:0) Drive Status

#### Function 0002h: Get Drive Parameters

Parameters

D1(7:0) Drive Identifier

Return

A0 Drive Parameter Table Pointer

#### Function 0003h: Read Sectors CHS

Parameters

D1(31:24) Drive Identifier

D1(23:16) Head

D1(15:6) Cylinder

D1(5:0) Sector

D2(7:0) Sectors to Read

A0 Buffer Pointer

Return

D0(31:0) Drive Status

D1 Sectors Read

#### Function 0004h: Write Sectors CHS

Parameters

D1(31:24) Drive Identifier

D1(23:16) Head

D1(15:6) Cylinder

D1(5:0) Sector

D2(7:0) Sectors to Write

A0 Buffer Pointer

Return

D0(31:0) Drive Status

D1 Sectors Written

#### Function 0005h: Verify Sectors CHS

Parameters

D1(31:24) Drive Identifier

D1(23:16) Head

D1(15:6) Cylinder

D1(5:0) Sector

D2(7:0) Sectors to Verify

A0 Buffer Pointer

Return

D0(31:0) Drive Status

D1 Sectors Verified

#### Function 0006h: Read Sectors LBA

Parameters

D1(31:24) Drive Identifier

D1(23:16) Sectors to Read

D1(15:6) LBA(47:32)

D2 LBA(31:0)

A0 Buffer Pointer

Return

D0(31:0) Drive Status

D1 Sectors Read

#### Function 0007h: Write Sectors LBA

Parameters

D1(31:24) Drive Identifier

D1(23:16) Sectors to Write

D1(15:6) LBA(47:32)

D2 LBA(31:0)

A0 Buffer Pointer

Return

D0(31:0) Drive Status

D1 Sectors Written

### Category FFFFh: Miscellaneous Features

#### Function 0000h: Power Off System

#### Function 0001h: Get Device Tree

Return

A0 Device Tree Pointer

#### Function 0002h: Get System Memory Map Table

Return

A0 System Memory Map Table Pointer

#### Function 0003h: Change Processor Clock

Parameters

D1 Processor Clock in kHz unit

Return

D0 Processor Clock Changed in kHz unit

# External Interfaces

# Power Supply

# System Initialization

# Debugging Interfaces

###### Brief Description of System Controller FPGA IP

* 1. Appendix Heading 2
     1. Appendix Heading 3

Appendix Heading 4

1. Footnote content [↑](#footnote-ref-1)