Extensible Homebrew Computer System Architecture Whitepaper

Detailed System Manual

2024. 9. 2.

Revision

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Before You Read This Document…

This document is detailed system manual of the homebrew computer powered by Motorola MC68030 Microprocessor. Its coverage is from low-level hardware structures and electrical characteristics to firmware operation calls to create your own bootloader and operating system or port existing applications or operating systems to this architecture.

Due to the educational purpose of this system architecture, you can freely create, modify, and delete any contents of it without almost every limitation. To read detailed information, see the license text inside of a box in the previous page.

Contacts

You can visit <https://github.com/kms1212/68k30-hbc> to create an issue to this repository.

Related Documents

More detailed informations of each components/standard used in this architecture may be needed to comprehend their operation, referencing documents in following table is recommended.

|  |  |
| --- | --- |
| Title | Contents |
| MC68030 User’s Manual | Detailed description of MC68030 Microprocessor |
| MC68882 User’s Manual | Detailed description of MC68882 Floating-point coprocessor |
| FLEX® 6000 PLD Family Datasheet | Electrical characteristics, device architecture, timing parameters, etc. of Altera® FLEX® 6000 FPGA Family |
| MAX® 7000 PLD Family Datasheet | Electrical characteristics, device architecture, ISP programming methods, timing parameters, etc. of Altera® MAX® 7000 CPLD Family |
| Altera® Configuration Handbook | Configuration methods for Altera® FPGA Families. |
| JEDEC Standard No.21-C Page 4.4.2 | Description of JEDEC 72-pin SIMM Memory module standard. |
| 030HBC Software Development Supplement Manual | Considerations and detailed information regarding software (Bootloader/OS/Application) development (TBD) |
| TBD |  |

Most of these documents will be archived into a single site soon.

Note that this list of related documents can be updated without noticing.

Notes and Warnings

Warning

Contents described inside this box are warnings about the factors which can cause misoperation of the system.

Note

Contents described inside this box can be an useful trick and shortcut to utilize this documentation.

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# Overview

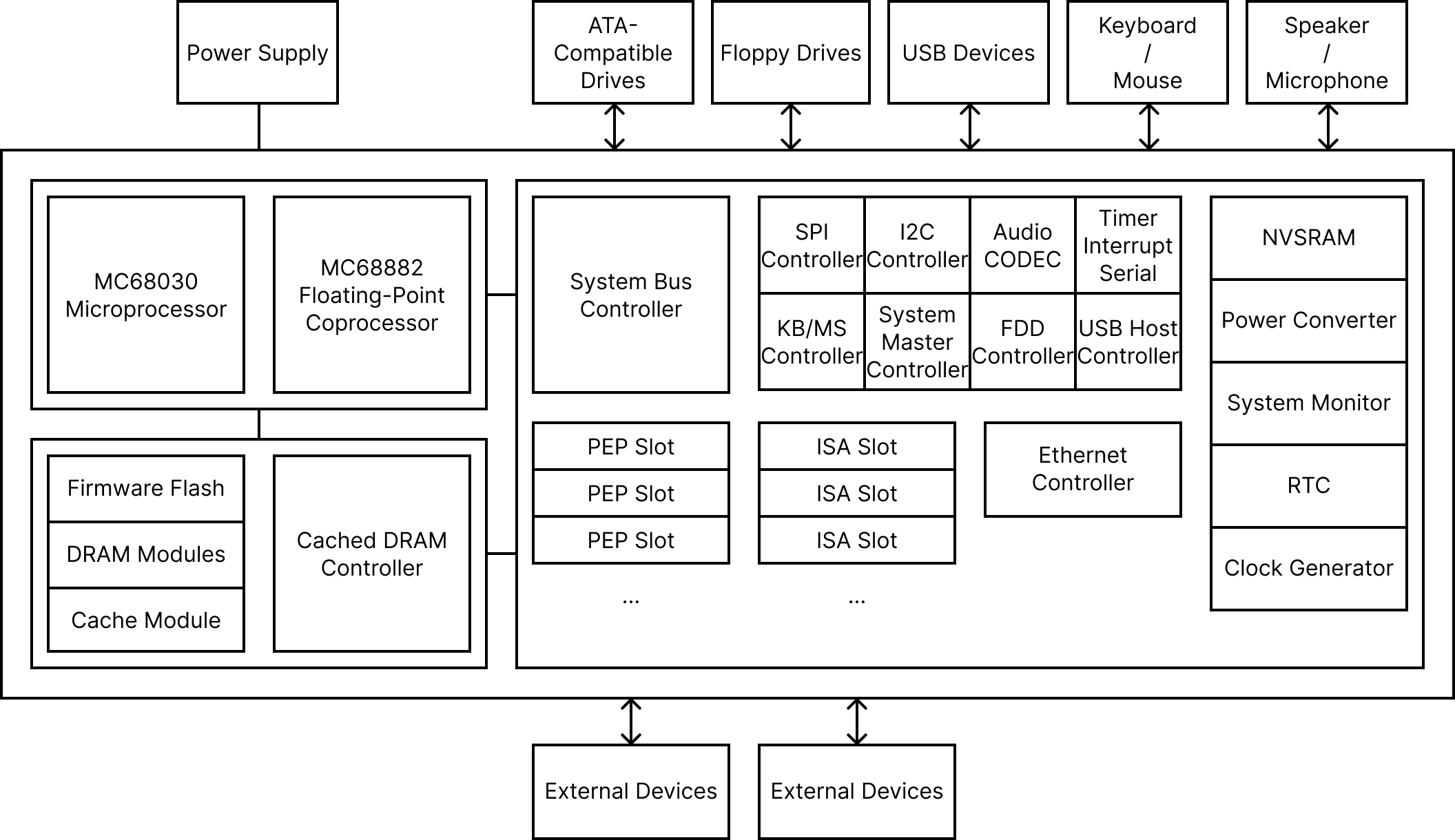


Figure 1 System Block Diagram

Contents in this chapter roughly explains about the entire architecture of the `030 Extensible Homebrew Computer. The architecture of this system is designed to provide flexible operations, rich system functions, and large expansion capabilities.

## Features

The features and characteristics of the `030 Extensible Homebrew Computer (hereafter ‘030EHBC’) are listed as follows:

* Powered by a Motorola MC68030 microprocessor and a MC68882 coprocessor
  + 32-bit microprocessor up to 50 MHz of operation clock
  + Integrated 256-byte data cache and 256-byte instruction cache
  + Paged Memory-Management Unit (MMU) integrated for memory protection
  + 7 levels of interrupt autovector
  + A MC68882 floating-point coprocessor which accelerates real-number arithmetic is installable
* Configurable processor frequency up to 50MHz and two fixed clocks at 24MHz and at 14.61818MHz
* Four 72-pin SIMMs for DRAM capacity up to 128MiB
* A system controller implemented on FPGA
  + Configurable CPU clock
  + CPU Burst Cache Fill operation
  + DRAM controller
  + IDE/ISA Bus controller
  + Power management features
* 4 DMA channels
* Full support of IRQ signals driven by ISA bus devices
* 8 programmable timers including refresh counter
* Rich capabilities of peripheral buses and external devices:
  + 1 floppy drive interface
  + 1 USB host interface
  + PS/2 keyboard and mouse interface
  + 1 RS232 serial port
  + 1 10Base-T 10Mbps ethernet port
  + Speaker/Microphone/Line-in audio jack
  + I2C, SPI
* 3 ISA 36-pin and 62-pin card-edge connector
* Real-time clock and NVSRAM
* Coin cell battery backup for a RTC and a NVSRAM
* 1MiB Flash Memory for Firmware
* A System Master Controller implemented on ATMega32 controls switches, a buzzer, reset signals, etc.
* A 24-pin ATX power supply connector for power inputs

## System Performance

Default

Bold

Italic

Bold Italic

Monospaced

Bold Monospaced

|  |  |
| --- | --- |
| Field | Description |
| Data | Data |
| Data | Data |
| Data | Data |
| Data | Data |

Table 1‑1 Descriptor Table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Offset | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0000h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0010h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0020h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0030h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0040h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0050h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0060h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Table 1‑2 Hex Space Table

Code

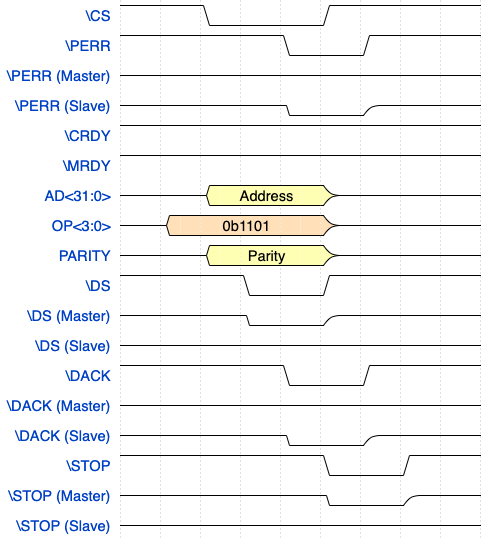


Figure 1‑2 Image File

Footnote[[1]](#footnote-1)

* Item1
* Item2
* Item3
* Item4
* Item5
* Item6
* Item7
* Item8
* Item9
* Item10
  + Subitem1
  + Subitem2
  + Subitem3

Note

Note Content

1. Item1
2. Item2
3. Item3
4. Item4
5. Item5
6. Item6
7. Item7
   1. Subitem1
   2. Subitem2
   3. Subitem3

Warning

Warning Content

System Block Diagram

# Processor & Coprocessor

## The Main Processor

## The Coprocessor

# Memory Subsystem

Figure 3 System Memory Map

## System Memory Map

|  |  |  |
| --- | --- | --- |
| FFFFFFFF |  | MMIO Area |
| FF000000 |
| FEFFFFFF |  | ISA SMEM Area |
| FE100000 |
| FE0FFFFF |  | ISA MEM Area |
| FE000400 |
| FE0003FE |  | ISA I/O Area |
| FE000000 |
| FDFFFFFF |  | Boot Firmware Area  (Max. 16 MiB) |
| FD000000 |
| FCFFFFFF |  | Reserved |
| FC000000 |
| FBFFFFFF |  | System Memory  (Max. 4,032 MiB) |
| 00000008 |
| 00000007 |  | Boot Vector or System Memory |
| 00000000 |

### Boot Vector

### System Memory

### Boot Firmware Area

### ISA Areas

### MMIO Area

## Dynamic RAM Modules

## Memory-Mapped I/O

## Direct Memory Access

# System Controller

## Register Description

### Register 00h: CPU Configuration

Default Value: 00h

Operation: Read / Write

Bit 7 Force CPU Clock to 8MHz

0 Disable

1 Enable

Bits 6-4 CPU Clock

000 33.33MHz

001 80MHz

010 66.67MHz

011 50MHz

100 40MHz

101 60MHz

110 25MHz

111 20MHz

Bits 3-1 Reserved

Bit 0 Enable CPU Burst Operation

0 Disable

1 Enable

### Register 01h: DRAM Configuration

Default Value: 00h

Operation: Read / Write

Bit 7 Reserved

Bits 6-4 Address Mapping Mode

000 Mapping mode 0

001 Mapping mode 1

010 Mapping mode 2

011 Reserved

100 Mapping mode 4

101 Mapping mode 5

110 Mapping mode 6

111 Reserved

Bit 3 RAS to CAS Delay

0 3 CPU clocks

1 2 CPU clocks

Bit 2 Reserved

Bit 1 Write Cycle CAS Pulse Width

0 2 CPU clocks

1 1 CPU clock

Bit 0 RAS Precharge Time

0 2 CPU clocks

1 1 CPU clock

### Register 02h: Firmware ROM Configuration

Default Value: 00h

Operation: Read / Write

Bits 7-3 Reserved

Bits 2-0 ROM Latency

000 8 CPU clocks

001 1 CPU clock

010 2 CPU clocks

011 3 CPU clocks

100 4 CPU clocks

101 5 CPU clocks

110 6 CPU clocks

111 7 CPU clocks

### Register 03h: Power Management Configuration

Default Value: 00h

Operation: Read / Write

Bit 7 Power Off System

0 No operation

1 Power off system immediately

Bits 6-2 Reserved

Bit 1 Power Switch Operation

0 Power off system immediately

1 Raise IRQ

Bit 0 Power Switch Status (Read Only)

0 Not pressed

1 Pressed

### Registers 04h-07h: DRAM Bank Boundary Configuration

Default Value: 00h

Operation: Read / Write

Bit 7 Reserved

Bit 6-4 Bank Boundary 1

Bit 3 Reserved

Bit 2-0 Bank Boundary 0

000: 128kiB

001: 256kiB

010: 512kiB

011: 1MiB

100: 2MiB

101: 4MiB

110: 8MiB

111: 16MiB

### Registers 08h-09h: IDE Bus Controller Configuration

#### Register 08h

Default Value: 00h

Operation: Read / Write

Bit 7 Enable IDE Controller

Bits 3-0 Command Delay Time

0000 16 CPU clocks

0001 1 CPU clock

0010 2 CPU clocks

0011 3 CPU clocks

0100 4 CPU clocks

0101 5 CPU clocks

0110 6 CPU clocks

0111 7 CPU clocks

1000 8 CPU clocks

1001 9 CPU clocks

1010 10 CPU clocks

1011 11 CPU clocks

1100 12 CPU clocks

1101 13 CPU clocks

1110 14 CPU clocks

#### Register 09h

Default Value: 00h

Operation: Read / Write

Bits 7-4 Command Active Time

Bits 3-0 Post-command Delay Time

### Register 0Ah: ISA Bus Controller Configuration

Default Value: 00h

Operation: Read / Write

Bits 7-6 16-bit I/O Command Delay

00 2 BUSCLK

01 3 BUSCLK

10 4 BUSCLK

11 5 BUSCLK

Bits 5-4 8-bit I/O Command Delay

Bit 3 Reserved

Bit 2 Enable ISA Bus Region

0 Disable

1 Enable

Bit 1 16-bit I/O Wait States

0 2 wait state

1 1 wait states

Bit 0 8-bit I/O Wait States

0 5 wait states

1 4 wait states

# System Bus

## Processor Memory Bus

## PEP Bus

## ISA Bus

## ATA Bus

# Onboard Peripherals

# Bootstrap Firmware

# External Interfaces

# Power Supply

# System Initialization

# Debugging Interfaces

###### Brief Description of System Controller FPGA IP

* 1. Appendix Heading 2
     1. Appendix Heading 3

Appendix Heading 4

1. Footnote content [↑](#footnote-ref-1)