SOEN 422
Embedded Systems

Section MM

Computer Science and Software Engineering (CSSE)
Fall 2025

Presented to:
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1. Hardware Setup

Potentiometer (The Door Sensor):

- Left Pin → 3.3V
- Right Pin → GND
- Middle Pin (Wiper) → **GPIO 34** (ADC1_CH6)

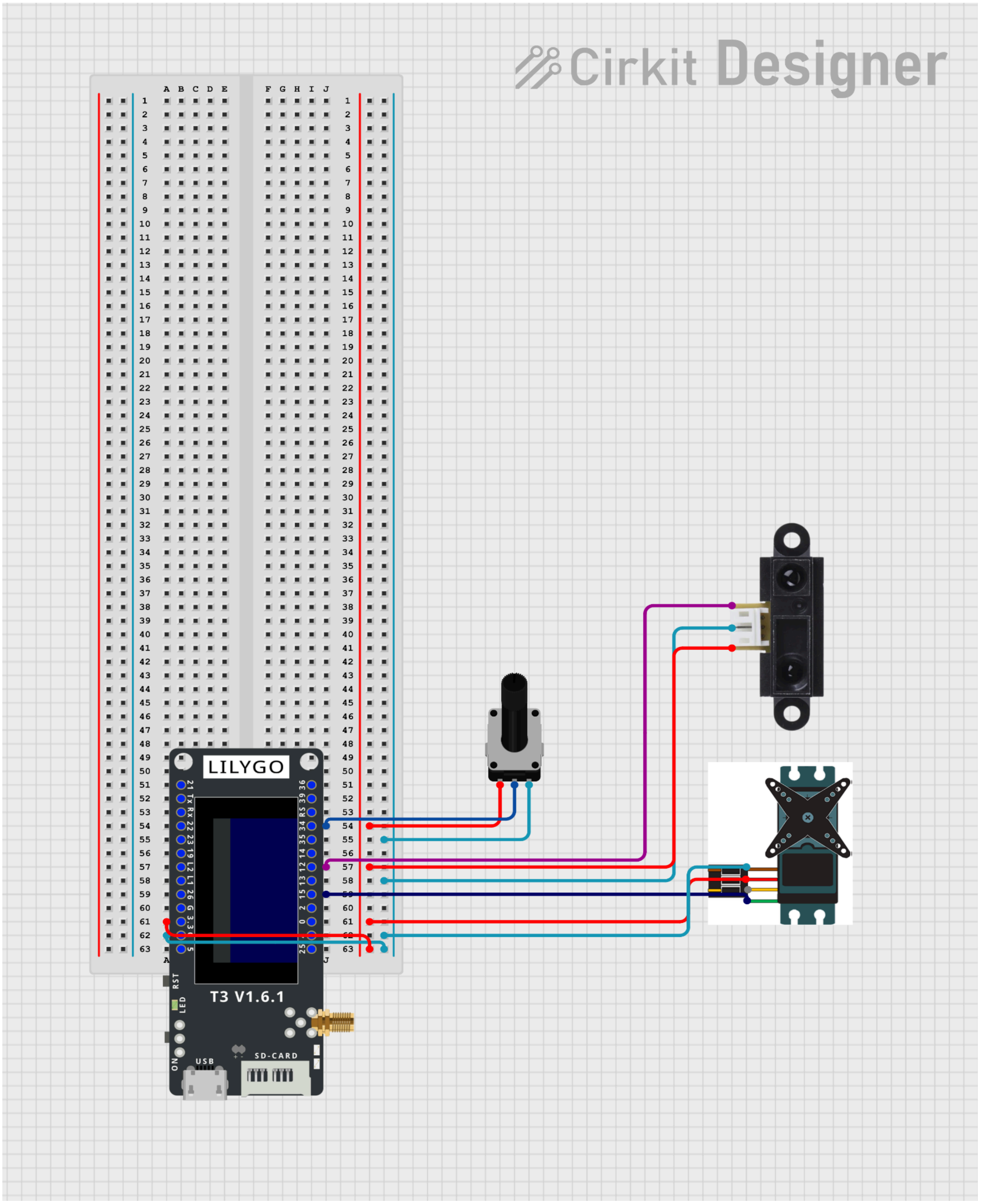
— Note: ESP32 ADC2 pins conflict with WiFi/LoRa, so we use ADC1 pins like 34.

Servo (The Lock):

- Red Wire → 5V (VIN)
- Black Wire → GND
- Yellow Wire (Signal) → **GPIO 15**

Infrared Sensor (The Motion Detector):

- VCC → 3.3V
- GND → GND
- OUT/Data → **GPIO 12**



Cirkit Designer
LILYGO
T3 V1.6.1
RST
LED
ON
USB
SD-CARD

2. Completed Tasks

These tasks represent the critical foundation of the project and are fully implemented in the current code structure (.h and .cpp files in the include and src directories).

Task Category	Task Description	Status	Rationale
Hardware Integration	**Environment Setup (PIO/VS Code**	Complete	Modular C++ environment configured and compiled.
Hardware Integration	**Modular Sensor Interface (sensors.h/.cpp)**	Complete	Created clean, isolated functions for reading **Potentiometer (ADC)** and **IR Sensor (GPIO)** data.
Hardware Integration	**Modular Actuator Interface (actuators.h/.cpp)**	Complete	Created clean, isolated functions for controlling the **Servo Motor (PWM)** lock mechanism.
Core Logic	**Finite State Machine (FSM) Architecture**	Complete	Defined the four core states (ARMED, DISARMED, ALARM_MOTION, ALARM_TAMPER) and the transition logic.
Core Logic	**Tamper/Forced Entry Detection Logic**	Complete	Implemented the core algorithm that checks the difference between initialDoorPosition and current position to detect tampering.

Core Logic	**FSM Orchestration (main.cpp)**	Complete	The main file is successfully decoupled and acts purely as an orchestrator, meeting high standards for code modularity.

3. Pending Tasks

These tasks build upon the completed foundation and represent the remaining two-thirds of the project effort.

Task Category	**Task Description**	**Status**	**Dependencies**
Communication	Implement **LoRa Network Stack**	Pending	FSM is ready to call the transmission function.
Communication	Implement **Application-Layer AES-128 Encryption**	Pending	LoRa Stack, Data Payload formatting.
Security	Implement **Hash-based Message Authentication Code (HMAC)**	Pending	AES Encryption, LoRa Packet structure.
Security	Implement **Bluetooth 2FA Challenge/Response Protocol**	Pending	FSM state handling for disarming.
Resilience/Forensics	Implement **MicroSD Card Black Box Logging** (SPI)	Pending	FSM alarm events, SPI library integration.
Resilience/Forensics	Implement **Watchdog Timer (WDT)** for Availability	Pending	FSM integration point (setup and periodic reset).

4. Conclusion and Next Steps

I have successfully implemented the entire physical integration and the core logical Finite State Machine (FSM) architecture. The next phase will focus entirely on implementing the specialized security and communication protocols (LoRa, AES, and HMAC) as proposed.