BRAC UNIVERSITY

CSE-350: Digital Electronics and Pulse techniques

Exp-03: Study of a TTL NAND gate with totem pole output

Name: Bousra Jahan Lia	Section: 10
ID: 20301335	Group: 02

OBJECTIVES

1. Building standard TTL NAND Gate.
2. Measure the voltages and verify the circuit.

Equipments and component list

Equipments

1. Digital Multimeter
2. DC power supply

Component

- NPN Transistor (C828) - x5 pieces
- Diode 1N4003 - x1 piece
- Capacitor - 4.7 μF - x1 piece
- Resistors -
  - 4K - x1 piece
  - 1.5K - x1 piece
  - 1K - x1 piece
  - 100 - x1 piece

Task-01: TTL NAND gate

THEORY

In this task, we will implement a Transistor-Transistor Logic (TTL) NAND gate with a totem-pole output. Transistor-Transistor Logic, or TTL, refers to the technology for designing and fabricating digital integrated circuits that employ logic gates consisting primarily of bipolar transistors. TTL is the successor of diode-transistor logic (DTL), overcoming the main problem associated with DTL, i.e., lack of speed. TTL provides

faster switching compared to DTL; in fact, TTL is the fastest saturated logic family. Figure 1 shows 2-input TTL NAND gate with a totem-pole output.

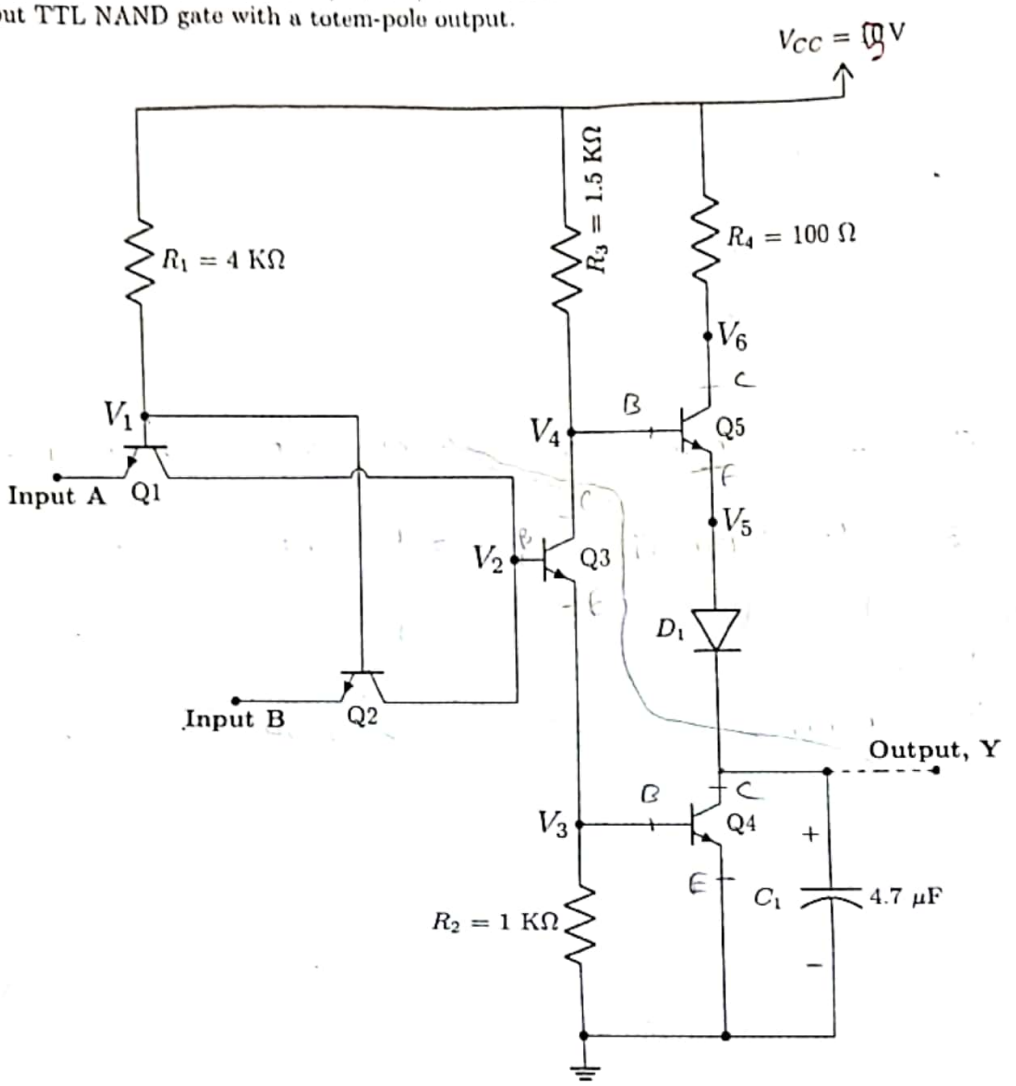


Fig 1: TTL NAND Gate

If any of the inputs A and B is LOW (0.2V), transistor Q1 and/or Q2 will operate in saturation mode and V_2 node will have a voltage of 0.2V + $V_{CE}(sat)$ = 0.4V which causes transistors Q3 and Q4 to be in cut-off mode. Now, node V_4 has 5V while V_6 is obviously less than 5V because of voltage drop in R_4 and Q5 will operate in forward-active mode which means V_{CE} of Q5 is 0.7V. As the diode D_1 has a conducting voltage drop of 0.7V and V_Y will be V_4 - 0.7 - 0.7 = 3.6V approximately which we shall consider as high voltage in output. When both inputs are HIGH (5V), transistors Q1 and Q2 will operate in reverse-active mode. In this case, transistors Q3 and Q4 will be in saturation which ensures that V_{CE} of Q4 is 0.2V and thus the output is 0.2V (LOW).

The most basic TTL circuit has a single output transistor configured as an inverter with its emitter grounded and its collector tied to V_{CC} with a pull-up resistor, and with the output taken from its collector. Most TTL circuits, however, use a totem pole output circuit, which replaces the pull-up resistor with a V_{CC}-side transistor sitting on top of the output transistor. The emitter of the V_{CC}-side transistor (whose collector is tied to V_{CC}) is connected to the collector of the output transistor (whose emitter is grounded) by a diode. The output is taken from the collector of the output transistor.

As mentioned earlier, TTL has a much higher speed than DTL. This is due to the fact that when the output transistor (Q4 in Figure 1) is turned off, there is a path for the stored charge in its base to dissipate through, allowing it to reach cut-off faster than a DTL output transistor. At the same time, the output capacitor is charged from V_{CC} through Q5 and the output diode (D_1), allowing the output voltage to rise more quickly to logic '1' than in a DTL output wherein the output capacitor is charged through a resistor.

:edure:

1. Connect the circuit as shown in Figure 1.
2. Observe the output for all possible input combinations and fill up table-1.

Data Table

V_A (V)	V_B (V)	V_1 (V)	V_2 (V)	V_3 (V)	V_4 (V)	V_5 (V)	V_6 (V)	V_Y (V)
0	0	0.685	0.0136	0	5.01	4.59	5.02	4.37
0	5	0.685	0.0161	0	5.01	4.59	5.02	4.37
5	0	0.7	0.0304	0	5.01	4.5	5.02	4.37
5	5	2.211	1.794	0.81	0.485	0.361	5.01	0.05

Table 1: Table for TTL NAND gate

Report

Please answer the following questions briefly in the given space.

1. Why is totem-pole output used in place of a passive pull-up resistor?

Ans. Totem-pole output has an output circuit with two transistors. ~~combined~~ The high or low level is determined without setting pull-up resistance to the output. Totem-pole output can both sink and source. Totem-pole configuration's place is to supply enough current to ensure that to output rises to a sufficiently high voltage when pushed up and drain enough current to ensure that the output falls to a suitably low value when pulled down.

2. What is the function of Q3 transistor(phase-splitter)?

Ans. Q_3 transistor works as switch in TTL NAND gate circuit. When Q_3 = ON, Q_5 base will get 0 input and Q_4 base will have high input. Similarly, when Q_3 = OFF, Q_5 base will

have high input and Q_4 base will have low input. This Q_3 transistor split input in high and low that's why it ~~calls~~ is called phase splitter.

3. What may happen if diode D_1 is not used in the circuit?

Ans. If diode D_1 is not used in the circuit then Q_5 ~~of~~ transistor will be ON. ~~From~~ the ~~taul~~ purpose of using NAND gate is getting inverted result. Because of the diode, when ~~g~~ we gave Input=Low we get Output = High and Input = High, Output = Low. But if we didn't use diode we will get High ~~output~~ in every case.

Input=Low: Q_1, Q_2 = Active
$Q_3 \rightarrow$ OFF, Q_4 = OFF, Q_5 = ON
V_0 = High

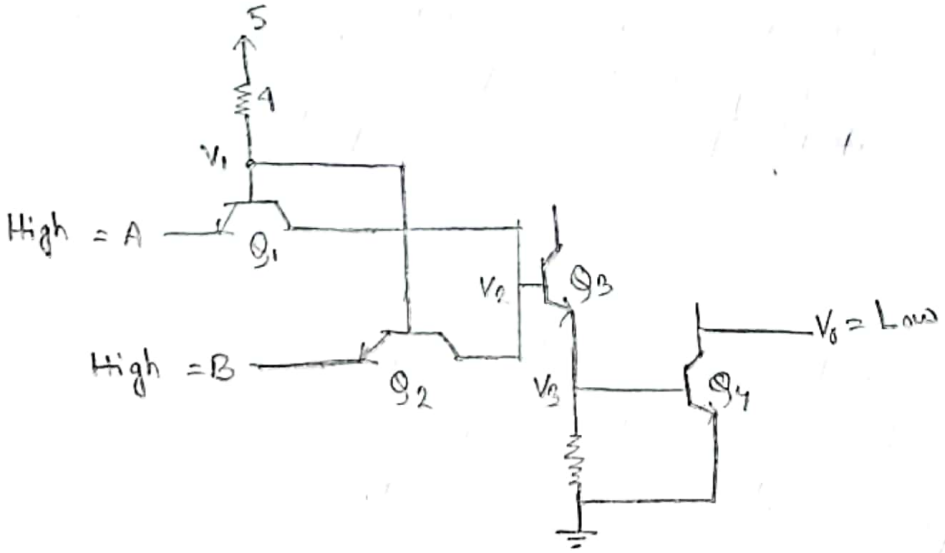
Input=High: Q_3 = ON, Q_4 = ON, Q_5 = OFF. $\therefore V_0$ = Low
[If the diode is connected and the circuit will multfunction.]

4. What is the mode of operation of the Q5 transistor when output is HIGH?

Ans. when, V_0 = High, Q_5 = ON [Mode of operation = saturation]
As Q_3 is OFF, So collector of Q_3 will not be connected with base of Q_5. And TTL is a part of saturated Logic Family, That's why ON transistor ON means Saturation.

5. Draw the active portion of the circuit when output is LOW.

Ans.



What is the operating mode of Q1 and Q4 transistors when Input A is LOW? Verify using experimental

ns.

From experimental data we get,
Input A is low, Value of Q_1 base = 0.685 V and Q_4 base = 0 V which means Q_1 transistor is in Active mode and Q_4 transistor is in cutoff mode.

we know,

In case of transistor, $V_\gamma = 0.5$ V [minimum voltage to turn on transistor]

Here $V_1 = 0.685$ V, If Q_1 is in saturation mode then, $V_1 = 0.8$ V
In this case V_1 is in Active region.
And $V_2 < 0.5$ V in every cases when A = low.
$\therefore Q_3$ = OFF, so, $V_3 = 0$ V, that's why Q_4 is cut off.

Data Table

V_A (V)	V_B (V)	V_1 (V)	V_2 (V)	V_3 (V)	V_4 (V)	V_5 (V)	V_6 (V)	V_Y (V)
0	0	0.685	0.0136	0	5.01	4.59	5.02	4.37
0	5	0.685	0.0164	0	5.01	4.59	5.02	4.37
5	0	0.7	0.0304	0	5.01	4.5	5.02	4.37.
5	5	2.211	1.794	0.8	0.885	0.361	5.01	0.05

Table 2: Table for TTL NAND gate

Dipika. 20.10.22
Signature