BRAC UNIVERSITY

CSE 350: Digital Electronics and Pulse techniques

Exp-01: Implementing Diode Logic (DL) gates

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Objectives

1. Construct Diode Logic (DL) gates.
2. Understanding the circuit operations.

Equipment and component list

Equipment

1. Digital Multimeter
2. DC power supply

Component

- NPN Transistor (C828) - x1 piece
- Diode 1N4003 - x2 pieces
- Resistors -
  - 450 Ω - x2 piece
  - 15 KΩ - x1 piece
  - 2.2 KΩ - x1 piece
  - 100 KΩ - x1 piece

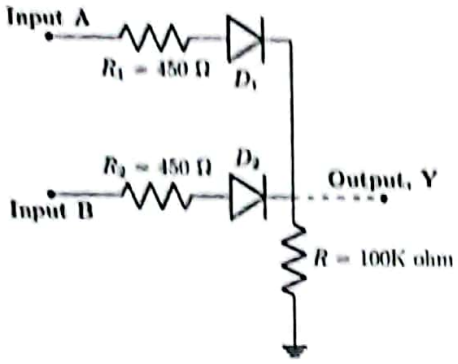


Fig 1: OR gate

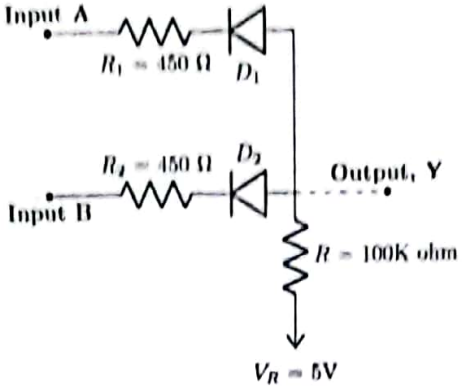


Fig 2: AND gate

Task-01: OR gate

THEORY

In digital logic, a 2-input OR gate outputs a logical HIGH if at least one of the inputs is HIGH. Otherwise, the output of the OR gate is logical LOW.
In this task, we will implement a Diode Logic (DL) OR gate. In Fig. 1, we can see two input nodes (A and B) and one output node (Y) of the OR gate. We will consider 5V as logical HIGH input and 0V as logical LOW input in our experiment. Now, if any of the inputs are set to 5V, the corresponding diode is turned on. As a result, a current flows through that diode. This current ultimately flows through R towards the ground, thus creating a voltage drop across the R resistor. As R_1 and R_2 resistors are very small compared to R, the voltage drop across R will be close to 5V. In this case, we will consider the obtained output voltage at node Y to be logically HIGH. Next, if all the inputs are set to 0V, no current flows through the diodes and resistor R. As a result, the voltage drop across R will be zero. So, the output voltage will be 0V, which we will consider to be logically LOW.

Task-02: AND gate

THEORY

In digital logic, a 2-input AND gate outputs a logical LOW if at least one of the inputs is LOW. Otherwise, the output of the AND gate is logical HIGH.
Similar to the previous task, we will implement a Diode Logic (DL) AND gate. If any of the inputs are set to 0V, the corresponding diode is turned on. As a result, a current flows through that diode from the V_R voltage source. This current flows through R and creates a voltage drop across the resistor. As R_1 and R_2 resistors are very small compared to R, the voltage drop across R will be close to 5V. As a result, the obtained output voltage at node Y will be close to 0V which we will consider as logically LOW. Next, if all the inputs are set to 5V, no current flows through the diodes and resistor R. Therefore, the voltage drop across R will be zero. So, the output voltage will be the same as V_R or 5V, which is logically HIGH.

Task-03: Inverter (NOT gate)

THEORY

In digital logic, an inverter or NOT gate is a logic gate which implements logical negation. It has a single input and a single output where the output is the exact opposite of the input. Meaning, if the input is Logical High, the output will be Logical Low and vice versa. The RTL implemantation of an inverter circuit is shown in Figure 03.
Here the input is applied to the base of a Transistor or, BJT (Q_1) through the resistor R_1 and the output is available at the collector terminal (point Y). We connect the ground terminal to the emitter node directly and to the base node through the resistor R_2. Hence, when the input V_i is LOW (0V), the 'Base' terminal

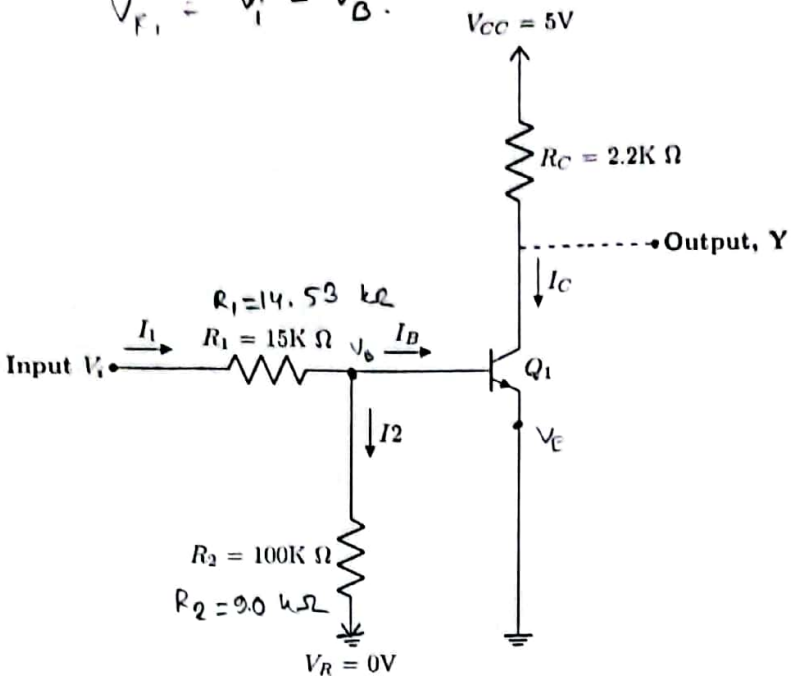


Fig 3: Inverter (NOT gate)

of the transistor cannot be at a voltage higher than zero. For Q1 to be turned ON, the Base-Emitter voltage difference must be greater then 0.5V. Thus, the BJT cannot turn ON when the input is LOW and operates in cutoff mode. This means Q_1 acts like an open circuit and the current passing through the R_C resistor (I_C) is zero. As a result, there will be no voltage drop in the resistor R_C and the voltage of the output point (Y) will be same as V_{CC} = 5V (High).
On the other hand, if a HIGH input (5V) is applied at the input terminal (V_i), Q_1 will be driven into saturation mode. In this mode, the Collector-Emitter voltage difference (V_{CE}) is nearly 0.2V. As the emitter is connected to the ground terminal, the emitter voltage (V_E) is zero. Hence, the collector voltage will be close to 0.2V(LOW). Thus, the output of the circuit is always the opposite of the input.

Procedure:

1. Connect the circuit as shown in Fig: 1, 2 & 3.
2. Observe the output for all possible input combinations thus verify the type of gate.
3. Fill up the following tables for OR gate, AND gate and Inverter.

Data Tables

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	0	0	0	0	0
0	5	0	21.9×10^{-3}	0	4.86×10^{-5}	4.55
5	0	21.7×10^{-3}	0	4.83×10^{-5}	0	4.55
5	5	11.6×10^{-3}	10.6×10^{-3}	2.58×10^{-5}	2.36×10^{-5}	4.59

Case-3:

Table 1: Table for OR Gate

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	11.4×10^{-3}	10.5×10^{-3}	2.53×10^{-5}	2.33×10^{-5}	0.425
0	5	21.7×10^{-3}	0	4.83×10^{-5}	0	0.36
5	0	0	21.9×10^{-3}	0	4.87×10^{-5}	0.467
5	5	0	0	0	0	4.97

Table 2: Table for AND Gate

V_i (V)	V_{R1} (V)	V_{R2} (V)	V_{Rc} (V)	I_1 (mA)	I_2 (mA)	I_B (mA)	I_C (mA)	V_Y (V)
0	0	0	0	0	0	0	0	5.02
5	4.33	0.681	4.97	0.298	7.57×10^{-3}	0.29043	2.28	37.6×10^{-3}

Table 3: Table for RTL inverter

Report

Let, $\beta_{forward} = 10$

Please answer the following questions briefly in the given space.

1. Verify that the transistor will be operating in the saturation and cutoff region in two cases for the inverter circuit (Use experimental data for verification).

Ans. When $V_{in} = 0$ (low)

$I_B = 0$; $V_o = 5.02$ (high)

↓

Transistor is in cutoff region (verified)

When $V_{in} = 5$ (high)

$\beta_{Forced} = \frac{I_C}{I_B} < \beta_{Forward}$

$\beta_{Forced} = \frac{2.28}{0.29043} = 7.85$

$7.85 < 10$

$\beta_{Forced} < \beta_{Forward}$ (verified)

2. For OR gate circuit, should I_{R_1} and I_{R_2} be equal theoretically when $V_A = V_B = 5V$? Did you obtain a similar result in your experiment? Explain briefly.

Ans. When $V_A = V_B = 5$ V [Case-3 : Both high], I_{R_1} & I_{R_2} should be equal theoretically. Yes, we obtained a similar result in our experiment where $I_{R_1} = 2.58 \times 10^{-5}$ mA and $I_{R_2} = 2.36 \times 10^{-5}$ mA. So, $I_{R_1} \approx I_{R_2}$. The slight 0.00000022 mA difference is the absolute error occurred due to the different V_{R_1}, V_{R_2} values from which I_{R_1} and I_{R_2} were calculated. V_{R_1} and V_{R_2} have slight different values because they were measured using a multimeter and we all know that multimeters show the values within a range and not the exact values.

3. (For both OR AND gate circuits) Will the diodes D_1 and D_2 work, if $V_A = V_B = 6V$ and $V_R = 5V$?

Ans. If $V_A = V_B = 6$ V [Case-3: Both inputs high] and $V_R = 5$ V:

For OR gate circuit, the diodes D_1 and D_2 will work because

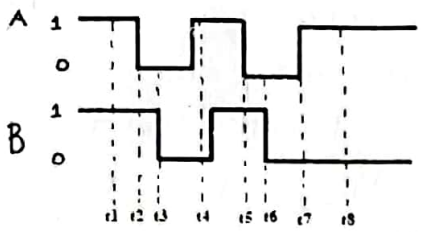
$I_A = I_B = \frac{6-5}{450} = 2.2 \times 10^{-3}$ A $> 2.644 \times 10^{-5}$ A, which it was supposed to be if $[V_R = V_{R_1} = V_{R_2}]$ V_R wasn't constant.

For AND gate circuit, since both the inputs are high and the drodes are in reverse direction, there will be no current flow across the diodes and the diodes will act as open circuits and $V_y = V_R = 5$ V. So, the diodes will be off ie will not work.

4. What is the function of $V_R = 0V$ at the base of an inverter in figure 3?

Ans. $V_R = 0$ Voltage means the R_2 resistor is basically grounded. Its function is to expand the very small transistor input voltage range (about 0.7V) to the logical "1" level (about 5V) by converting the input voltage into current. The base resistor's (R_2's) resistance is settled by a compromise: it is chosen low enough to saturate the transistor and high enough to obtain high input resistance.

5. Assuming AND gate, Draw the output.



AND gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Ans.

	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
A	1	0	0	1	0	0	1	1
B	1	1	0	0	1	0	0	0
output ← Y	1	0	0	0	0	0	0	0

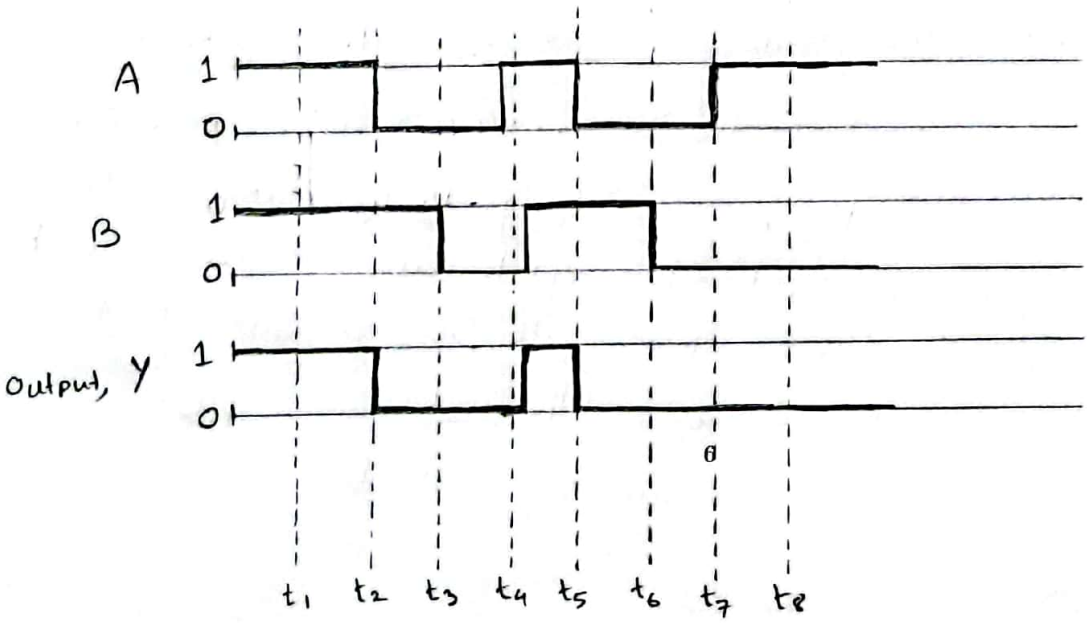


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Table 4: Table for OR Gate

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	11.9×10^{-3}	10.5×10^{-3}	2.53×10^{-5}	2.33×10^{-5}	0.425
0	5	21.7×10^{-3}	0	4.83×10^{-5}	0	0.36
5	0	0	21.9×10^{-3}	0	4.87×10^{-5}	0.467
5	5	0	0	0	0	4.97

Table 5: Table for AND Gate

V_i (V)	V_{R1} (V)	V_{R2} (V)	V_{Rc} (V)	I_1 (mA)	I_2 (mA)	I_B (mA)	I_C (mA)	V_Y (V)
0	0	0	0	0	0	0	0	5.02
5	4.35	0.681	4.97	0.298	7.57×10^{-3}	0.29043	2.28	37.6×10^{-3}

Table 6: Table for RTL inverter

Signature

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