Brac University

CSE 350: Digital Electronics and Pulse techniques

Exp-04: Analysis of the binary weighted and R/2R ladder D/A converters

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Name:	Section:
ID:	Group:

Objectives

1. To construct two different D/A converters
2. Verifying that the digital signal is converted to a proportional analog signal

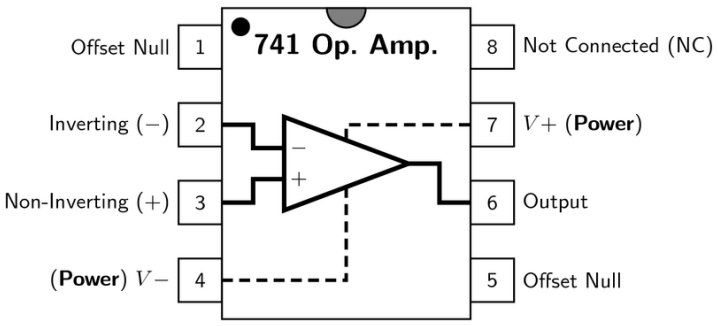
Equipment and component list

Equipment

1. Digital Multimeter
2. DC power supply

Component

- Operational amplifier - UA741 - x1 piece
- Resistors -
  - ♦ 10 KΩ - x4 piece
  - ♦ 5 KΩ - x1 piece
  - ♦ 1.25 KΩ - x1 piece
  - ♦ 20 KΩ - x6 piece
  - ♦ 2.5 KΩ - x1 piece
  - ♦ 1 KΩ - x1 piece



741 IC pin diagram

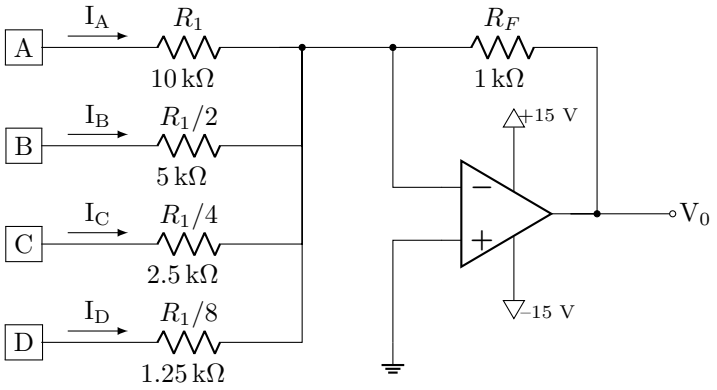


Figure 1: Binary weighted D/A converter

Task-01: Binary weighted D/A converter

THEORY

A four bit converter will have $2^4 = 16$ input combinations. Consequently, the converter will show 16 different output analog voltage levels for 16 different input combinations.

Case 1: (D, C, B, A) = (0, 0, 0, 1)
The voltage across R_1 is 5V. So, the current through R_1 is $I_A = 0.5$ mA. Since the current into the op-amp input terminals are negligible, this 0.5 mA current will flow through the R_F resistance. Hence, the voltage across the resistance R_F is, $V_{R_F} = 0.5$ mA $\times$ 1 KΩ = 0.5 V. Consequently, the output voltage is -0.5V.

Case 2: (D, C, B, A) = (0, 0, 1, 0)
The voltage across $R_1/2$ is 5V. So, the current through $R_1/2$ is $I_B = 1$ mA. Since the current into the op-amp input terminals are negligible, this 1 mA current will flow through the R_F resistance. Hence, the voltage across the resistance R_F is, $V_{R_F} = 1$ mA $\times$ 1 KΩ = 1V. Consequently, the output voltage is -1V.

Case 3: (D, C, B, A) = (0, 0, 1, 1)
The voltage across R_1 is 5V and the voltage across $R_1/2$ is 5V. The current through R_1 is $I_A = 0.5$ mA and the current through $R_1/2$ is $I_B = 1$ mA. So, the total current through the resistance R_F is 1.5 mA. Hence, the voltage across the resistance R_F is, $V_{R_F} = 1.5$ mA $\times$ 1 KΩ = 1.5V. Consequently, the output voltage is -1.5V.

Similarly, we can calculate the output voltage for any other input combination. The analog output voltage levels corresponding to digital input voltages vary as shown in figure 3.

The output is a negative going staircase waveform with 15 steps of -0.5V each. In practice, due to the variations in the logic HIGH voltage levels, all the steps will not have the same size. The value of the feedback resistor R_F changes the size of the steps. Thus, a desired size for a step can be obtained by connecting appropriate feedback resistor. The only condition to look out for is that the maximum and minimum output voltages should not go beyond the saturation levels of the op-amp.

We can find that the output voltage is defined by the expression:

$$V_o = \left(\frac{V_A}{R_1} + \frac{V_B \times 2}{R_1} + \frac{V_C \times 4}{R_1} + \frac{V_D \times 8}{R_1}\right) \times (-R_F) \tag{1}$$

Task-02: R/2R ladder D/A converter

THEORY

A digital to analog converter with R and 2R resistors is shown in figure 2. As in the binary-weighted resistors converter, the binary inputs are simulated by the switches A-D and the

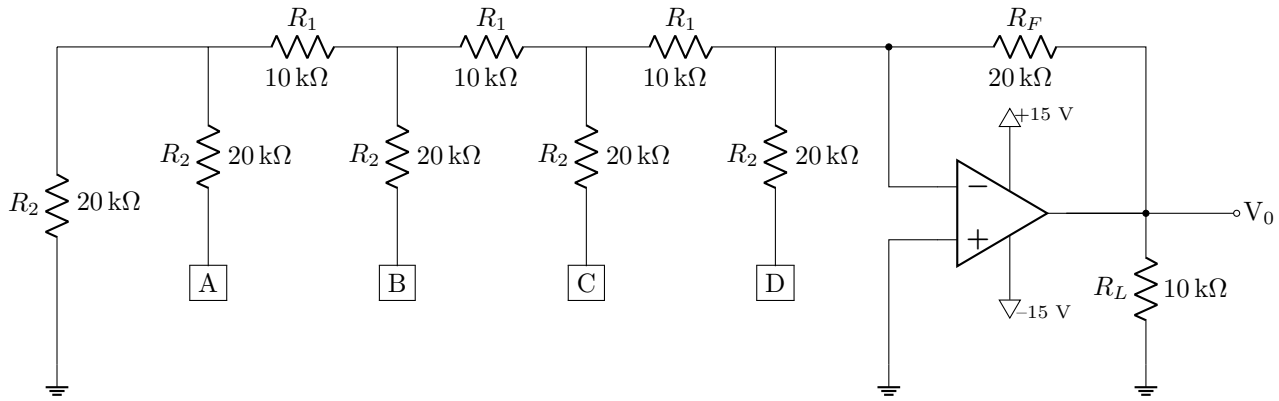


Figure 2: R/2R ladder D/A converter

output is proportional to the binary inputs. Binary inputs can be either in the HIGH (+5V) or LOW (0V) state.

The circuit can be solved using thevenin theorem. We will obtain an output vs input plot similar to that in figure 3 for this converter as well. We can find that the output voltage is defined by the expression:

$$V_O = (\frac{V_A}{8} + \frac{V_B}{4} + \frac{V_C}{2} + V_D) \times (\frac{-R_F}{R_2}) \tag{2}$$

Procedure:

1. Construct the circuits on breadboard. Supply +15V and –15V to the op amp.
2. Consider the **HIGH** input to be **5V** and the **LOW** input to be **0V**.
3. Use multimeter to measure the output voltage for different input combinations. This output voltage is the 'analog' output signal. Fill up tables 1 and 2.

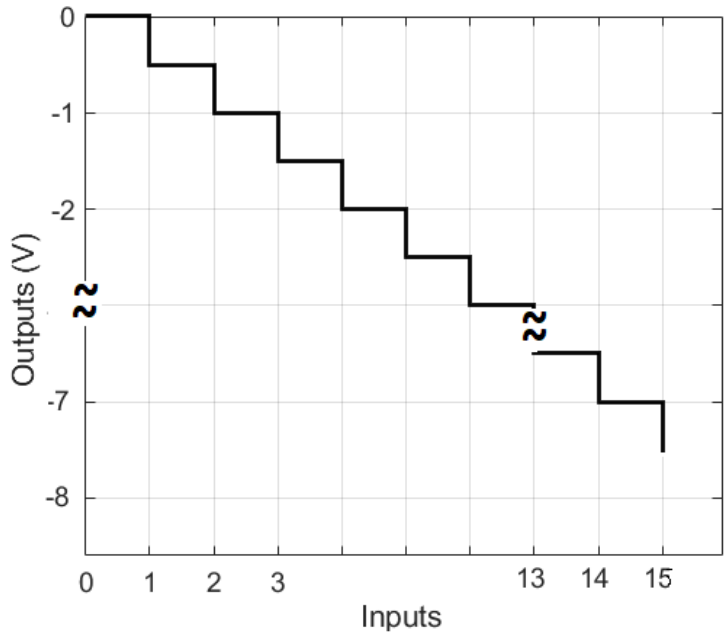


Figure 3: Staircase plot of output vs input in binary weighted D/A converter.

Data Tables

In all the data tables, write the input combinations in ascending order.

SL	$V_D(V)$	$V_C(V)$	$V_B(V)$	$V_A(V)$	$V_Y(V)$
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Table 1: Table for binary-weighted D/A converter

SL	$V_D(V)$	$V_C(V)$	$V_B(V)$	$V_A(V)$	$V_Y(V)$
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Table 2: Table for R/2R ladder D/A converter

$\overline{Signature}$

Report

Please answer the following questions briefly in the given space.

1. Fill up table 3 for all possible input combinations considering the **HIGH** input voltage to be the **sum of the last two digits of your student ID** and the LOW input to be 0V. You can use either of the D/A converters. (If the last two digits are zero or their sum is 5V, use the first two digits)

2. Find the resolution of both D/A converters.
Ans.

3. For any one of the converters, change the value of R_F (feedback resistance) to $0.5\times R_F$ and then to $2\times R_F$. For each case, measure output voltage for any two consecutive input combinations and calculate the step sizes. Does the effect on step size match with the theory?
Ans.

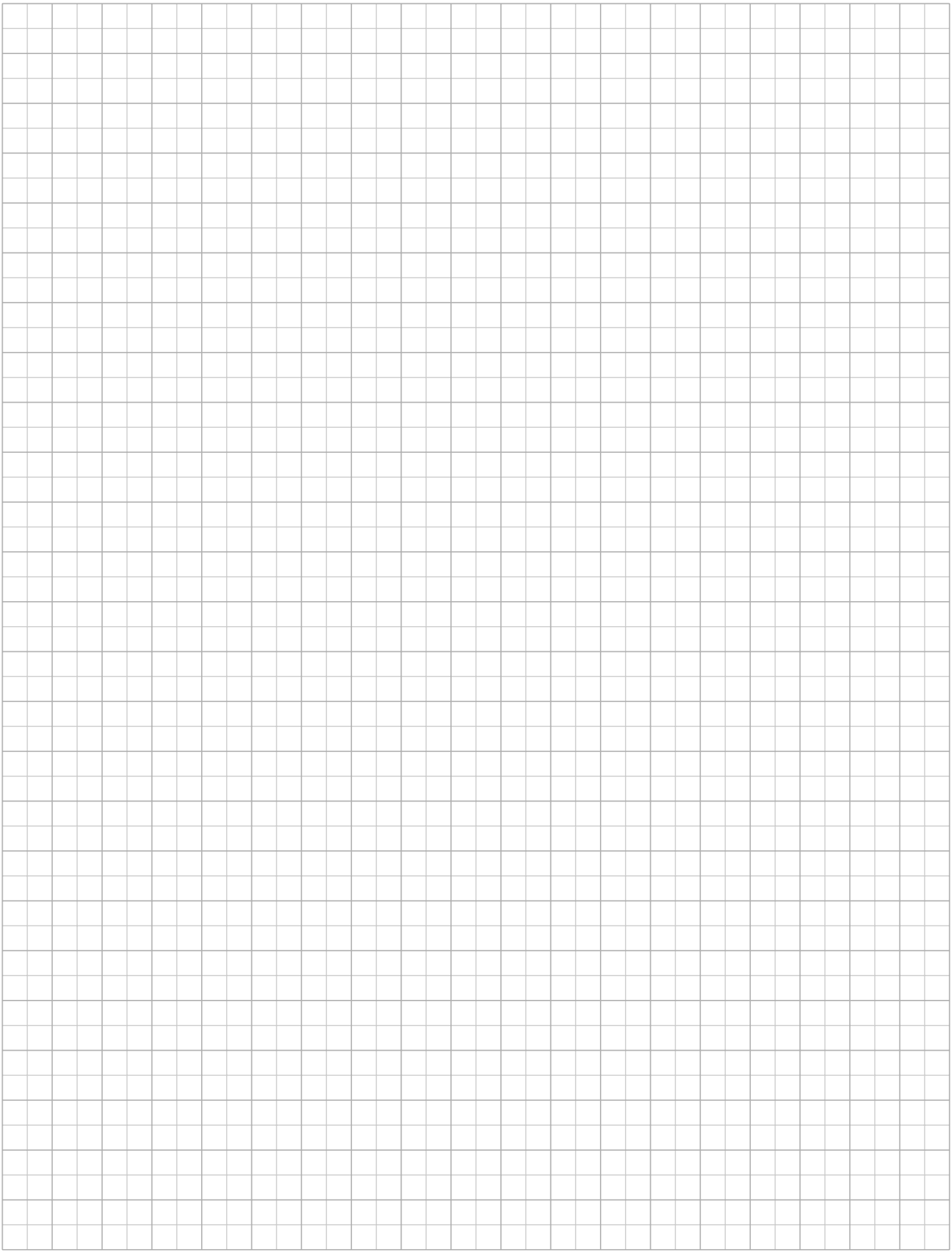
4. How can you get output lower than -15 V in the above D/A converters?
Ans.

5. Plot the results obtained in table 1 and table 2 in the given graph paper. Keep the serial no of inputs in the horizontal axis and the output voltages in the vertical axis.

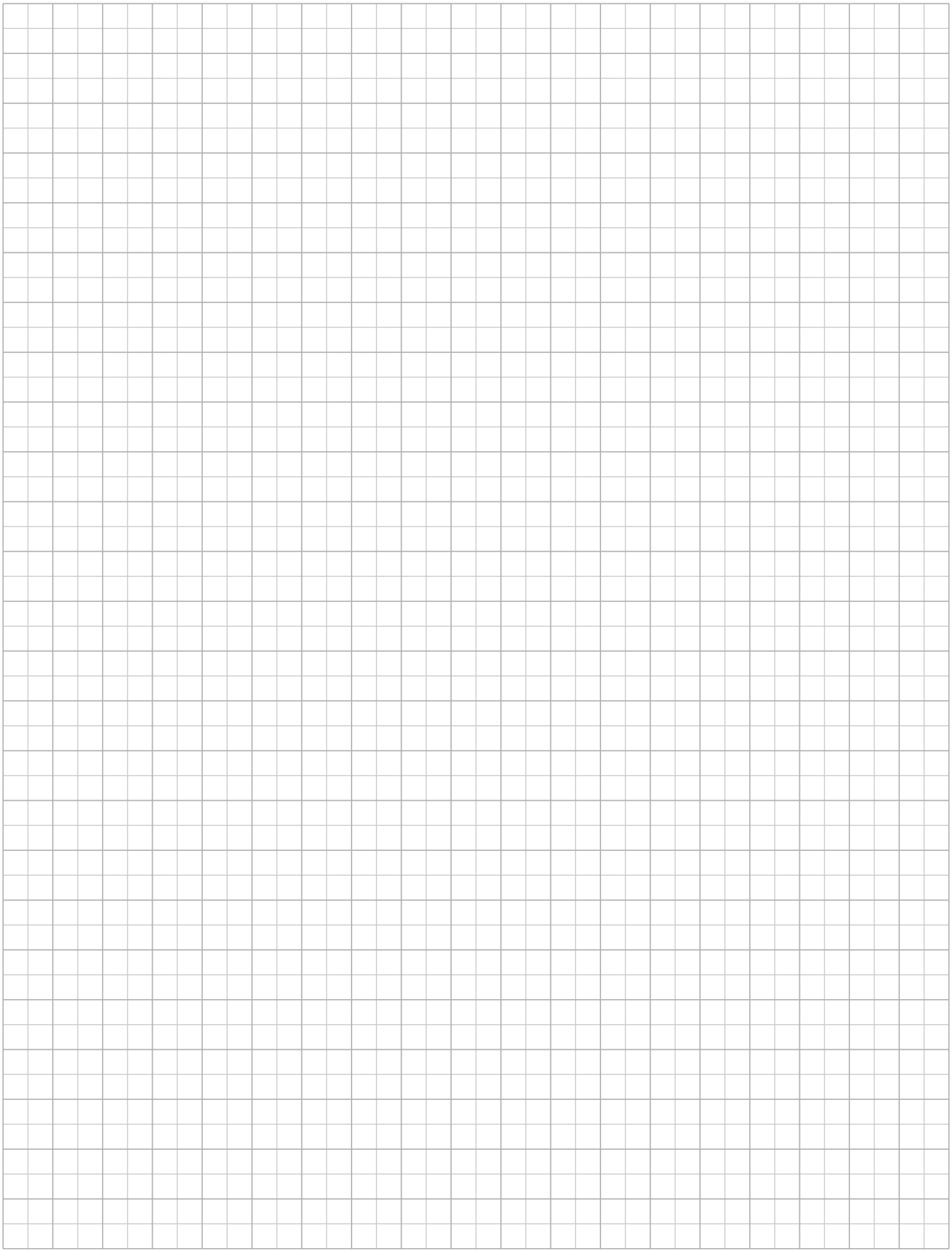
6. Briefly discuss which of the two converters is better in a practical scenario.

SL	$V_D(V)$	$V_C(V)$	$V_B(V)$	$V_A(V)$	$V_Y(V)$
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Table 3: Table for question 1 in report



Graph paper for table 1



Graph paper for table 2