Brac University

CSE 350: Digital Electronics and Pulse techniques

Exp-02: Implementing Diode Transistor Logic (DTL) gates

Name:	Section:
ID:	Group:

Objectives

1. Constructing a Diode Transistor Logic (DTL) gate.
2. Understanding the circuit operations.

Equipment and component list

Equipment

1. Digital Multimeter
2. DC power supply

Component

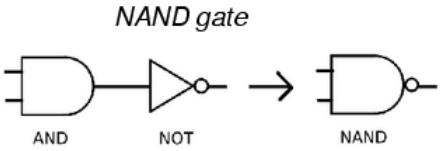
- NPN Transistor (C828) - x1 piece
- Diode 1N4003 - x4 pieces
- Resistors -
  - 2 KΩ - x2 pieces
  - 20 KΩ - x1 piece

Task-01: DTL NAND gate

THEORY

In this task, we will implement a Diode Transistor Logic (DTL) NAND gate. As can be seen in Fig. 1, a 2-input NAND gate outputs a logical HIGH if at least one of the inputs is LOW. Otherwise, the output of the NAND gate is logical LOW. It can be created by passing the output of a AND gate through an Inverter or NOT gate. One can build all other logic gates using such NAND gates. The DTL implementation of a NAND circuit is shown in Fig. 2.

Diode–transistor logic (DTL) is a class of digital circuits that is the direct predecessor of transistor–transistor logic (TTL) and the successor of resistor-transistor logic (RTL). The output side of the basic DTL NAND circuit



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 1: NAND gate Truth Table

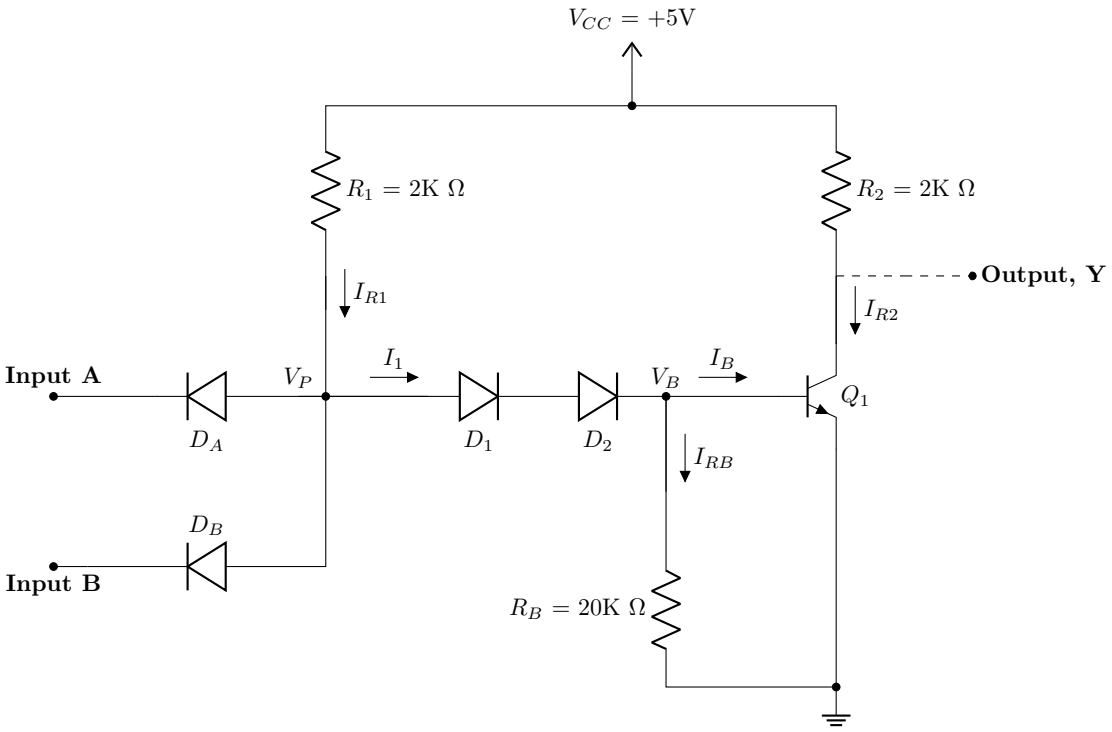


Figure 2: Diode Transistor Logic (DTL)

has a similar structure to the RTL inverter circuit, but it uses diode-logic AND on the input side. Thus, DTL circuits implement NAND gates by combining both DL and RTL logic, something that is not possible to do using solely RTL circuits or DL circuits. DTL also has better noise margin and fanout characteristics compared to RTL. (Noise margin indicates a circuit's immunity to noise, and fanout is the number of identical gates that a circuit can drive without facing errors).

On the input side of Fig. 2, we can see two diodes in reverse bias connection with respect to input - this acts as an AND gate circuit according to diode logic. The output of this AND gate is fed to the inverter input V_B (base terminal of BJT Q1) through the diodes D_1 and D_2 creating the NAND circuit. The output is obtained at the collector terminal of Q1.

When both inputs are HIGH (5V), the cathode voltage of the diodes D_A and D_B become higher than their anode voltages. As a result, both input diodes operate in the reverse bias region (turned off/disconnected), and the node V_P has a high voltage level. This causes the transistor Q_1 to operate in the saturation mode and the the NAND gate generates a LOW output. In this case, the voltage of point P (V_P) is close to 2.2V as the voltage of base terminal (V_B) in saturation is nearly 0.8V and there is a voltage drop of 0.7V in each of diodes D_1 and D_2.

When either input is LOW (0V), the corresponding input diode operates in the forward bias (turned on), and there is a voltage drop of 0.7V across the diode. Hence, the voltage at the node V_P becomes only 0.7V

higher than the LOW voltage at the input and drops much below the 2.2V required to turn on the BJT Q1. This causes the the transistor Q1 to work in the cutoff region and it acts like an open circuit. Hence, the current passing through the R_2 resistor (I_{R2}) is zero. As a result, there will be no voltage drop in the resistor R_2 and the voltage of the output point (Y) will be same as VCC = 5V (High).

Task-02: DTL Inverter

THEORY

As mentioned in the previous task, when either of the input terminals are HIGH, the corresponding diode operates in the reverse bias region - meaning it is virtually disconnected from the circuit. So we can say that if one of the inputs are set to logical HIGH, we can ignore that diode altogether, and the remaining diode input acts as a single input to the RTL inverter. Thus the resulting circuit acts as an inverter circuit (NOT gate). A roundabout way of explaining this is via the truth table of the NAND gate (Fig. 1) - when one input is set to HIGH, the output follows the inverted logic of the remaining input.

Procedure:

1. Connect the circuit as shown in Fig. 2.
2. Observe the output for all possible input combinations and fill up table-1 for NAND gate.
3. Operate the gate in Fig. 2 as an inverter by connecting either of the inputs to +5V and using the remaining one as input terminal. Fill up table-2.

Data Tables

V_A (V)	V_B (V)	V_{DA} (V)	V_{DB} (V)	V_P (V)	I_{R1} (mA)	I_{R2} (mA)	V_B (mV)	V_Y (V)
0	**0**							
0	**5**							
5	**0**							
5	**5**							

Table 1: Table for DTL NAND Gate

Input A (V)	**Input B (V)**	V_P **(V)**	V_B **(V)**	**Output Y (V)**
5	**0**			
5	**5**			

Table 2: Table for DTL Inverter

Report

Please answer the following questions briefly in the given space.

1. Using experimental data, find the operating mode of **Q1** when input A is **HIGH** and input B is **LOW**. Additionally, find whether diodes **DA** and **DB** are ON or OFF (by using the voltage across them).
Ans.

2. Assume that the **output** of the circuit shown in Fig: 1 is **LOW**. Draw the partial circuit consisting of only those components which remain active.
Ans.

3. What should be the relation between the currents I_{R1}, I_B **and** I_{RB} when all inputs are **HIGH**? Did you obtain a similar result in your experiment? Explain briefly. (use a Multi-meter as Ammeter to measure I_B).
Ans.

4. Use the relation between the currents I_{R1}, I_B **and** I_{RB} when all inputs are **HIGH** to verify the operating mode of Q1 when all inputs are HIGH. [Assume beta (β_F) $\geq$ 100]
Ans.

5. Will the circuit still work properly as NAND gate if the diodes D_1 **and** D_2 are removed? Measure the output voltage for the four different cases and verify.

Ans.

6. Vary the **input A** from **0V to 5V** while keeping **input B** fixed at 5V. What is the **maximum** value of **input A** for which the **output** remains **HIGH**? [consider any voltage above 1V as **HIGH**]

Ans.

Data Tables

V_A (V)	V_B (V)	V_{DA} (V)	V_{DB} (V)	V_P (V)	I_{R1} (mA)	I_{R2} (mA)	V_B (mV)	V_Y (V)
0	**0**							
0	**5**							
5	**0**							
5	**5**							

Table 3: Table for DTL NAND Gate

Input A (V)	**Input B (V)**	V_P **(V)**	V_B **(V)**	**Output Y (V)**
5	**0**			
5	**5**			

Table 4: Table for DTL Inverter

Signature