BRAC UNIVERSITY

Inspiring Excellence

Department of Computer Science and Engineering

Course Code: CSE260	**Credits: 1.5**
Course Name: Digital Logic Design	**Semester: Sum'18**

Experiment 04

Design and Implementation of parity generator and checker

I. Topic Overview:

In this lab student will get familiar with the idea of parity bit. They will learn how the parity bit works, how the circuit for parity bit generation can be designed and how they can be implemented.

II. Lesson Fit:

Students must have the knowledge of fundamental logic gates and their input/output characteristics.

III. Learning Outcome:

After this lecture, the students will be able to:

a. Understand how parity bit can be generated by logic circuit gate.

b. Implementation of parity bit generator and the parity bit checker.

IV. Anticipated Challenges and Possible Solutions

a. Finding out the Boolean expression for parity bit generator and checker.

Solutions:

Understanding the lecture given in the lab to find the expression for parity bit generator and checker

V. Acceptance and Evaluation

Students will show their progress as they complete each step of the problem. They will be marked according to their lab performance. Students have to show the outputs and proper connections for the given problem. Otherwise, full marks will not be given.

VI. Activity Detail

a. **Hour: 1**

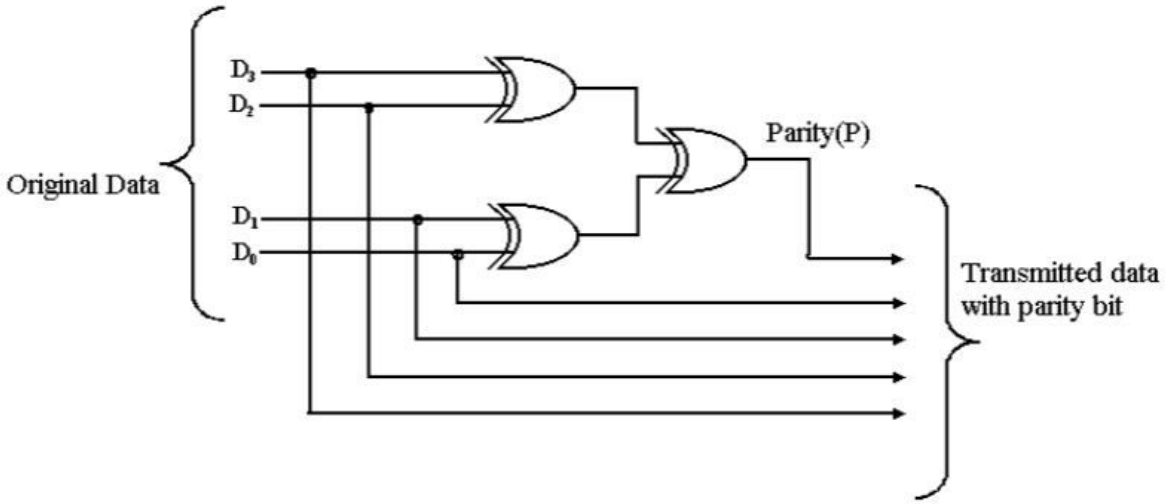
Discussion: parity bit generator and checker

Required Components and Equipments

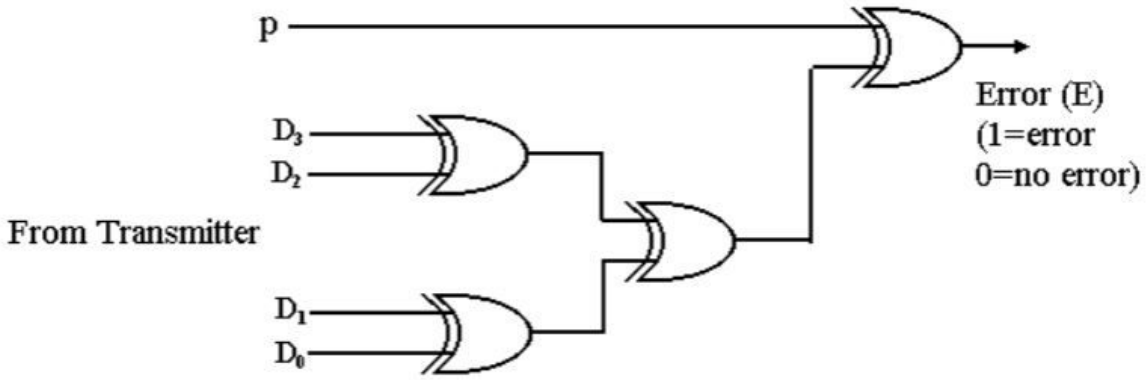
1. AT-700 Portable Analog/Digital Laboratory
2. 74003

Diagram of Circuit:

Even Parity generator



Even Parity Checker



Procedure:

- Construct the Circuit of Figure 1, on the breadboard of AT-700.
- Remember each IC's pin 14 connected to "+5V" position of DC Power Supply of AT-700, and pin 7 connected to "GND" position.
- Connect the inputs to Data switches and outputs to any position of LED Display.
- Determine the parity generator's output for each of the following sets of input data,

$D_3D_2D_1D_0$; (a) 0111; (b) 1001; (c) 0000; (d) 0100

Determine the parity checker's output for each of the following sets of data from the transmitter

P	D_3	D_2	D_1	D_0
0	1	0	1	0
1	1	1	1	0
1	1	1	1	1
1	0	0	0	0

b. **Hour: 2**

Students will implement the circuit of parity bit generator as instructed

Problem Task: Task 01

c. **Hour 3:**

Students will implement the circuit of parity bit checker as instructed

Problem task: Task 02

VII. Home tasks

a. Lab report of Experiment 04

Experiment 4 Activity List

Task 1: Implement parity bit generator on breadboard.

task 2: Implement parity bit checker on breadboard.