Cse 260

Lab Assignment-6

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Ans:

1. Name of the Experiment:
Implementation of 4-bit Magnitude Comparator.

2. Objective:
i) To investigate the rules of comparing two 4-bit numbers.
ii) To familiarize with the boolean functions of a magnitude comparator
iii) To implement the circuit for two 4-bit numbers.

3. Required Components and Equipments:
↳ Logic Gates (XNOR, AND-4, AND, NOR, AND-3).

↳ Inputs (using logicstate)

↳ LEDs (Blue or any other colors)

↳ Power Source / Ground.

4 Experimental Setup : (No need to draw ICs Configurations)

A = B

A3 A2 A1 A0
1 0 1 1

B3 B2 B1 B0
1 0 1 1

A	B	A xnor B
0	0	1
0	1	0
1	0	0
1	1	1

A_0 equal B_0 = A_0 xnor B_0.

A1 B1 = A1 xnor B1

A2 B2 = A2 xnor B2

A3 B3 = A3 xnor B3.

A equal B = A_0 xnor B_0 . A_1 xnor B_1 .
A_2 xnor B_2 . A_3 xnor B_3 .

$A3 \text{ xnor } B_3 = X_3$

A > B

A3 A2 A1 A0
1 0 1 1

B3 B2 B1 B0
0 0 1 1

A3 A2 A1 A0
1 1 0 1

B3 B2 B1 B0
1 0 1 1

A3 A2 A1 A0
1 1 1 1

1 1 0 1

A3 A2 A1 A0
1 1 1 1

1 1 1 0

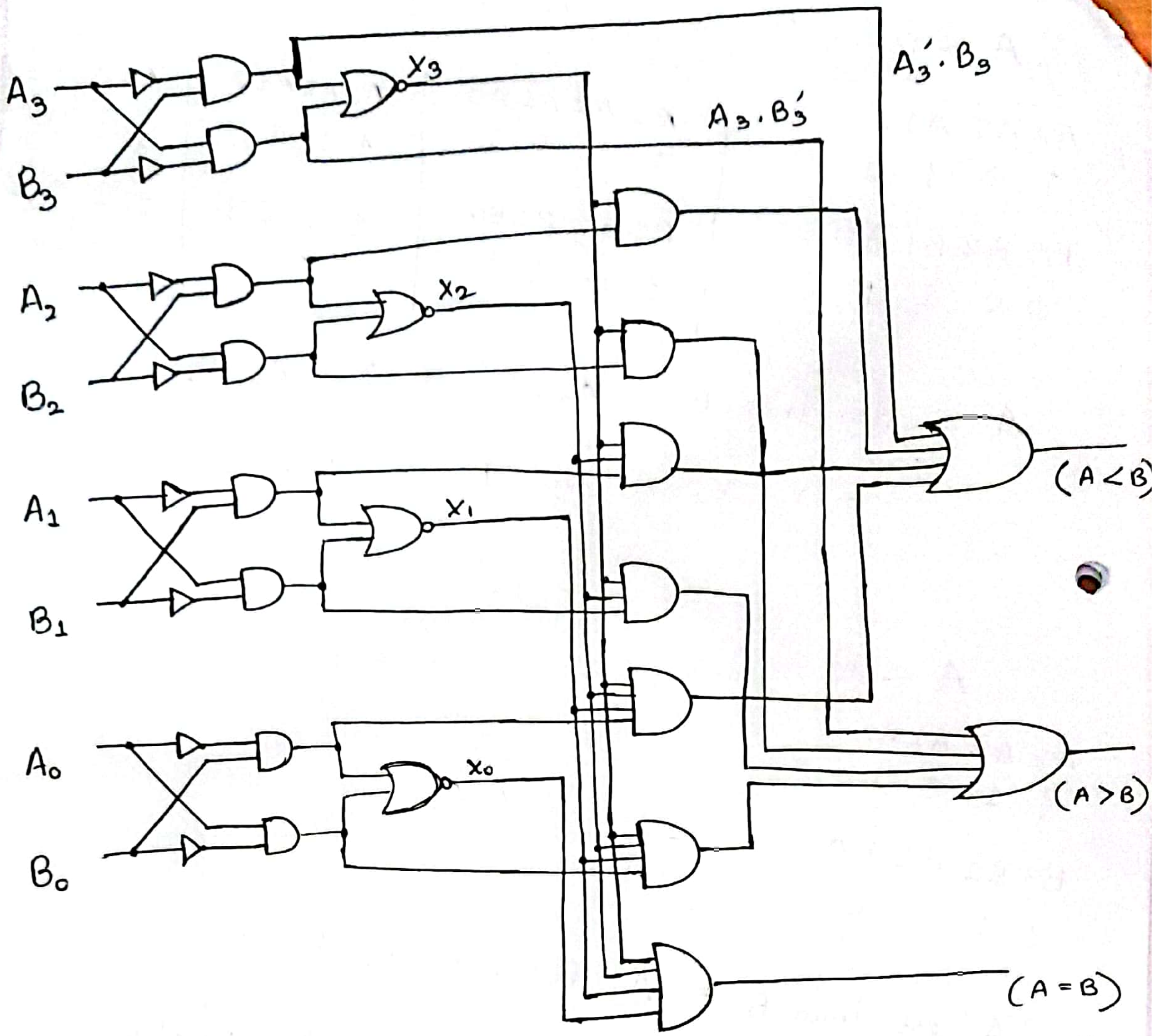
A greater than B $= A_3 . B_3' + X_3 . A_2 . B_2' + X_3 . X_2 . A_1 . B_1' + X_3 . X_2 . X_1 . A_0 . B_0'$

A < B

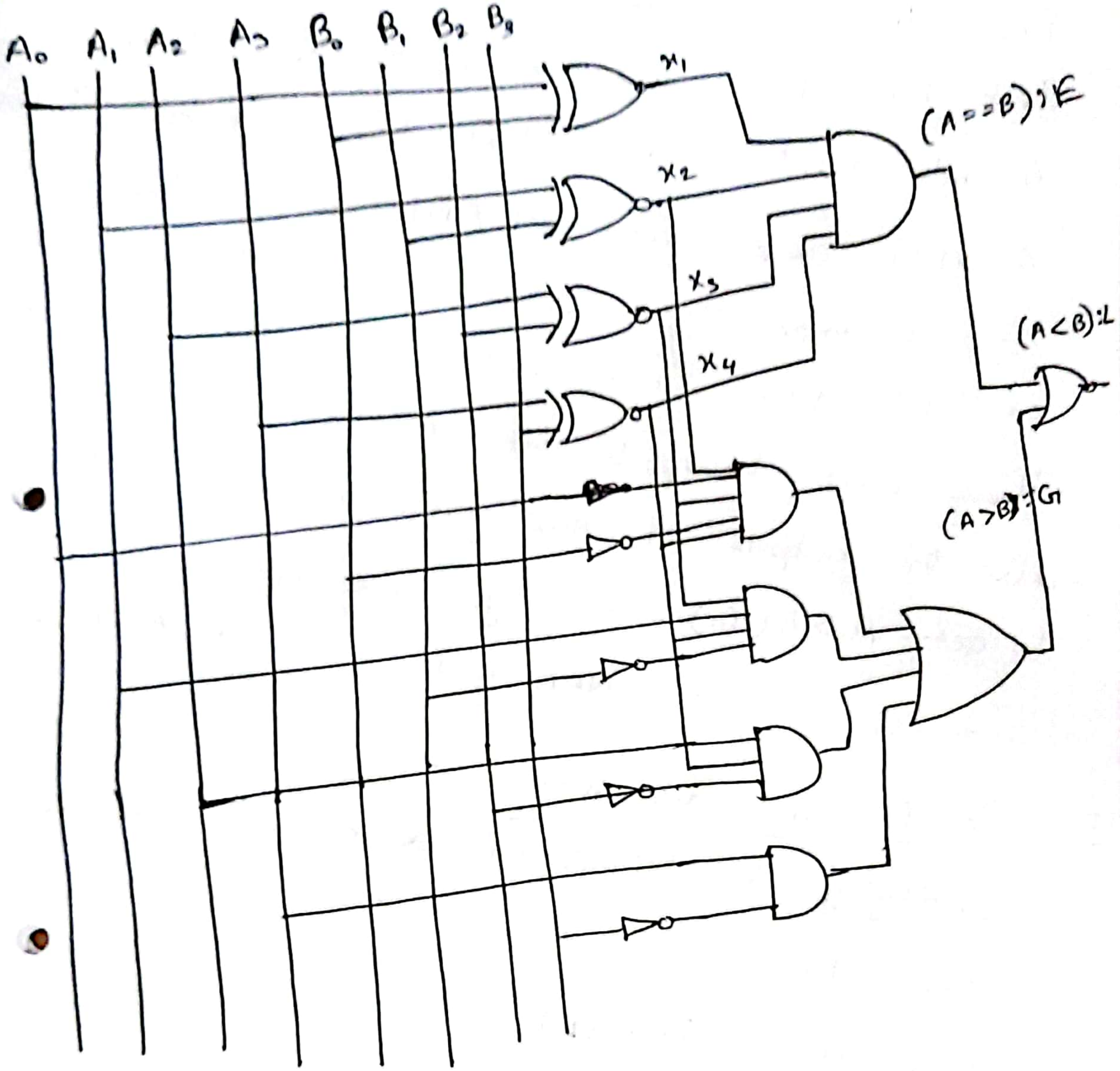
A3 A2 A1 A0
1 1 0 1

B3 B2 B1 B0
1 1 1 0

A less than B $= A_3' . B_3 + X_3 . A_2' . B_2 + X_3 . X_2 . A_1' . B_1 + X_3 . X_2 . X_1 . A_0' . B_0$


A3
B3
X3
A3'. B3
A3 . B3'
A2
B2
X2
A1
B1
X1
A0
B0
X0
(A<B)
(A>B)
(A=B)

OR



From the diagram we can see that, there have been taken all the inputs from two 4-bits number. After that, there was also taken 4. XNOR Gates and 4 AND Gates. Then, all of ~~them~~ these outputs we connected which we got from XNOR Gates with an AND Gate. These were taken to get A = B (E). After that, all the outputs of AND gates with an OR gate to get A > B (G). Finally, we connected E and G with a NOR gate to get A < B (L).

5 Results and discussion:

Justifying the designs of a 4-bit magnitude comparator.

1) For $A = B$, if: (E)

$A_1 = B_1$

$A_2 = B_2$

$A_3 = B_3$

$A_4 = B_4$

$(A_1 == B_1)$: $x_1 = A_1' B_1' + A_1 B_1 = A_1 \cdot B_1$ ~~OR $(A_2 == B_2)$~~

OR $(A_2 == B_2)$ $x_2 = A_2' B_2' + A_2 B_2 = A_2 \cdot B_2$

OR $(A_3 == B_3)$ $x_3 = A_3' B_3' + A_3 B_3 = A_3 \cdot B_3$

OR $(A_4 == B_4)$ $x_4 = A_4' B_4' + A_4 B_4 = A_4 \cdot B_4$

$\therefore (A == B) = x_1 \cdot x_2 \cdot x_3 \cdot x_4$

11) For $(A > B)$, if : (G)

$(A_4 = 1, B_4 = 0)$: $A_4 \cdot B_4'$ OR $(A_4 = B_4)$ and $(A_3 = 1, B_3 = 0)$

$\therefore x_4 \cdot A_3 \cdot B_3'$ OR $(A_4 = B_4)$ and $(A_2 = 1, B_2 0)$:

$x_4 \cdot x_3 \cdot A_2 \cdot B_2'$ OR $(A_4 = B_4)$ and $(A_3 = B_3)$

and $(A_2 = B_2)$ and

$(A_1 = 1$ and $B_1 = 0)$: $x_4 \cdot x_3 \cdot x_2 \cdot A_1 \cdot B_1'$

$$\therefore (A > B) = A_4 \cdot B_4' + x_4 \cdot A_3 \cdot B_3' + x_4 \cdot x_3 \cdot A_2 \cdot B_2' + x_4 \cdot x_3 \cdot x_2 \cdot A_1 \cdot B_1'$$

ii) For $(A<B)$ if : (L).

$(A_4=0,\ B_4=1): A_4'.B_4$ OR $(A_4=B_4)$ and

$(A_3=0,\ B_3\ 1): x_4.A_3\ B_3$ OR $(A_4=B_4)$ and

$(A_3=B_3)$. and $(A_2=0,\ B_2=1): x_4.x_3.A_2'.B_2$

OR $(A_4=B_4)$ and $(A_3=B_3)$ and $(A_2=B_2)$

and $(A_1=0,\ B_1=1): x_4.x_3.x_2.A_1'.B_1$

$$(A<B) = A_4'.B_4 + x_4.A_3'.B_3 + x_4.x_3.A_2'.B_2 + x_4.x_3.x_2.A_1'.B_1$$

The changes have ~~to~~ to be made to find the 3rd result in the circuit design.

$$(A==B): E = x_1.x_2.x_3.x_1$$

$$(A>B): G = A_4.B_4' + x_4.A_3.B_3' + x_4.x_3.A_2.B_2' + x_4.x_3.x_2.A_1.B_1'$$

$$(A<B): L = A_4'.B_4 + x_4.A_3'.B_3 + x_4.x_3.A_2'.B_2 + x_4.x_3.x_2.A_1'.B_1$$

Scanned with CamScanner

$\therefore (A < B) = E' . G' \Rightarrow L = (E + G)'$

Implement Using NOR Gate :-

A > B	A == B	A < B
0	0	1
0	1	0
1	0	0
1	1	Undefined