Department of Computer Science and Engineering

Course Code: CSE260	Credits: 1.5
Course Name: Digital Logic Design	Semester: Fall'18

Lab 08

How to Use Mux for Data Transmission

I. **Topic Overview:**

The students will familiarize themselves with the mux. They will understand how to use mux to transfer data. They will also learn how to make 2:1 mux from 4:1 mux.

II. **Lesson Fit:**

The lab will follow the theory class.

III. **Learning Outcome:**

After this lecture, the students will be able to:

a. Use mux

b. How to add multiple optional number in a same circuit with mux

IV. **Anticipated Challenges and Possible Solutions**

a. **Problem:** Student may not the understand function of the mux.

Solution: Explain the purpose of the mux.

b. **Problem:** Student may not understand how to use the selector to transfer data.

Solution: Explain the concept of the selector

c. **Problem:** Students may fail to map the mux into ic

Solution: Explain the mapping between the mux and the ic.

V. **Acceptance and Evaluation**

Students will show their progress as they complete each problem. They will be marked according to their class performance. Their maybe students who might not be able to finish all tasks, they will submit them later and give a viva to get their performance mark.

VI. Activity Detail

a. Hour: 1

Discussion:

Explain the mux, selector, and adder.

Problem Task: Set up mux with selector.

b. Hour: 2 & 3

Problem Task: Set up adder ic and connect the output of the mux to adder and show the final output.

VII. Home tasks

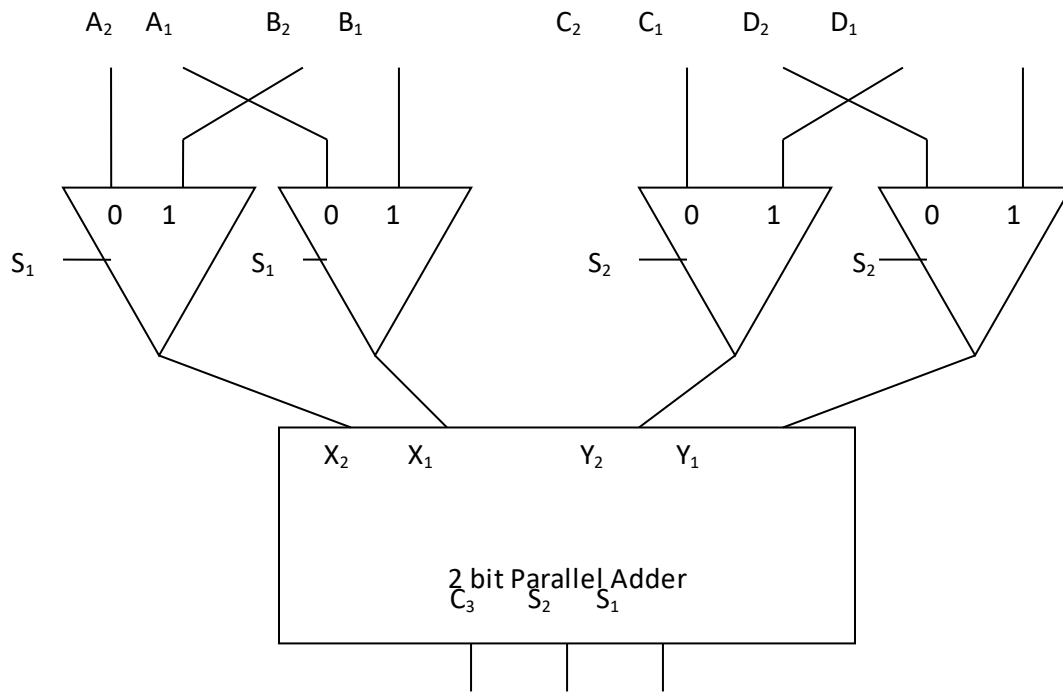a. Prepare a report based on the experiment.

Lab 08 Activity List

Design and Implementation of the following circuit:

Four 2 bit numbers A, B, C, D and two selection variables S_1 and S_2 are available. S1 will select either A or B and S2 will select either C or D. Depending on the two selection variables, the circuit will work in the following way.

S1	S2	Operation

0	0	A+C
0	1	A+D
1	0	B+C
1	1	B+D

A_2 A_1 B_2 B_1 C_2 C_1 D_2 D_1

0   1   0   1   0   1   0   1

S_1 S_1 S_2 S_2

X_2 X_1 Y_2 Y_1

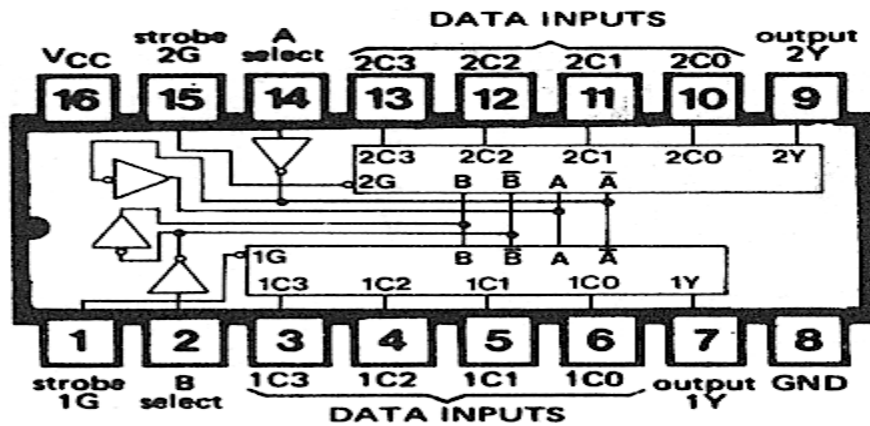2 bit Parallel Adder

C_3 S_2 S_1

IC: MUX (74153) Adder: 7483
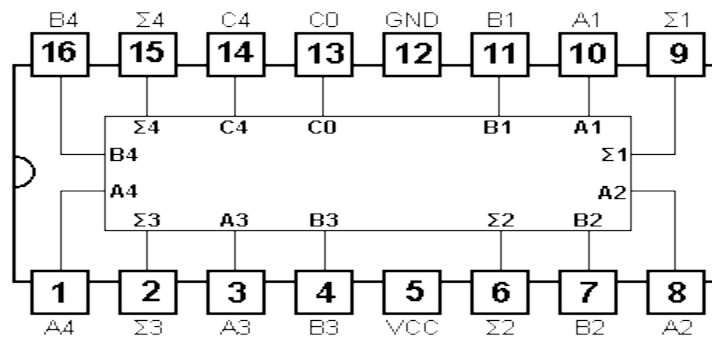
Report:

The report should cover the followings

1. Name of the experiment
2. Objective
3. Required Components and Equipments
4. Experimental Setup (i.e., diagram of the circuit)
5. Results and Discussions

a. Draw a circuit diagram which will compare three 4 bit numbers. You have Magnitude Comparators and 2:1 MUXs.

Mux 74153

Adder 7483

Set: C4 = C_{OUT}, C_0 =0

Strobe = Low

MUX Connection:

Make 4:2 Mux to 2:1 Mux in the following way

Short Selector A and B

Selector	Data Input (Active)	Output (1Y)	Output (2Y)
00	1C0, 2C0	1C0	2C0
11	1C3, 2C3	1C3	2C3

Give Inputs:

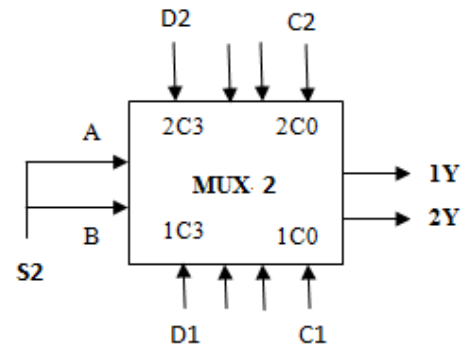First IC Connection: A = B= S1 (Selector)

1C0 → A1

1C3→ B1

2C0→ A2

2C3→ B2
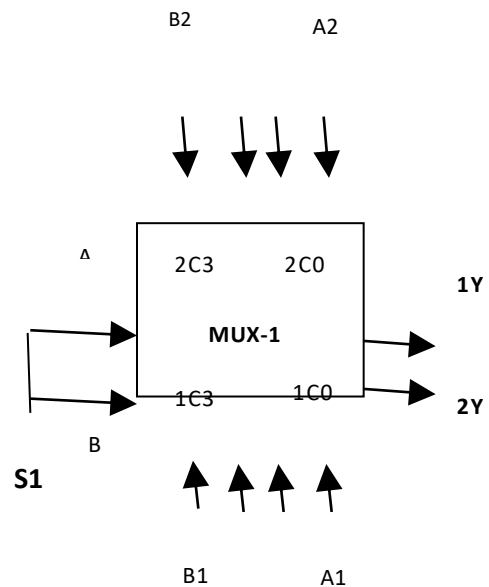
Second IC Connection: C = D = S2 (Selector)

1C0 → C1

1C3→ D1

2C0→ C2

2C3→ D2

Selector: S1	OUTPUT of MUX-1		Selector: S2	OUTPUT of MUX-2	
(First MUX)	**1Y**	**2Y**	(Second MUX)	**1Y**	**2Y**
0	A1	A2	0	C1	C2
0	A1	A2	1	D1	D2
1	B1	B2	0	C1	C2

1	B1	B2	1	D1	D2