Cse 260

Lab Assignment - 3

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Ans:

(1) Name of the Experiment:

Parity Generator and Checker

(2) Objective:

- To design and implement an Even parity Generator and Even parity checker using XOR gates (IC - 7486).

(3) Required Components and Equipments.

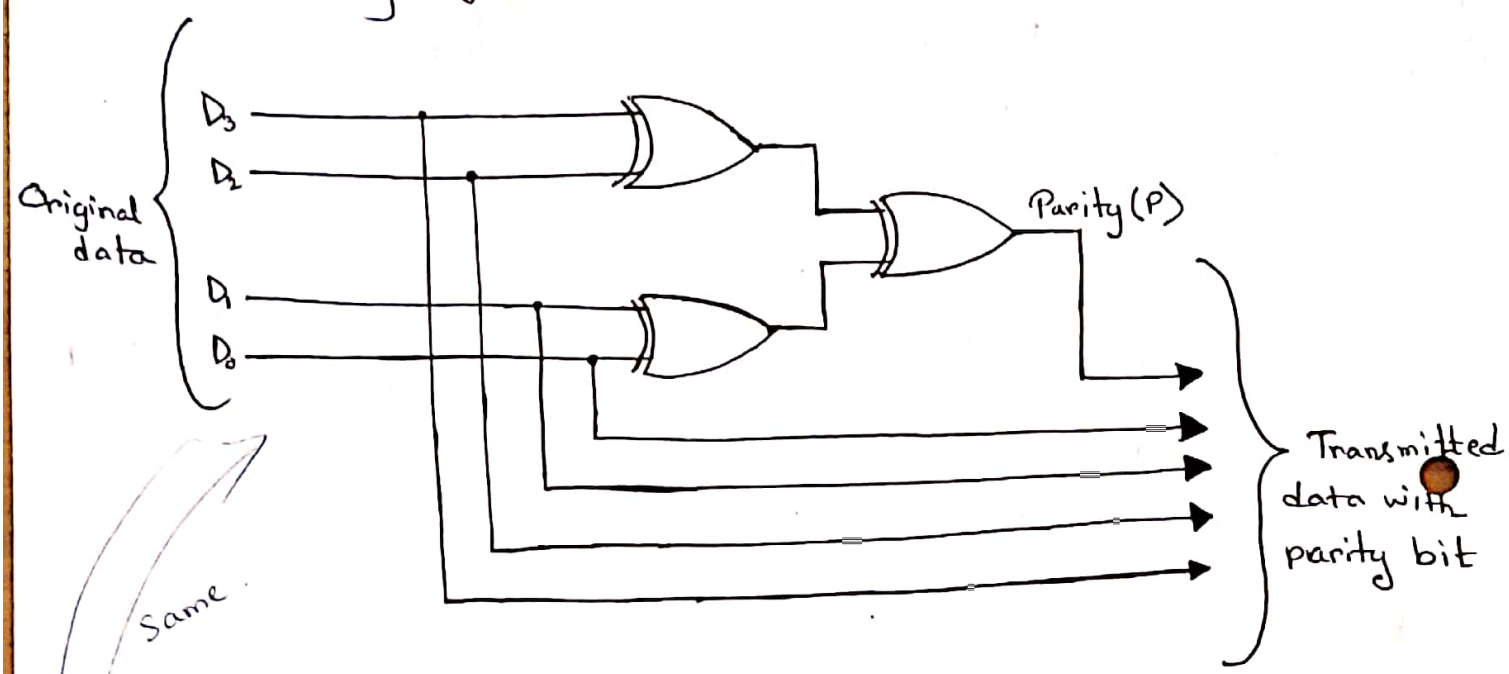
offline
1. AT-700 Portable Analog / Digital Laboratory.
2. 7400 x3.

1. Logic Gates (XOR gates mainly)
2. Inputs (using logic state)
3. LEDs (Blue and other colors)
4. Power Source.

Ans no:

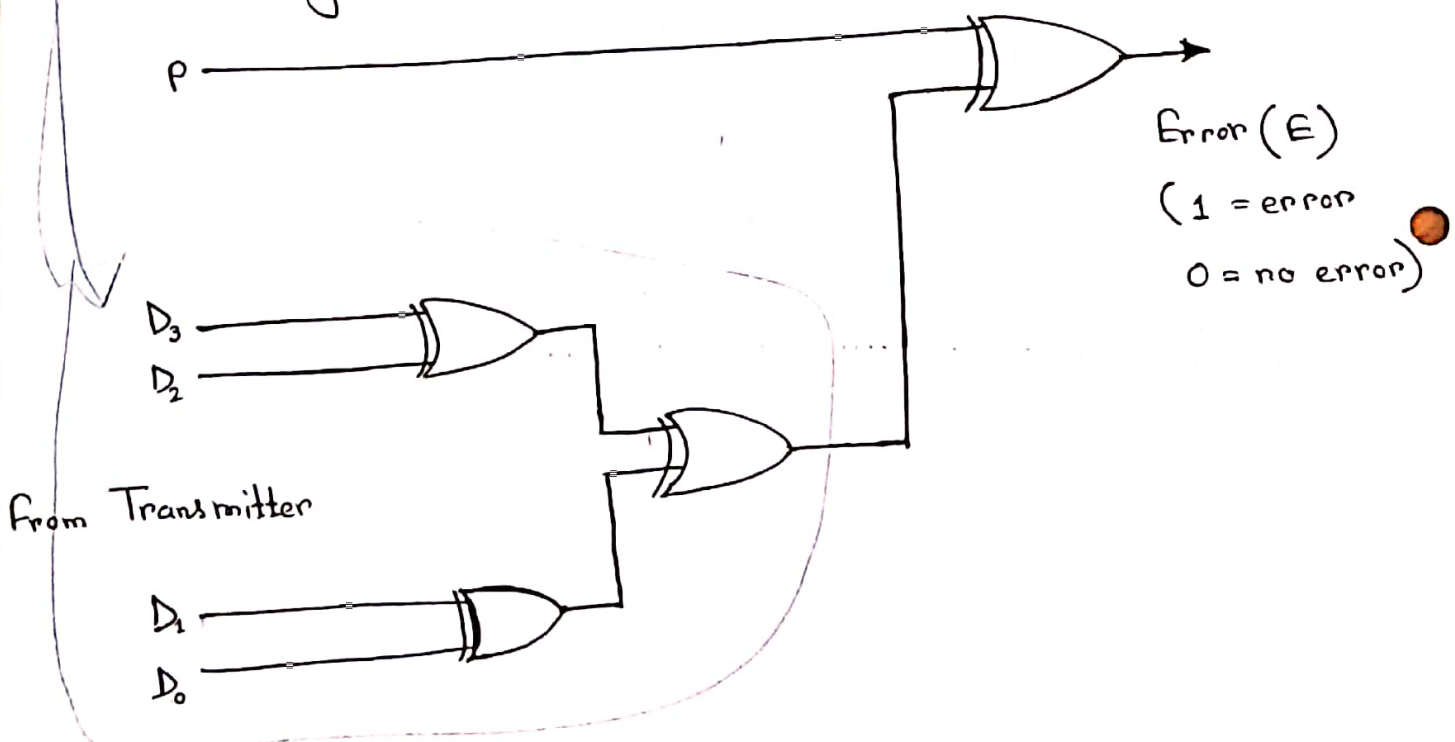
④ Experimental Setup:

Even Parity generator



Same

Even Parity Checker



Ans no:

(5) Results in Tabular form:

Even Parity generators outputs :-

	D_3	D_2	D_1	D_0	P → (output)
(a)	0	1	1	1	1
(b)	1	0	0	1	0
(c)	0	0	0	0	0
(d)	0	1	0	0	1

Even Parity checkers outputs :-

P	D_3	D_2	D_1	D_0	Error → (output)
0	1	0	1	0	0
1	1	1	1	0	0
1	1	1	1	1	1
1	0	0	0	0	1

Ans no:

⑥ Discussions (Explanation of the results):

Sender	P	Receiver	Error
0110	0	0111	

0111 [1] → 0111 [1] (1 ↔ 1) → no error

↳ to make even 1s

↳ if matches error = 0.

0111 [0] (1 ↔ 1) → 1 error

↳ if doesn't mach error = 1.

S	R	E
0	0	0
0	1	1
1	0	1
1	1	0

XOR

~~0101~~ [0]

- Even Parity generator takes inputs and generates a parity.

If even number of 1s, parity = 0, otherwise parity = 1, to make even number of 1s.

- At the receiver end, even parity checker checks the received parity from the sender with the parity generated again by the similar circuit. All of this is done using XOR gates.

Drawbacks - (Two)

	Sender	Receiver	
①	0111	0101	1 error, but cannot say where the error is.
②	0101 [0]	1111 [0] (0 ↔ 0)	0 error, but actually there is error (1 bit change can be detected, but not more than 1).