Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

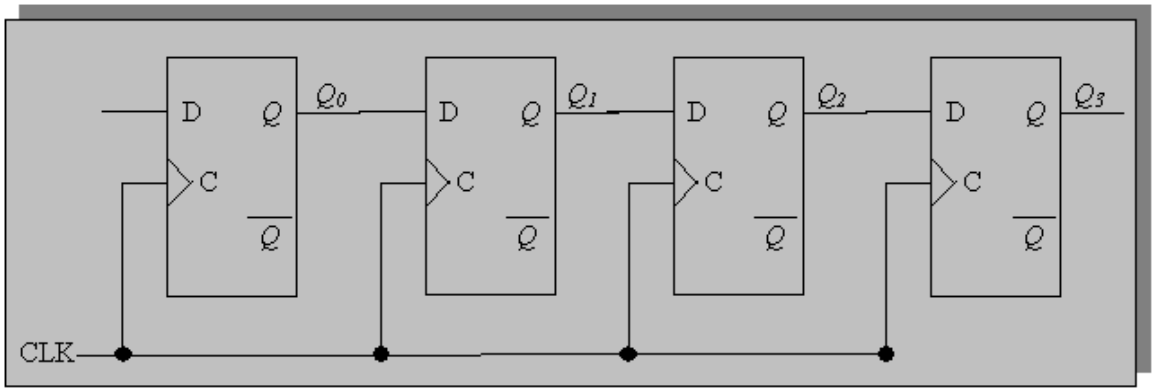
Experiment # 10

Data Transfer using Shift Register and Implementation Ring Counter.

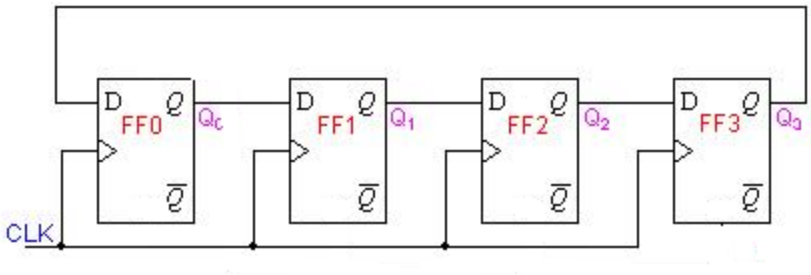
Register that is capable of shifting data one bit at a time is called a shift register. The logical configuration of a serial shift register consists of a chain of flip-flops connected in cascade, with the output of one flip-flop being connected to the input of its neighbor. The operation of the shift register is synchronous; thus each flip-flop is connected to a common clock. Using D flip-flops forms the simplest type of shift-registers.

You have undoubtedly seen shift registers in action in devices such as an electronic calculator, where the digits shown on the display shift over each time you key in a new digit. This is the same action, taking place in a shift register.

Figure shows the simplest possible shift register.



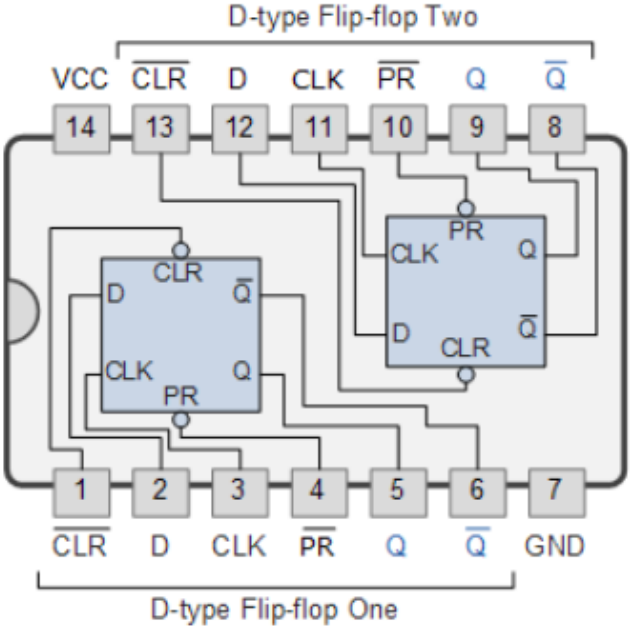
Ring Counter: A ring counter is basically a circulating shift register in which the output of the most significant stage is fed back to the input of the least significant stage. The following is a ***4-bit ring counter*** constructed from D flip-flops. The output of each stage is shifted into the next stage on the positive edge of a clock pulse.



Clock Pulse	Q3	Q2	Q1	Q0
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	1	0	0	0

1. **Implement a 4-bit shift register using D- latch.**
2. **Implement a Ring Counter using this 4-bit shift register.**

74LS74 Dual D-type Flip Flop



Report:
The report should cover the followings

1. Name of the Experiment
2. Objective
3. Required Components and Equipments
4. Experimental Setup (No need to draw the IC configurations)
5. Results and Discussions .The discussions part must include the answers of the following questions:

    - What is the difference between a register and a latch?
    - In your design which operation you went for – parallel or serial operation?
    - What are the advantages of these two operations over one another?