Week-8 Cse260

Lab Assignment - 5

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Ans:

(1) Name of the Experiment:

Design and Implementation of 4-bit Parallel Binary Adder

(2) Objective:

To implement addition and subtraction together:

1. B1 xor C_0, B2 xor C_0, B3 xor C and B4 xor C_0.
2. Connect output from step 1 to the input of 7483 ICs B inputs.
3. Keep C_0 common for all steps.
4. Give $C_0 = 0$ to perform addition, $C_0 = 1$ to perform subtraction.

(3) Required Components and Equipments:

↳ IC 7486 (XOR)
↳ IC 7483 (4 bit parallel adder);
↳ XOR gates, AND gates, OR gates (Logic Gates)
↳ Inputs (using logic state)
↳ LEDs (Blue and other colors)
↳ Power Source. (Ground)

(4) Experimental Setup:

Figure 1: Half Adder Circuit

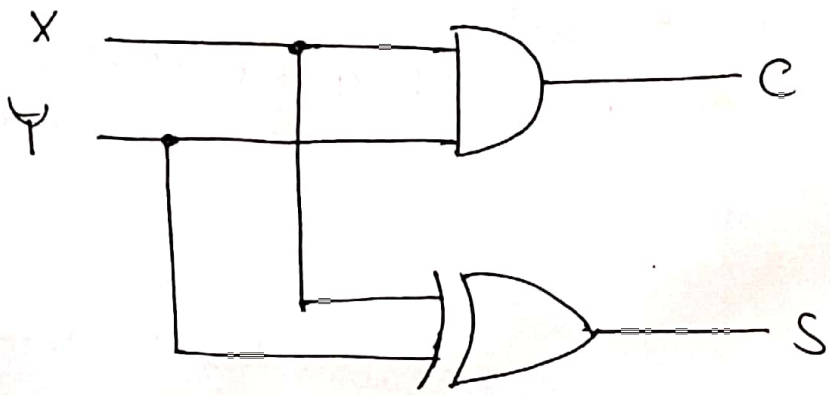
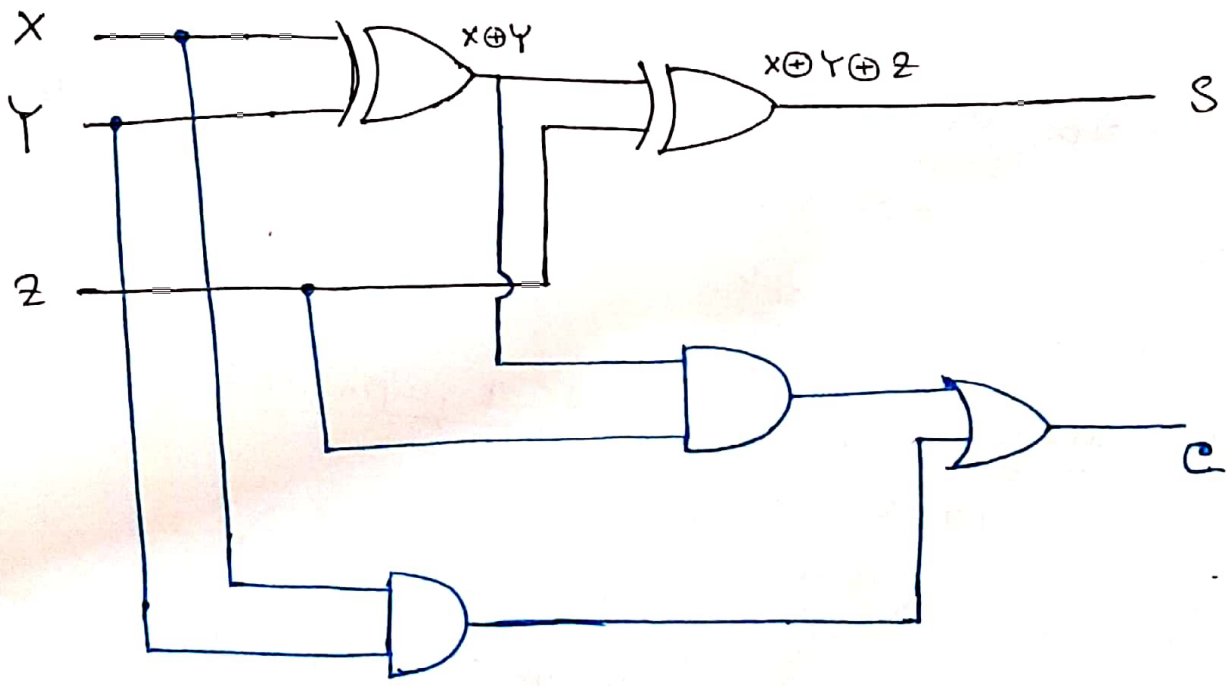


Figure 2: Full Adder Circuit



Full Adder = 2 Half Adders + 1 OR Gate.

(5) Results in Tabular Form

Truth Table of Half Adder: (2 bit)

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

- $C = XY$
  $S = X'Y + XY' = X \oplus Y$

Truth Table of Full Adder (3 bit):

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$C = X'YZ + XY'Z + XYZ' + XYZ$$

$$= Z(X'Y + XY') + XY(Z' + Z)$$

$$\Rightarrow \boxed{C = Z(X \oplus Y) + XY}$$

(5) → continuation.

$$S = X'Y'Z + X'YZ' + XY'Z + XYZ$$

$$= X'(Y'Z + YZ') + X(Y'Z' + YZ)$$

$$= X'(\underbrace{Y \oplus Z}_{A}) + X(\underbrace{Y \oplus Z}_{A})'$$

$$= X'A + XA' \quad \text{→ substitution}$$

$$= X \oplus A$$

$$= X \oplus (Y \oplus Z)$$

$$\Rightarrow \boxed{S = X \oplus Y \oplus Z}$$

(6) Discussion:

More ~~that~~ than 2 bits cannot be done in Half adder circuit.

For extra carry,

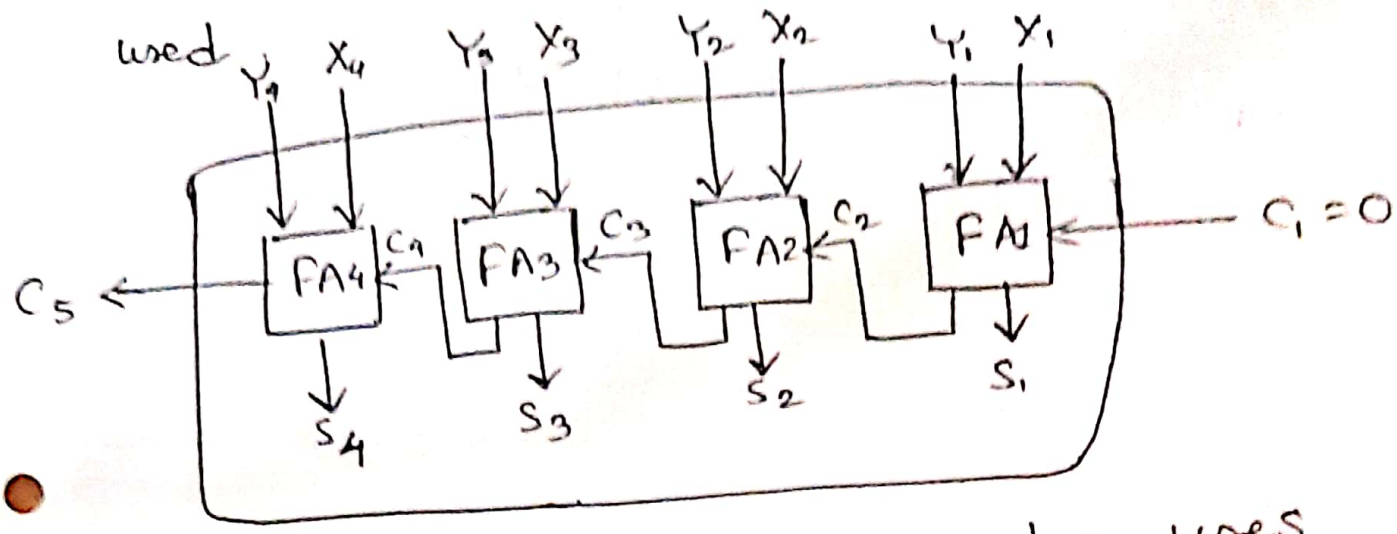
$$\begin{array}{r} \textcircled{1} \\ 1\ 1 \\ 1\ 1 \\ \hline 0 \end{array} \rightarrow c_1 = 0.$$

We need Full adder circuit, zero is added ~~in~~ in the 1st column to fully do it with full adder circuit.

Full Adder = 2 Half Adders + 1 OR Gate

→ continuation.

(10) In 4 bit Parall adder, 4 full adders are used



4 bit Binary Parallel Subtractor uses NOT gate (only for subtraction)

$X - Y = (+X) + (-Y)$

↳ not gate

↳ In 4bit Binary Parallel Adder / Subtractor, we use XOR gate as it produces invert output of one operand when the other operand is equal to 1.

X	Y	Output	
1	0	1	
1	1	0	(invert of Y)
0	1	1	(invert of Y)
0	0	0	

(10) → cont.

When $C_1 = 0$ (Adder)

When $C_1 = 1$ (Subtractor)