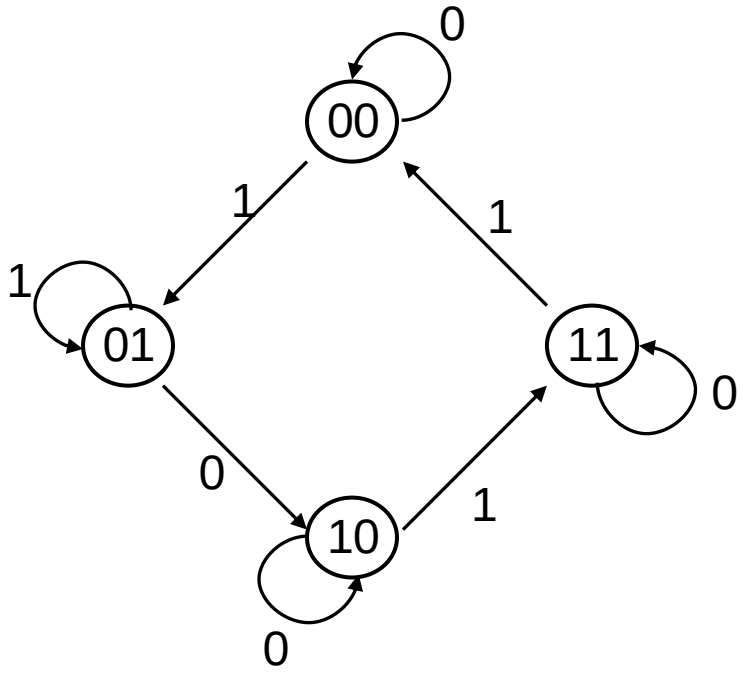
Department of Computer Science and Engineering
BRAC University
CSE 260: Digital Logic Design

Experiment # 9

Design a sequential circuit for the following state diagram with T flip-flops



Report:

The report should cover the followings

1. Name of the Experiment
2. Objective
3. Theory
4. Required Components and Equipment's
5. Experimental Setup (No need to draw the IC configurations)
6. Experimental Result and discussions.

Connections:

Use IC: 7476(JK flip flop) short j and k to make t
Pin: 2, 7 = Set High always [Connect from input switch]
Pin: 3, 8 = Set them 0 at first and then set to 1. [Connect from input switch]
x= comes from input.
TA = A'Bx' + ABx [2J = 2K] [Short]
TB = B'x + Ax + A'Bx' [1J = 1K] [Short]
[1CK = 2CK] [Short] clock pulse input [falling edge]
Connect: 1Q = B, 2Q = A to Led

NB: TA, TB obtained from Table 2.

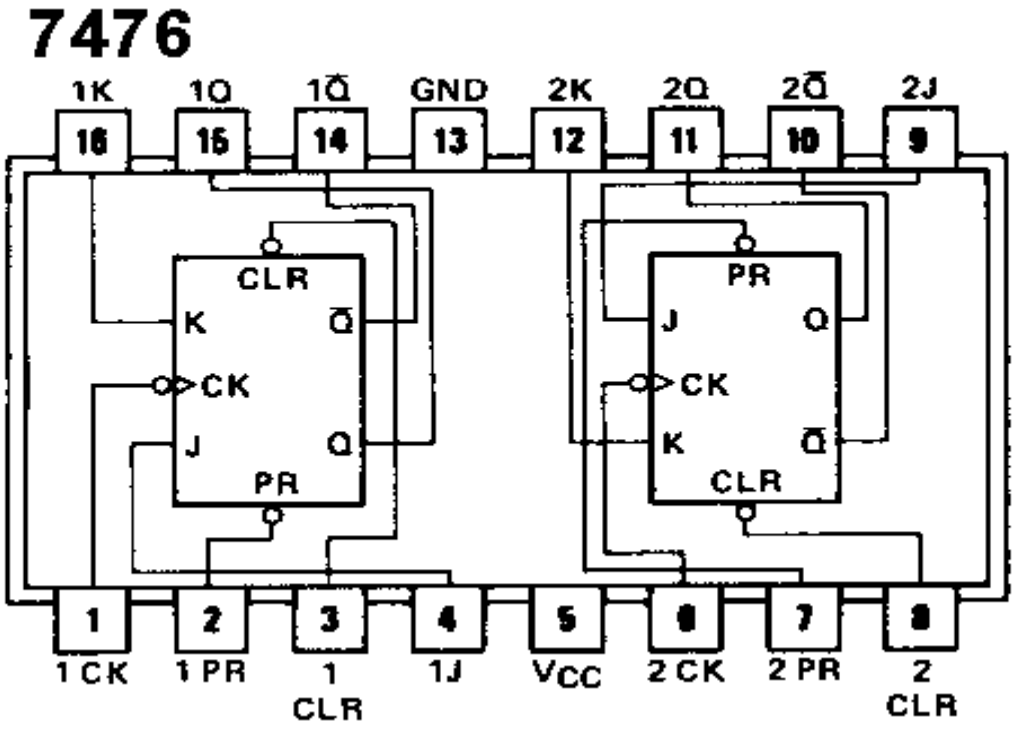


Table 1: Truth table of T Flip Flop

T	Q (Current State)	Q+ (Next State)
0	0	0
0	1	1
1	0	1
1	1	0

Table 2: Truth table of the given state diagram using T Flip Flop

Current State		Input	Next State		Input to the T FF to implement the state diagram	
A	B	x	A+	B+	TA	TB
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	0	0
1	0	0	1	0	0	0
1	0	1	1	1	0	1
1	1	0	1	1	0	0
1	1	1	0	0	1	1