CSE460: VLSI Design

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Section- 07

Lab Assignment 4

General guidelines

Draw the layout using the appropriate tool as taught in the lab, perform **DRC** and rectify all design errors (if any), submit the full screen screenshots of the design file and the simulation file **with proper discussion.**

Problem:
Draw the layout in ***microwind2*** for the logic function described the following equation:

$$Y = \overline{A.B + C}$$

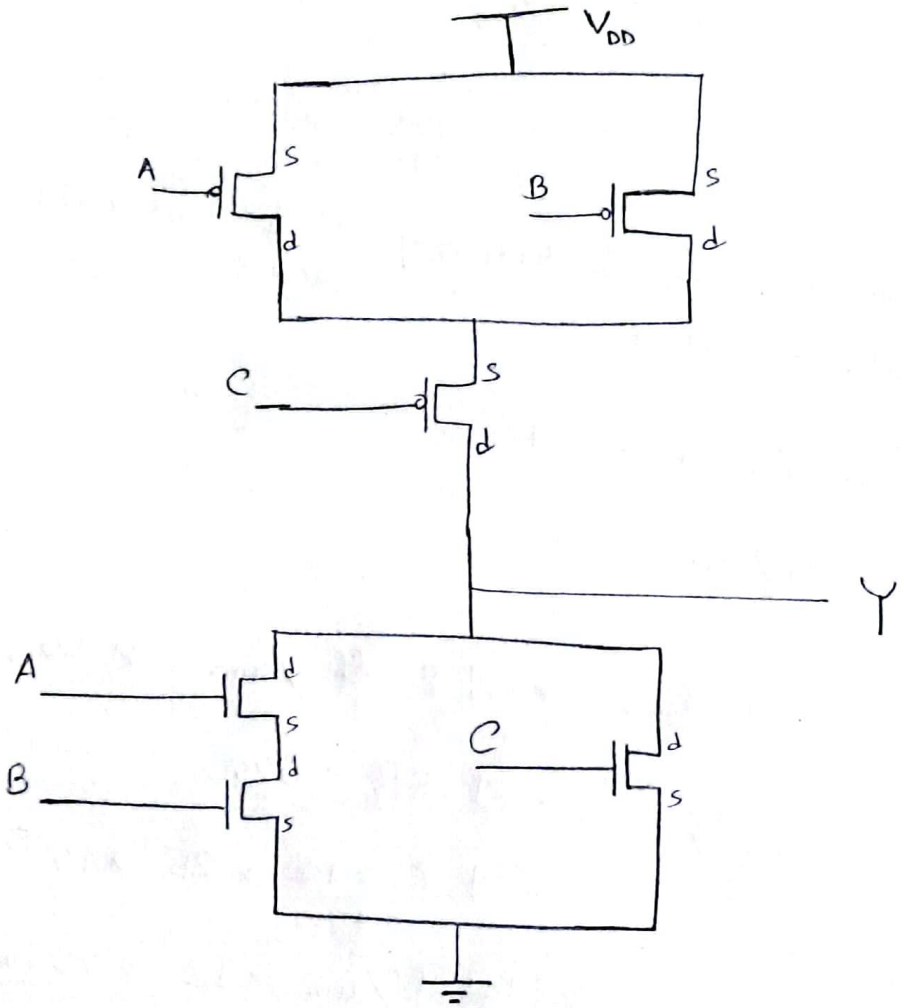
Answer:

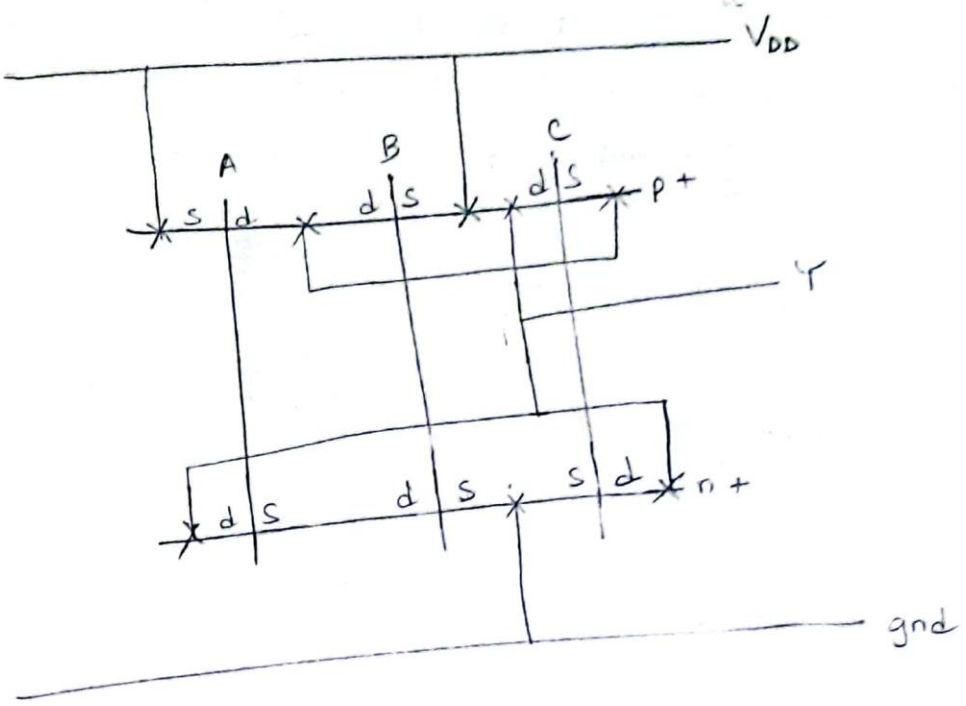
$$Y = \overline{A \cdot B + C}$$

AND OR

NOT

$(A + B)C$

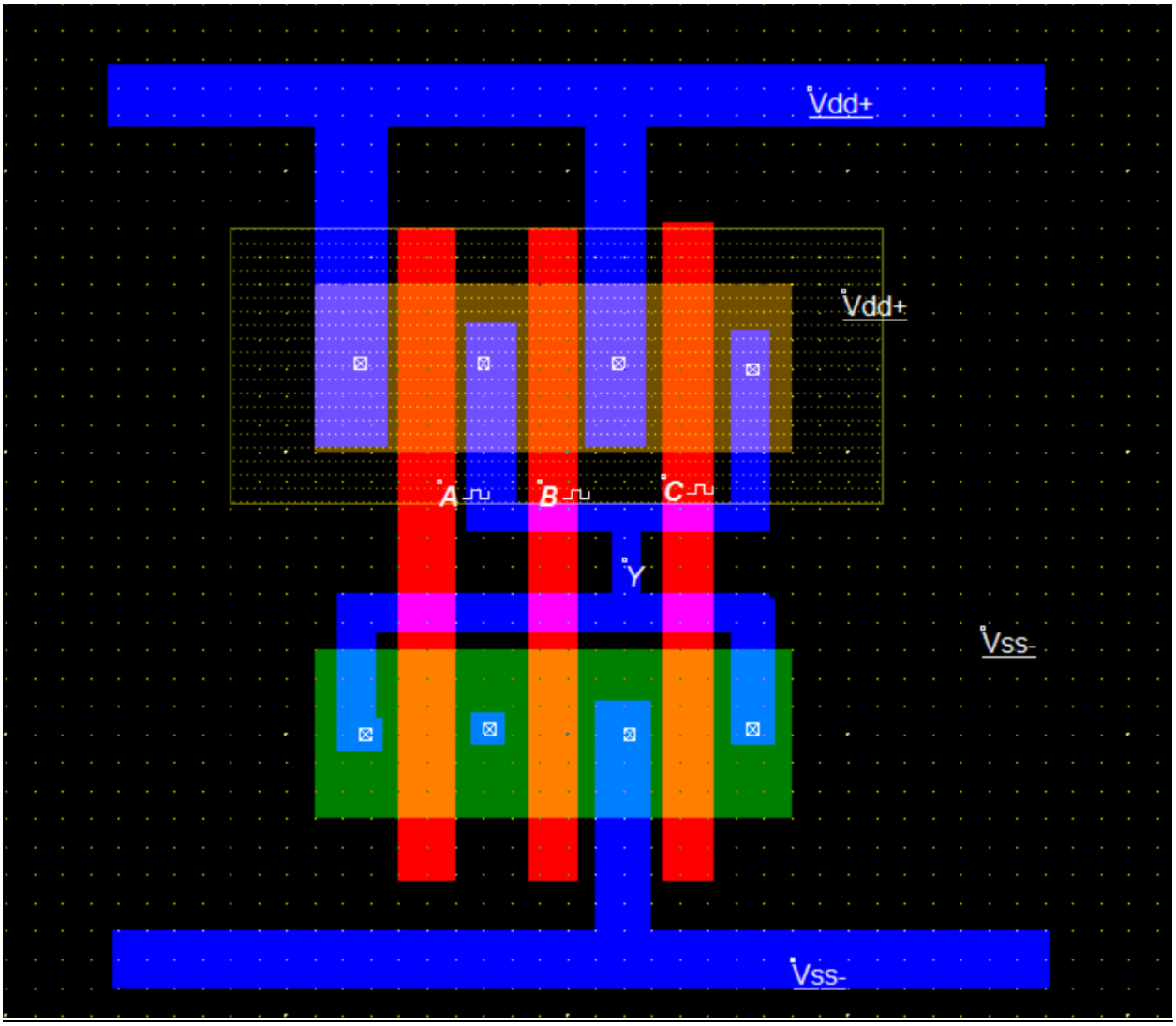




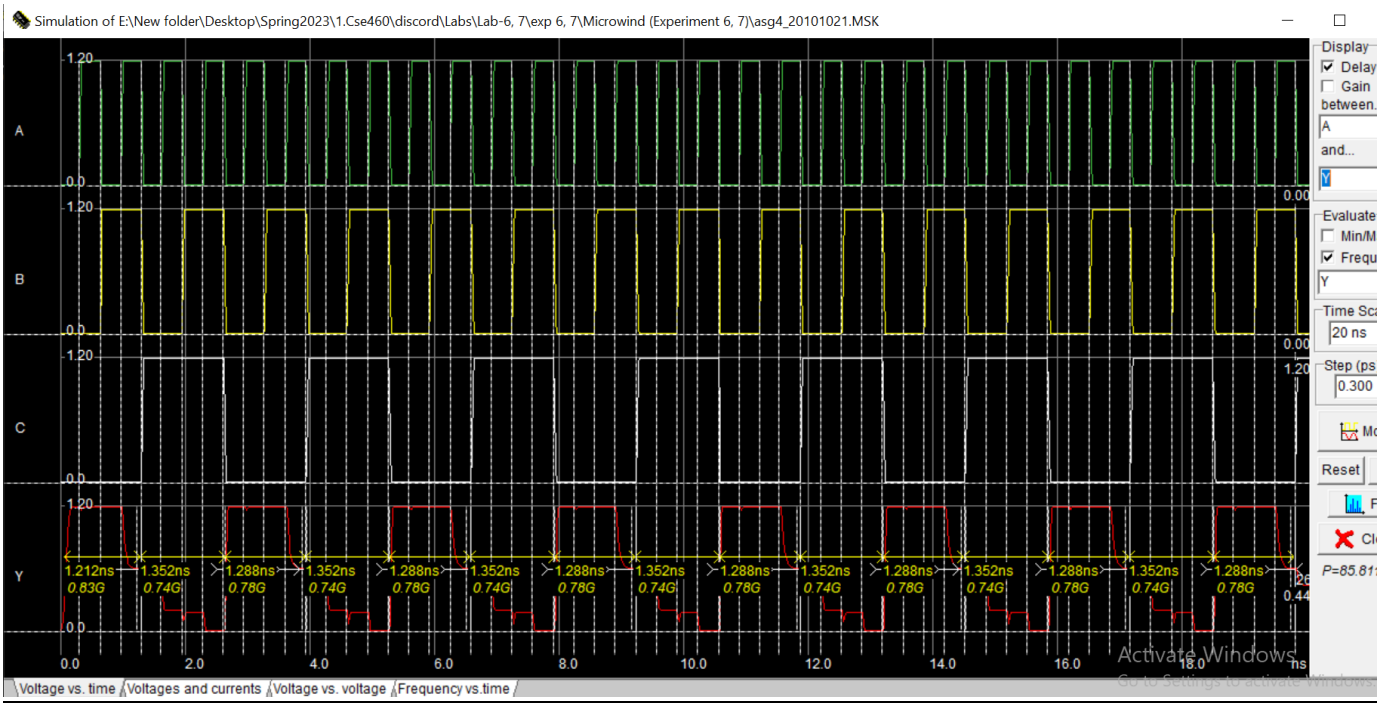
S|D S|D → series

S|D D|S → ~~parallel~~ parallel

Circuit in microwind2:



Simulation in microwind2:



Discussion:

Lab Assignment - 4

$$Y = \overline{A.B + C}$$

Truth Table:

A	B	C	Output, Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$A \cdot B = X$

AND

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

$X + C$

$AB + C = Z$

OR

X	C	Z	$\overline{Z}$ (Y)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Rearrangement according to Microwind Timing Diagram :

A	B	C	Output, Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0

If we observe closely, we can see that the above Truth table matches the timing diagram/simulation of microwind2 i.e., the timing diagram matches the output. When A=B=C=0, Output Y=1 and when A=B=C=1, Output Y=0 which match the table.