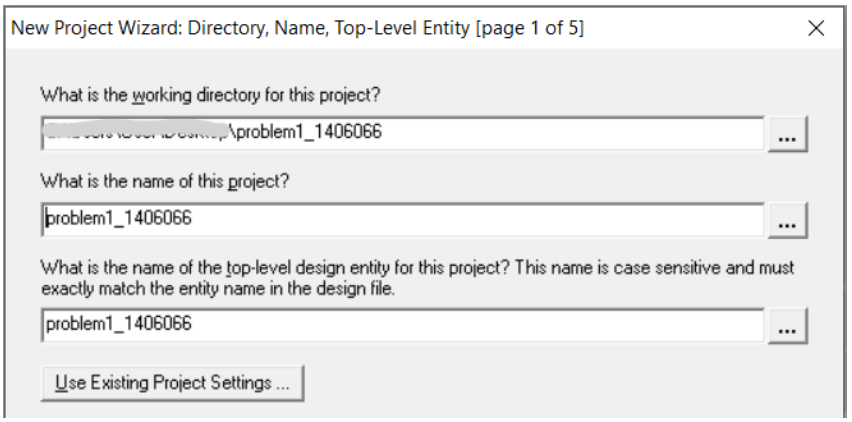
CSE460-7L: Assignment 1+2 (Spring 2021)

Assignment submission link: https://forms.gle/K2y1f2h2HEpCG85M7 (Online submission only)
Assignment submission deadline: **16 Feb, 2023, 11.59PM**

General guidelines

- Assignments are individual
- For each problem you will need to prepare 3 parts:
  1. *Code*: attach a screenshot or copy paste the code from .v file
  2. *Output*: **attach *FULL SCREEN* screenshots** of
     - Verilog code
     - Compilation Report - Flow Summary (Compilation report of the .v file)
     - Simulation Report - Simulation Waveforms (Simulation report of the .vwf file)

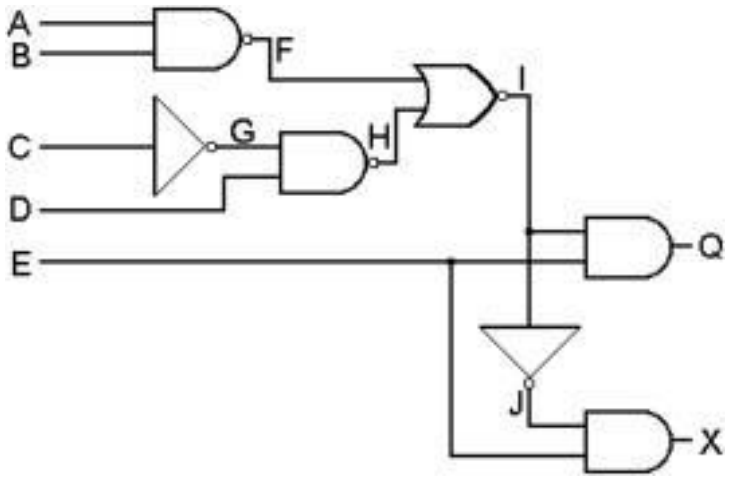
  [Tampered/edited/cropped screenshots will not be accepted.]
  3. *Discussion/Explanation*: explain the output waveforms/discuss what is asked
- Each problem will be of equal points. You will not be graded on the length/number of code/explanation/outputs; rather on the clarity, readability and precise explanations of your code/logic/outputs
- Points distribution for each problem is
  Code: 40%, *Output*: 20%, *Discussion/Explanation of output*: 40%
- **You will need to create separate directories/project for each problem**
- **The name of your working directory for each problem of the assignment should be …\problem#_StudentID [# = 1/2/3/4/5..]**
  For example, for problem 1 the name of the directory should be problem1_1406066



- Consequently, the name of your main module in the Verilog file should be problem#_StudentID [# = 1/2/3/4/5..]
  Continuing from the previous example, the name of the module should be problem1_1406066
- Finally, **compile all the problems for a given assignment into a single pdf file**
- The **name of the pdf should be Section_StudentID.pdf** (Example: 1_1406066.pdf)

Problems for Assignment 1

1. Write the verilog code (both **structural and behavioral**) of the following circuit and verify using a timing diagram. (to verify, you will first have to generate the truth table by hand first, and replicate every row of the table in the waveform simulation.)
   N.B. Q and X are the output.



2. Design a **8-to-1 MUX** (using 2-to-1 MUX and 4-to-1 MUX sub-circuits) and verify using a suitable timing diagram

Problems for Assignment 2

1. The truth table of a **priority encoder** for the priority of (w[3]>w[0]>w[1]>w[2]) looks like the following:

w[3]	w[2]	w[1]	w[0]	y[1]	y[0]
1	x	x	x	1	1
0	x	x	1	0	0
0	x	1	0	0	1
0	1	0	0	1	0

   Design a priority encoder of (w[3]>w[0]>w[1]>w[2]) using Verilog HDL and verify using a timing diagram.