CSE460: VLSI Design

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Section- 07

Lab Assignment 5

General guidelines

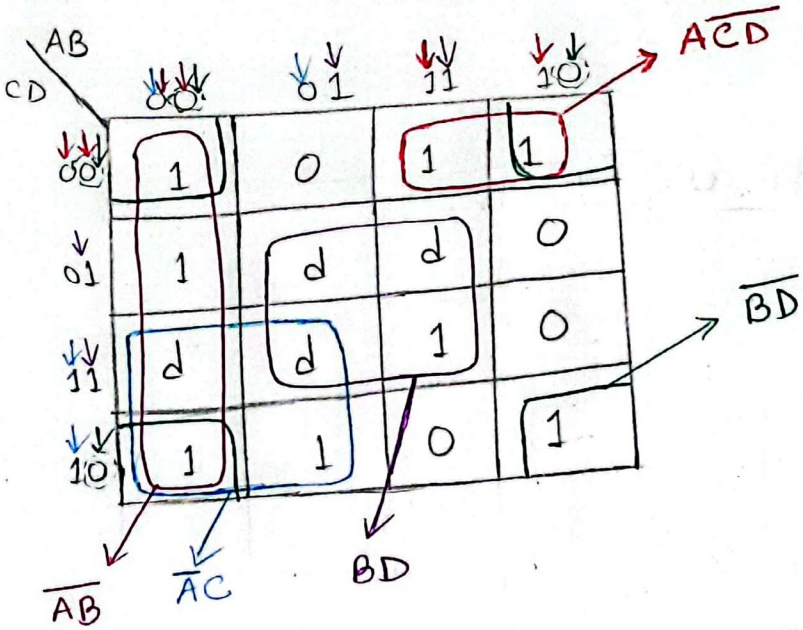
Draw the circuit using the appropriate tool as taught in the lab and rectify all design errors (if
any), submit the full screen screenshots of the design file and the simulation file **with proper
discussion.**

Problem:
Derive the Boolean logic expression from the following K-Map and implement the logic function
using CMOS technology. You may use blocks/sub-circuits made using CMOS technology but
cannot use readily available logic gates.

CD \ AB	00	01	11	10
00	1	0	1	1
01	1	d	d	0
11	d	d	1	0
10	1	1	0	1

Answer:

Lab Assignment - 05



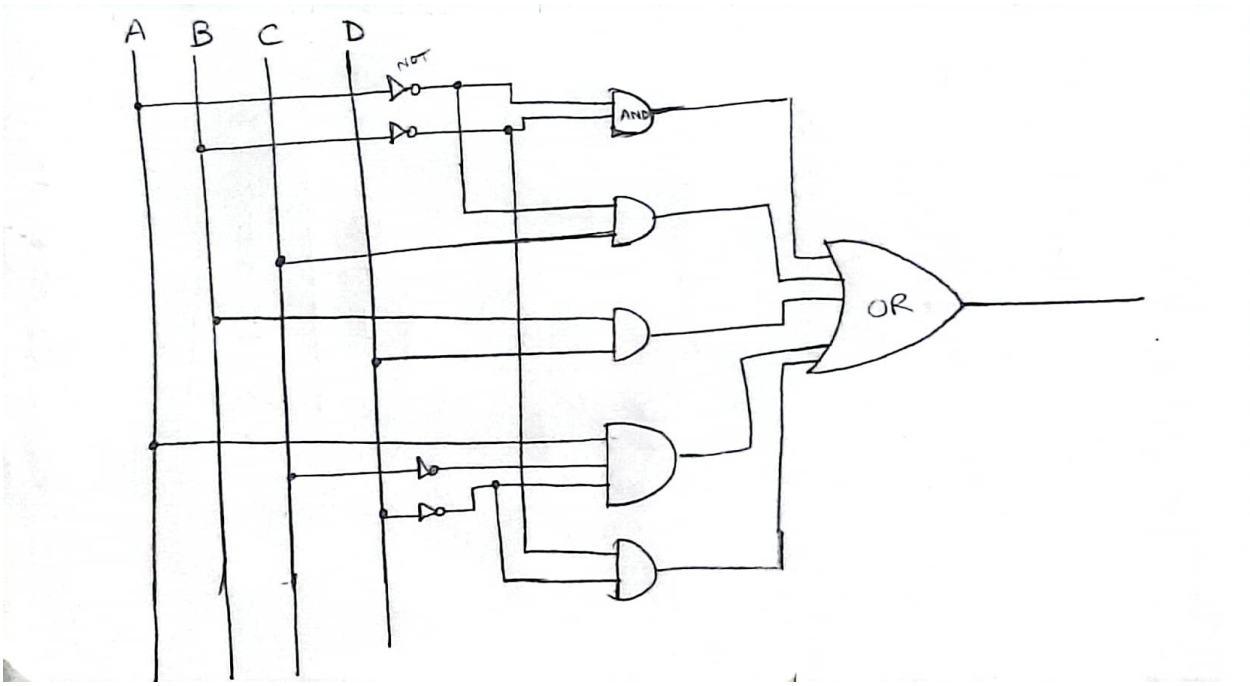
Minterm
SoP
Sum of Products

Minimization
↓
✓ not changing
included

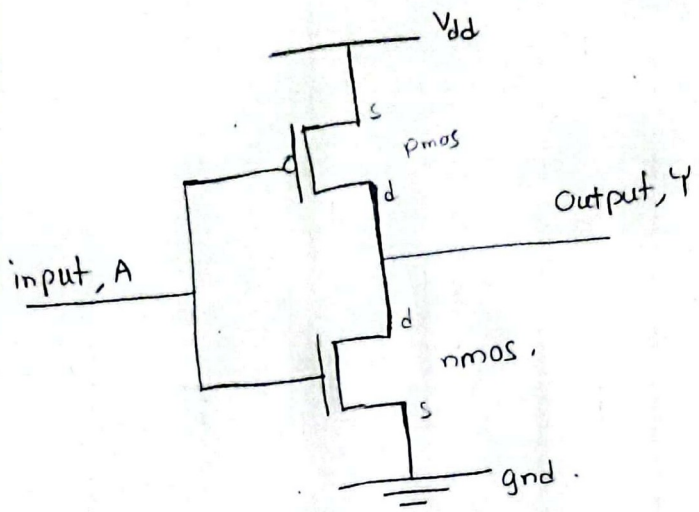
$2^0, 2^1, 2^2, 2^3$
1, 2, 4, 8

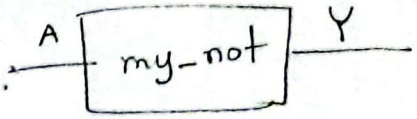
ignore
d } no definite
d } 1

$$Y = \overline{AB} + \overline{AC} + BD + \overline{ACD} + \overline{BD}$$

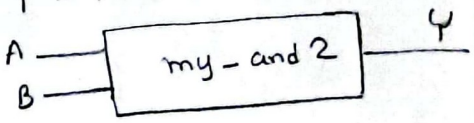

A
B
C
D
NOT
AND
OR

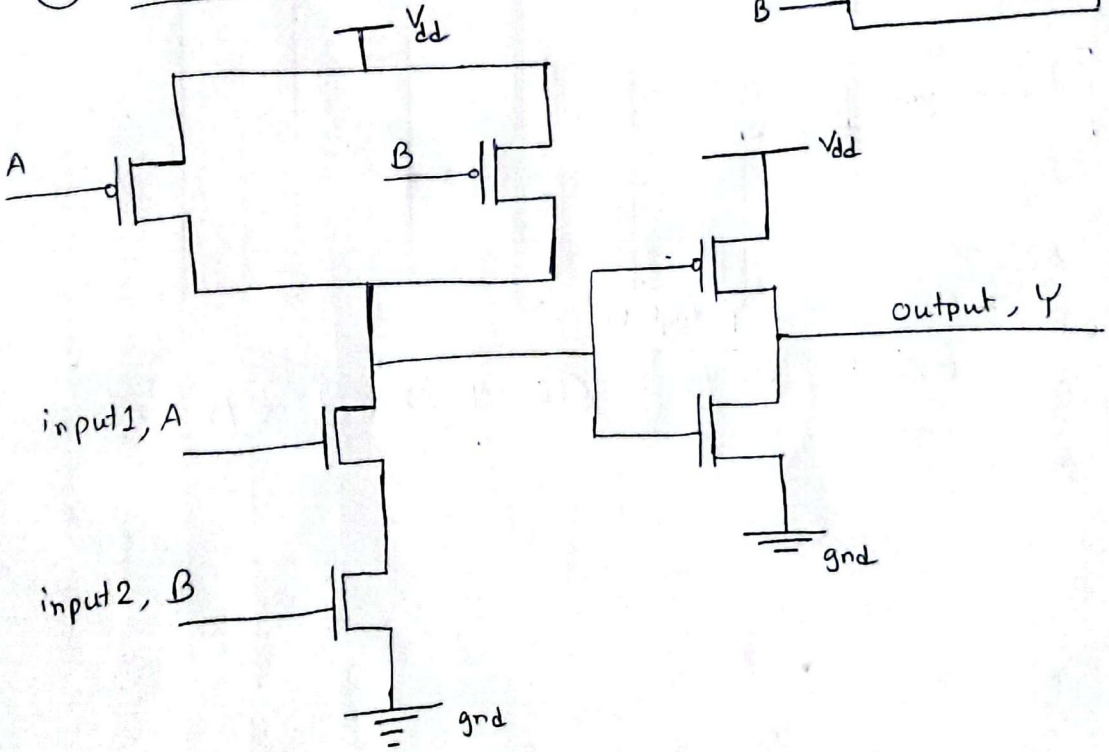
① CMOS Inverter $Y = \overline{A}$





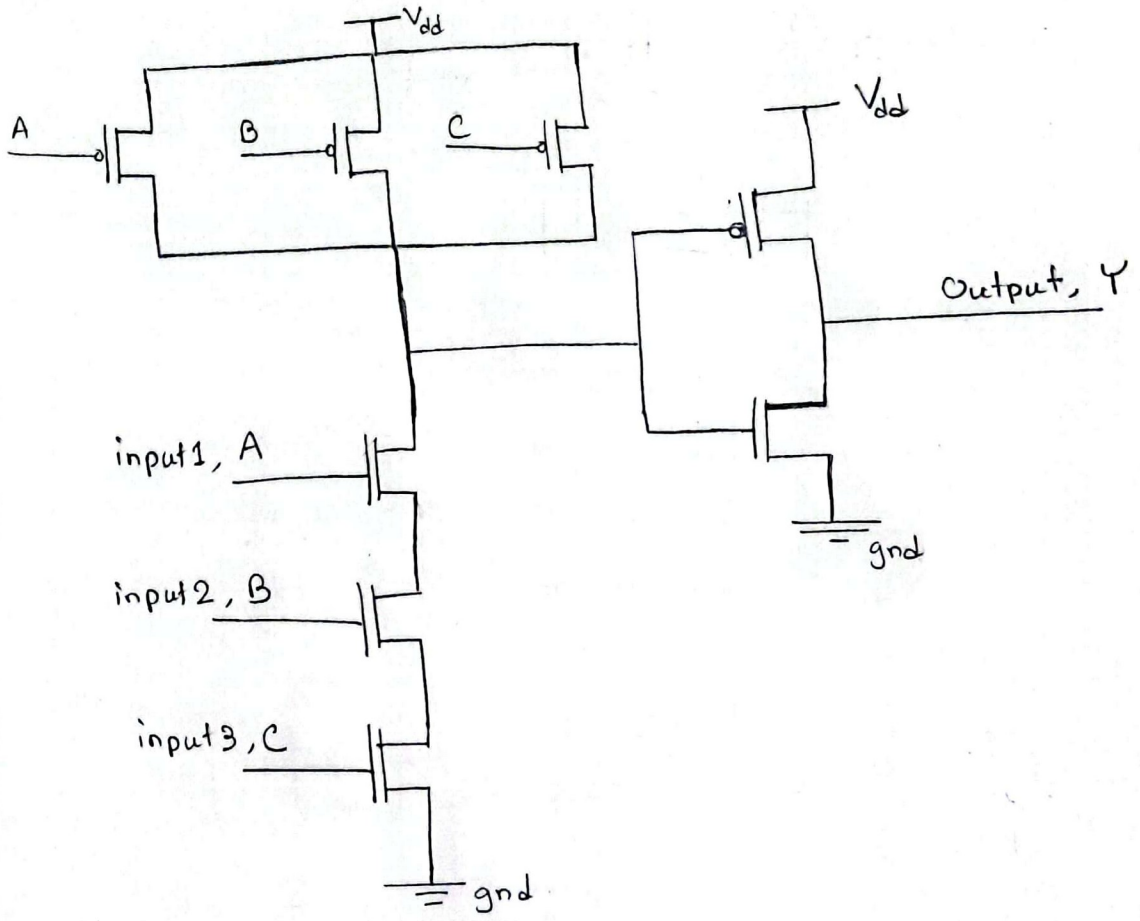
② 2-input CMOS AND gate, CMOS AND-2 $Y = A \cdot B$.

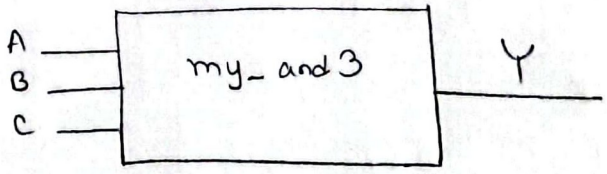


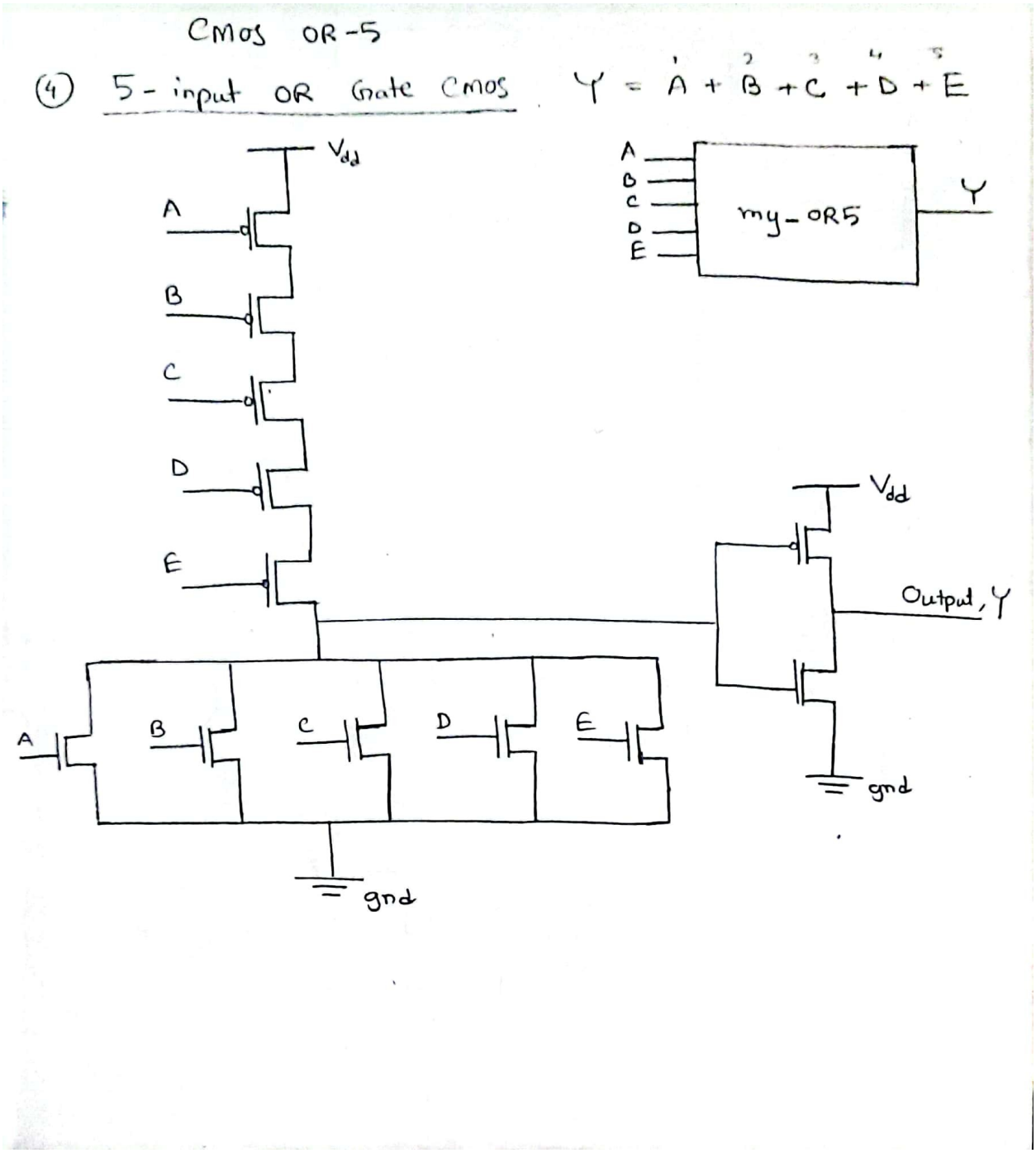


CMOS AND-3

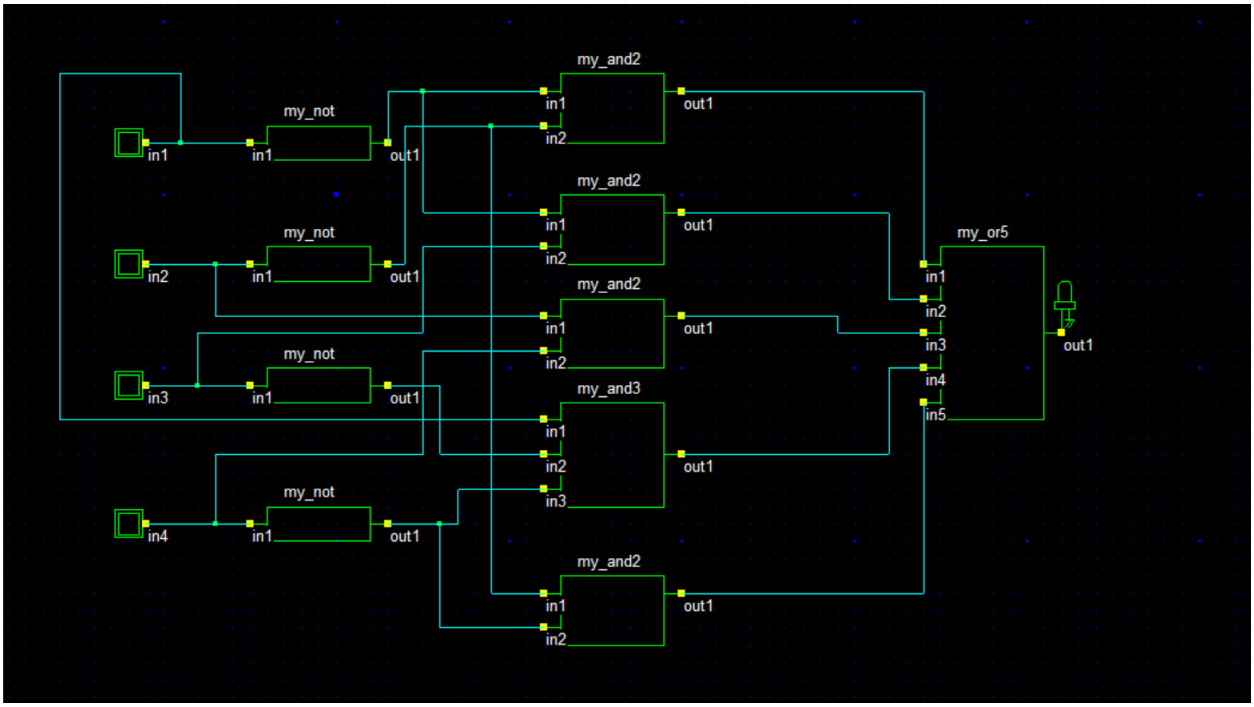
③ 3-input CMOS AND gate. $Y = A \cdot B \cdot C$



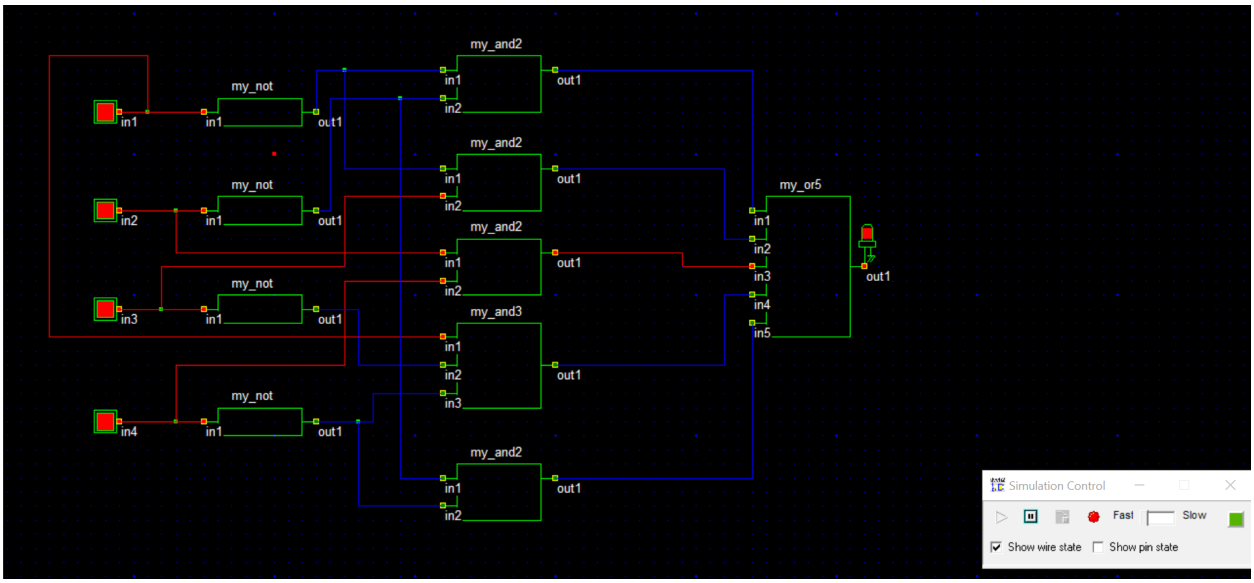




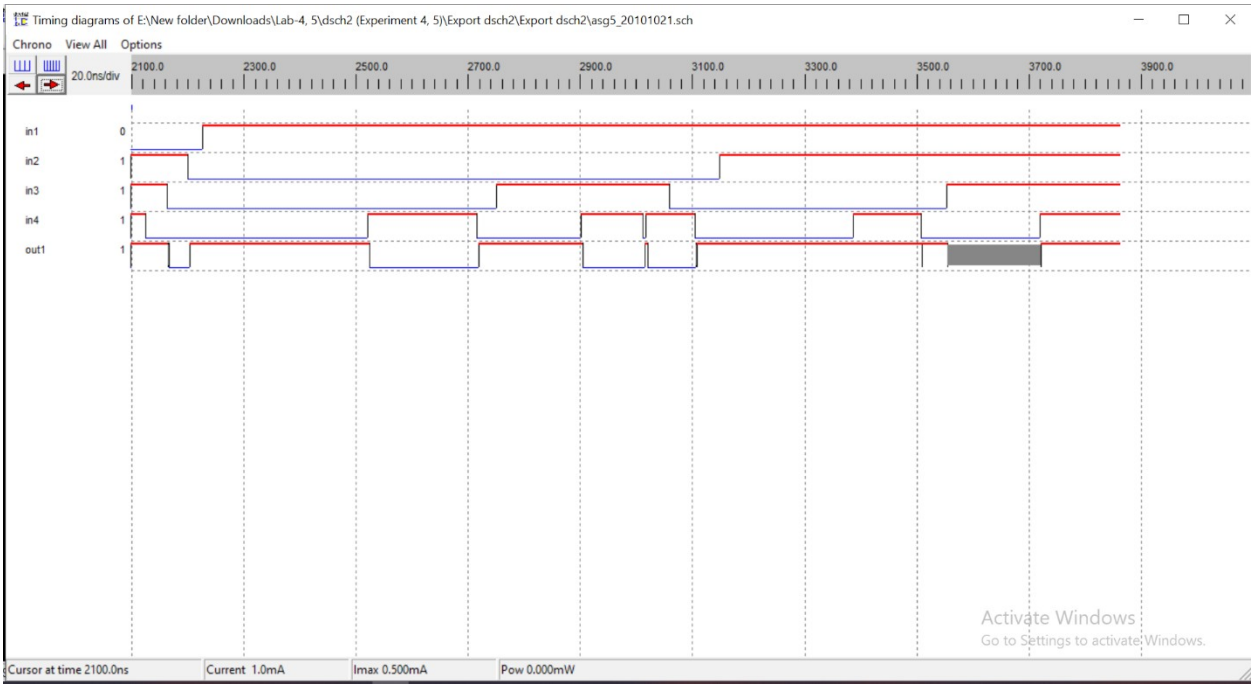
DSCH2 Design:



DSCH2 Simulation:



DSCH2 Timing Diagram:



Discussion:

Here, in the Timing Diagram, in1 = A, in2 = B, in3 = C, in4 = D and out1 = Y (or the output).

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$$Y = \underbrace{\overline{AB}}_{\text{Nand1}} + \overline{A}C + \underbrace{BD}_{\text{AND}} + A\overline{CD} + \underbrace{\overline{BD}}_{\text{Nand2}}$$

A	B	C	D	$\overline{AB}$	$\overline{A}C$	BD	$A\overline{CD}$	$\overline{BD}$	output Y
0	0	0	0	1	1	0	0	1	1
0	0	0	1	1	1	0	0	1	1
0	0	1	0	1	1	0	0	1	1
0	0	1	1	1	1	0	0	1	1
0	1	0	0	1	1	0	0	1	1
0	1	0	1	1	1	1	0	0	1
0	1	1	0	1	1	0	0	1	1
0	1	1	1	1	1	1	0	0	1
1	0	0	0	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	0
1	0	1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	1
1	1	0	1	0	1	1	1	0	1
1	1	1	0	0	0	0	1	1	0
1	1	1	1	0	0	1	0	0	1