CSE460: VLSI Design

Name- Ms Rodsy Tahmid
ID- 20101021
Section- 07

Lab Assignment 3

Question 1:

Write Verilog code for 1001 or 1111 pattern detector both

(a) as a Moore type FSM and
(b) as a Meal type FSM.

So, for each type of FSM, your report must contain the following:

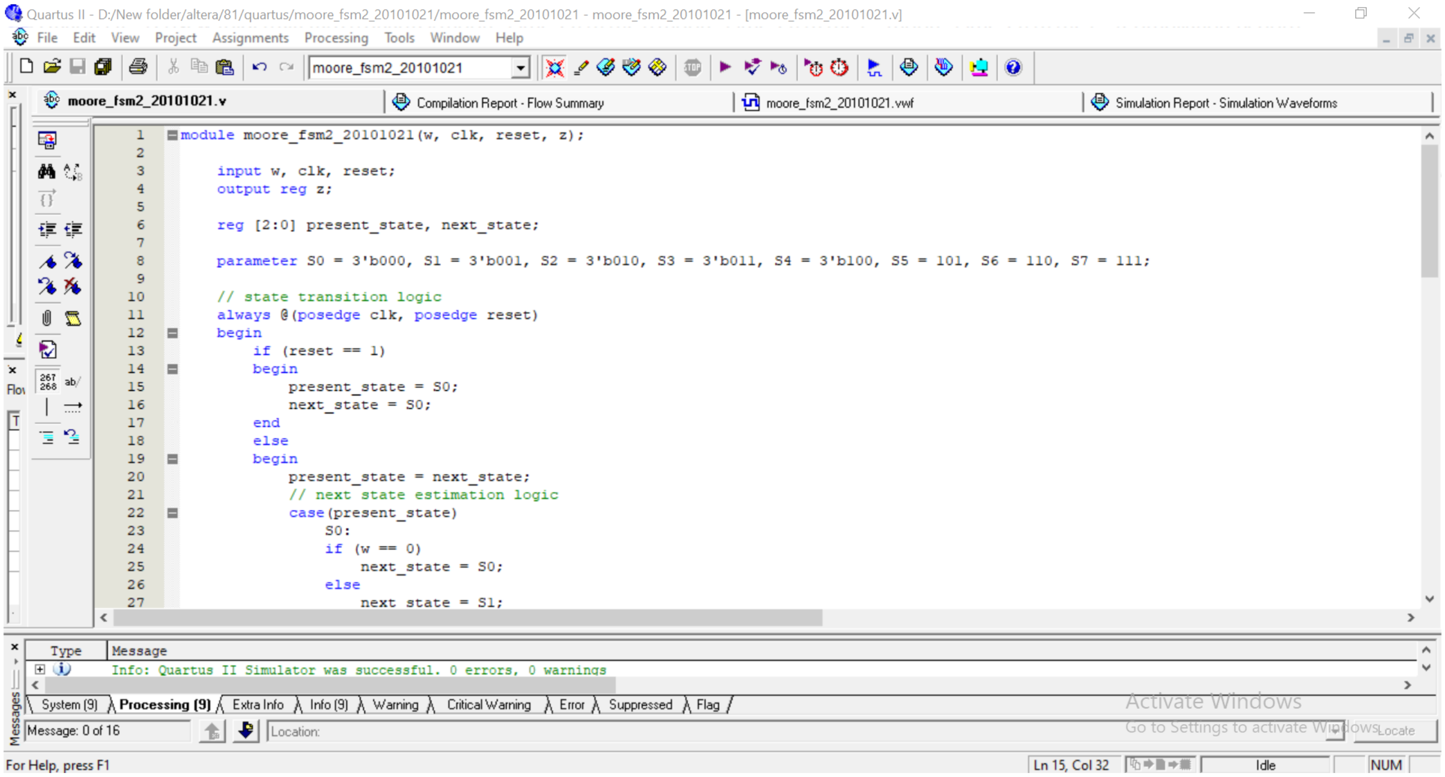
1. Screenshot of the Verilog Code
2. Screenshot of the timing diagram showing the patterns are detected successfully
3. Discussion and comments on the timing diagram.

[State Diagram are provided in the slide]

Answer:

Problem 1(a) – Moore FSM:

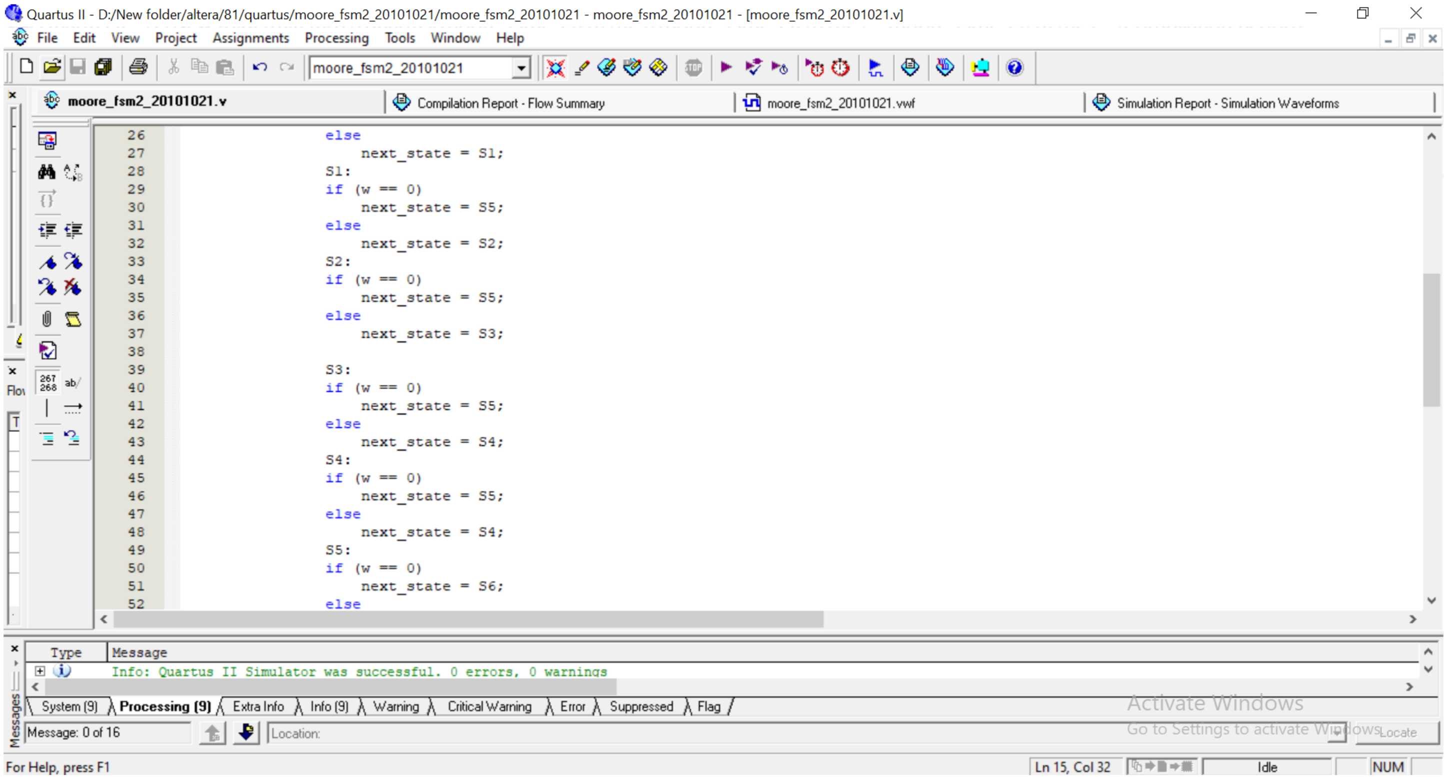
1. Screenshot of the Verilog Code



Quartus II - D:/New folder/altera/81/quartus/moore_fsm2_20101021/moore_fsm2_20101021 - moore_fsm2_20101021 - [moore_fsm2_20101021.v]
File Edit View Project Assignments Processing Tools Window Help
moore_fsm2_20101021
moore_fsm2_20101021.v
Compilation Report - Flow Summary
moore_fsm2_20101021.vwf
Simulation Report - Simulation Waveforms

```
module moore_fsm2_20101021(w, clk, reset, z);

    input w, clk, reset;
    output reg z;

    reg [2:0] present_state, next_state;

    parameter S0 = 3'b000, S1 = 3'b001, S2 = 3'b010, S3 = 3'b011, S4 = 3'b100, S5 = 101, S6 = 110, S7 = 111;

    // state transition logic
    always @(posedge clk, posedge reset)
    begin
        if (reset == 1)
        begin
            present_state = S0;
            next_state = S0;
        end
        else
        begin
            present_state = next_state;
            // next state estimation logic
            case(present_state)
                S0:
                if (w == 0)
                    next_state = S0;
                else
                    next_state = S1;
```

Type	Message
ⓘ	Info: Quartus II Simulator was successful. 0 errors, 0 warnings


Quartus II - D:/New folder/altera/81/quartus/moore_fsm2_20101021/moore_fsm2_20101021 - moore_fsm2_20101021 - [moore_fsm2_20101021.v]
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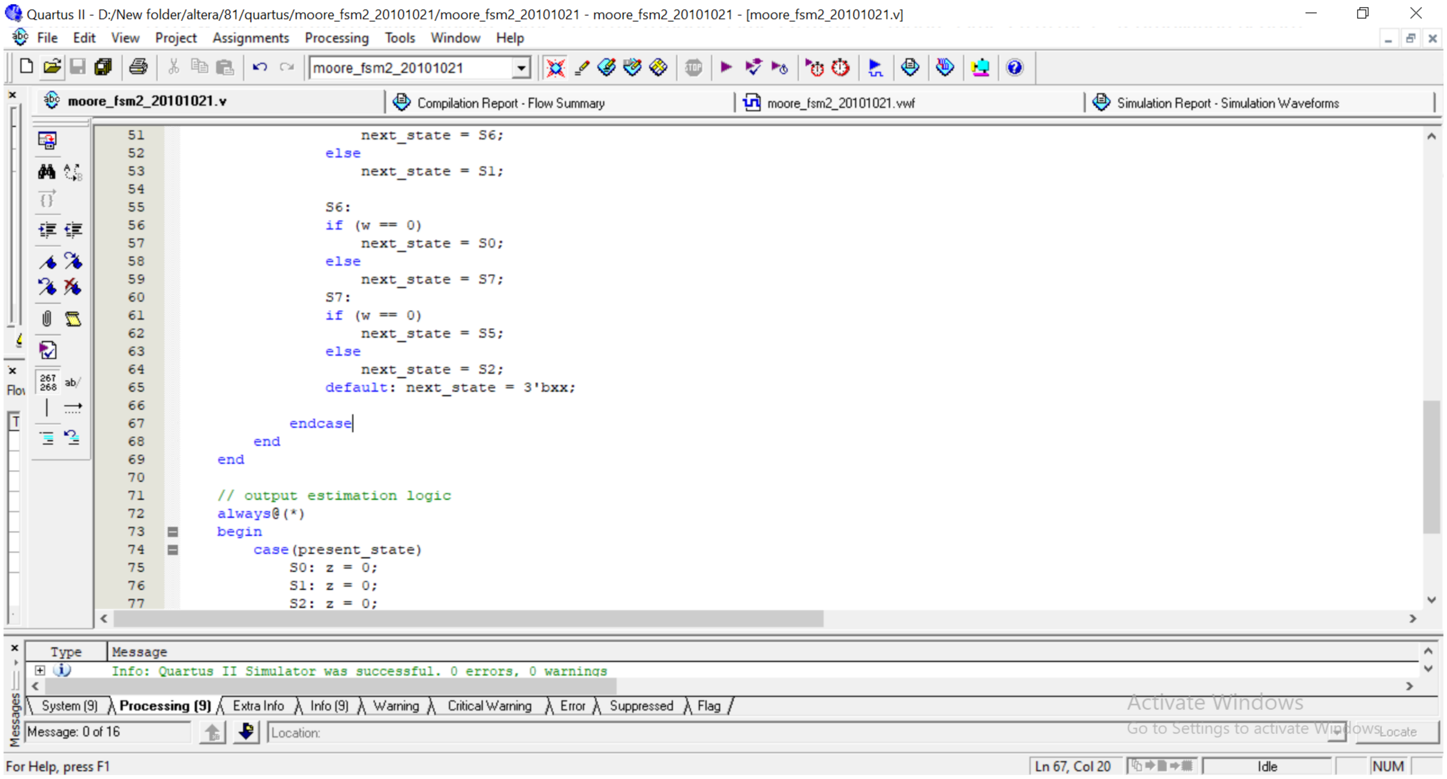
moore_fsm2_20101021
moore_fsm2_20101021.v
Compilation Report - Flow Summary
moore_fsm2_20101021.vwf
Simulation Report - Simulation Waveforms
Type
Message
System (9)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
Locate
Activate Windows
Go to Settings to activate Windows.
For Help, press F1
Ln 15, Col 32
Idle
NUM

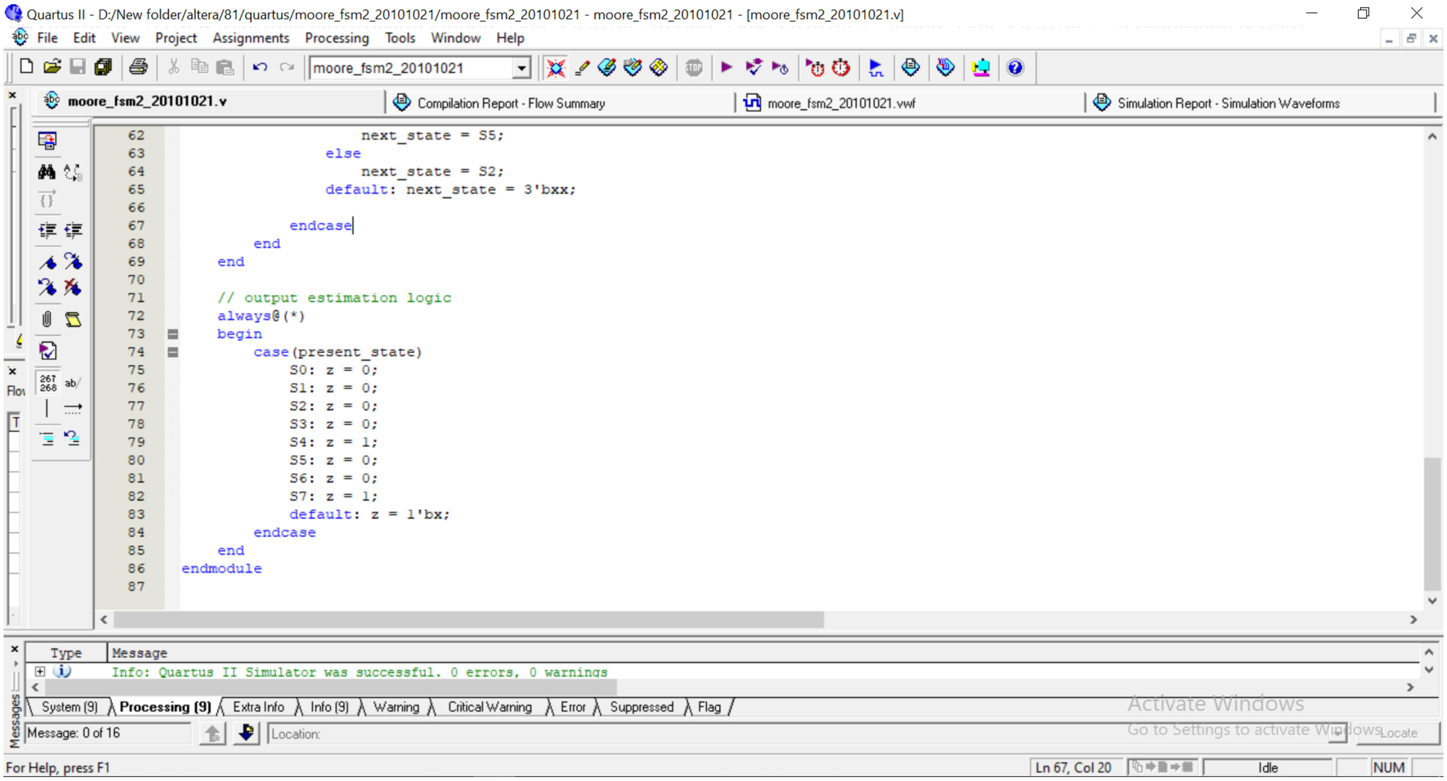
```
                else
                    next_state = S1;
                S1:
                if (w == 0)
                    next_state = S5;
                else
                    next_state = S2;
                S2:
                if (w == 0)
                    next_state = S5;
                else
                    next_state = S3;

                S3:
                if (w == 0)
                    next_state = S5;
                else
                    next_state = S4;
                S4:
                if (w == 0)
                    next_state = S5;
                else
                    next_state = S4;
                S5:
                if (w == 0)
                    next_state = S6;
                else
```

```
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```


Quartus II - D:/New folder/altera/81/quartus/moore_fsm2_20101021/moore_fsm2_20101021 - moore_fsm2_20101021 - [moore_fsm2_20101021.v]
File Edit View Project Assignments Processing Tools Window Help
moore_fsm2_20101021
moore_fsm2_20101021.v
Compilation Report - Flow Summary
moore_fsm2_20101021.vwf
Simulation Report - Simulation Waveforms
Type
Message
System (9)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
Locate
Activate Windows
Go to Settings to activate Windows.
For Help, press F1
Ln 67, Col 20
Idle
NUM

```
                    next_state = S6;
                else
                    next_state = S1;

                S6:
                if (w == 0)
                    next_state = S0;
                else
                    next_state = S7;
                S7:
                if (w == 0)
                    next_state = S5;
                else
                    next_state = S2;
                default: next_state = 3'bxx;

            endcase
        end
    end

    // output estimation logic
    always@(*)
    begin
        case(present_state)
            S0: z = 0;
            S1: z = 0;
            S2: z = 0;
```

```
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

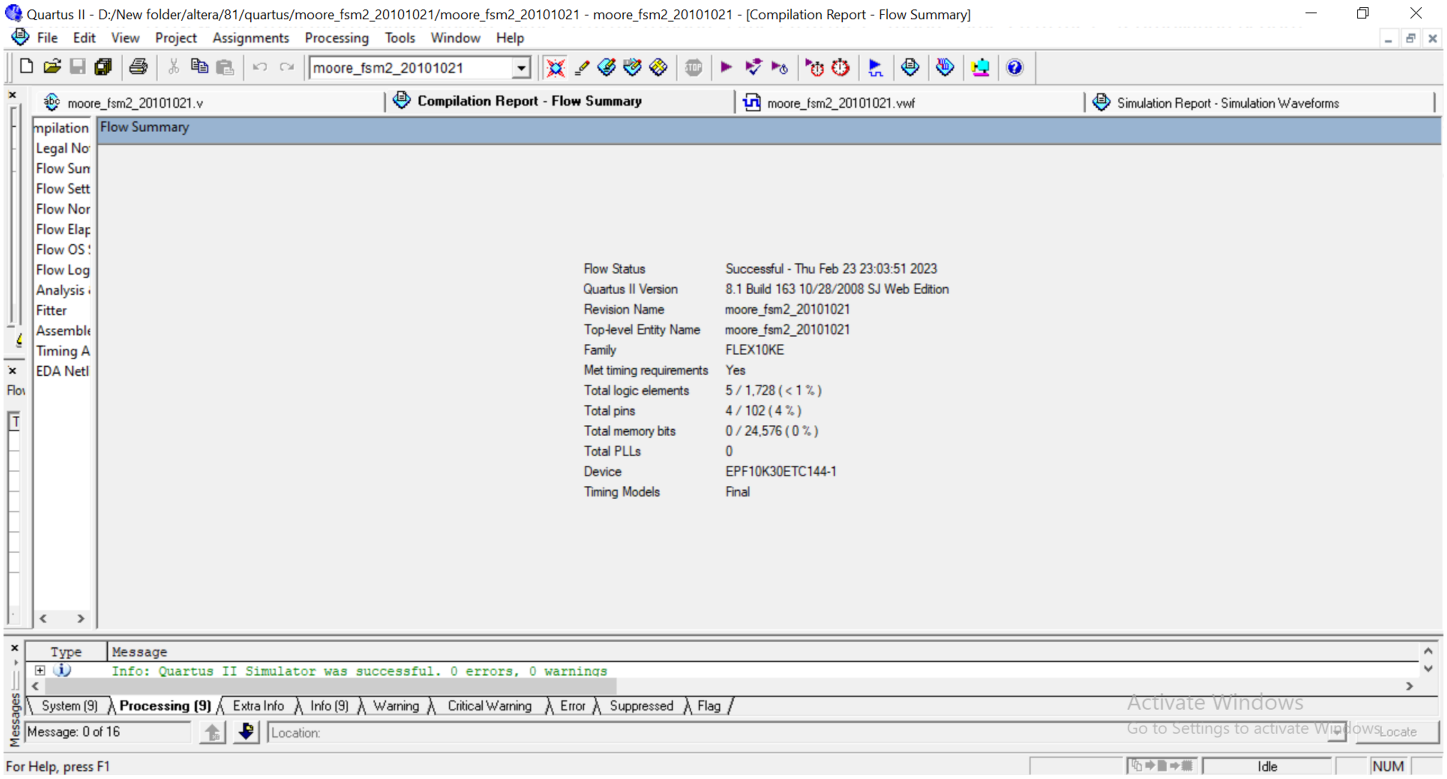

Quartus II - D:/New folder/altera/81/quartus/moore_fsm2_20101021/moore_fsm2_20101021 - moore_fsm2_20101021 - [moore_fsm2_20101021.v]
File Edit View Project Assignments Processing Tools Window Help
moore_fsm2_20101021
moore_fsm2_20101021.v
Compilation Report - Flow Summary
moore_fsm2_20101021.vwf
Simulation Report - Simulation Waveforms

```
          next_state = S5;
        else
          next_state = S2;
        default: next_state = 3'bxx;

      endcase
    end
  end

  // output estimation logic
  always@(*)
  begin
    case(present_state)
      S0: z = 0;
      S1: z = 0;
      S2: z = 0;
      S3: z = 0;
      S4: z = 1;
      S5: z = 0;
      S6: z = 0;
      S7: z = 1;
      default: z = 1'bx;
    endcase
  end
endmodule
```

```
Type  Message
      Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

System (9) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
Locate
Activate Windows
Go to Settings to activate Windows.
For Help, press F1
Ln 67, Col 20
Idle
NUM

Compilation Report:


Quartus II - D:/New folder/altera/81/quartus/moore_fsm2_20101021/moore_fsm2_20101021 - moore_fsm2_20101021 - [Compilation Report - Flow Summary]
File Edit View Project Assignments Processing Tools Window Help
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moore_fsm2_20101021.v
Compilation Report - Flow Summary
moore_fsm2_20101021.vwf
Simulation Report - Simulation Waveforms
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Timing A
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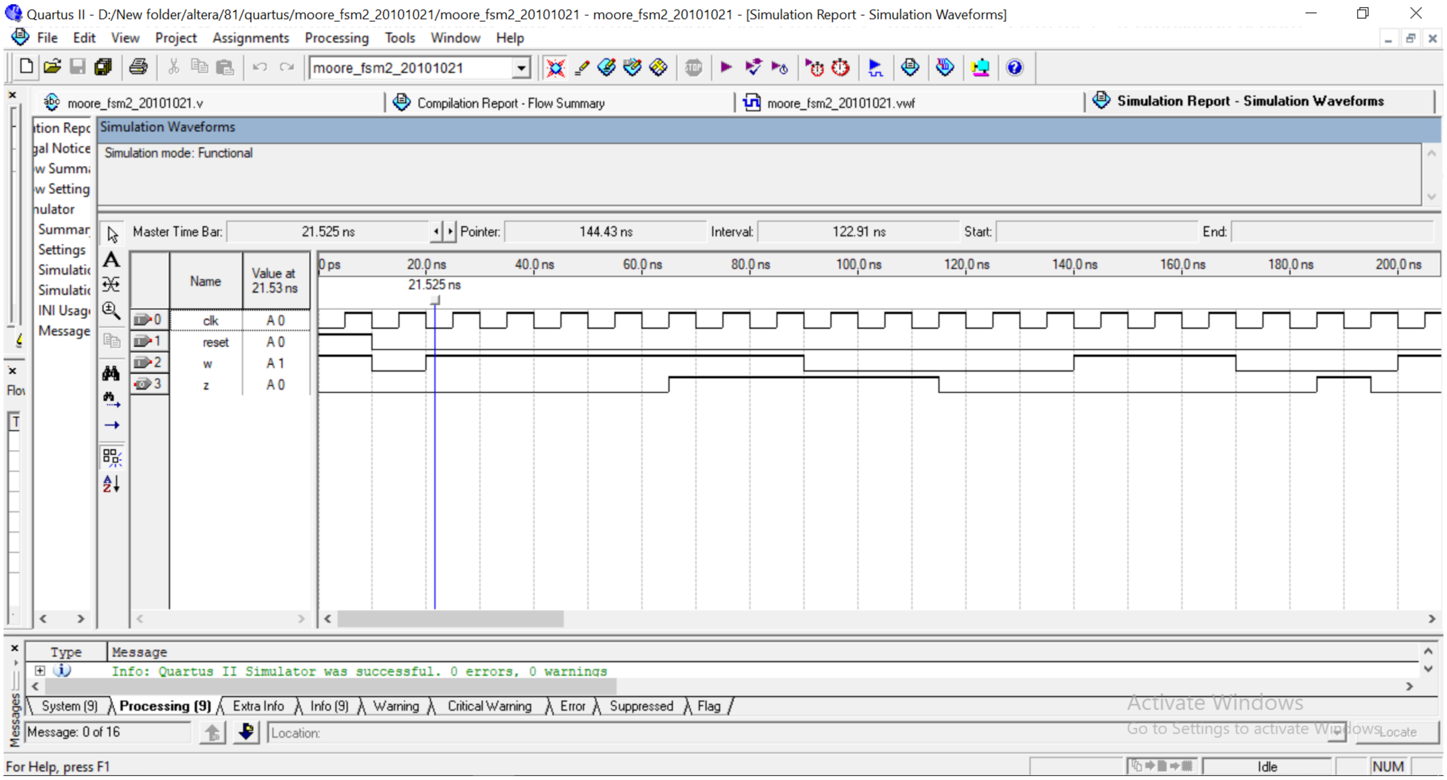
Flow Summary

Flow Status	Successful - Thu Feb 23 23:03:51 2023
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	moore_fsm2_20101021
Top-level Entity Name	moore_fsm2_20101021
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	5 / 1,728 (< 1 %)
Total pins	4 / 102 (4 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

```
Type  Message
      Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

System (9) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
Locate
Activate Windows
Go to Settings to activate Windows.
For Help, press F1
Idle
NUM

2. Screenshot of the timing diagram showing the patterns are detected successfully



Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 21.525 ns Pointer: 144.43 ns Interval: 122.91 ns Start: End:

	Name	Value at 21.53 ns
0	clk	A 0
1	reset	A 0
2	w	A 1
3	z	A 0

```
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

Message: 0 of 16 Location:

3. Discussion and comments on the timing diagram.

We know, in Moore type FSM, output of the sequential circuit depends only on the states of the circuit.

And since the above code shows this characteristic, it is a Moore type FSM.

Here, the finite state machine generates output, z =0 when the previous 4 values of w were 1001 or 1111; otherwise output low, z=0, is returned.

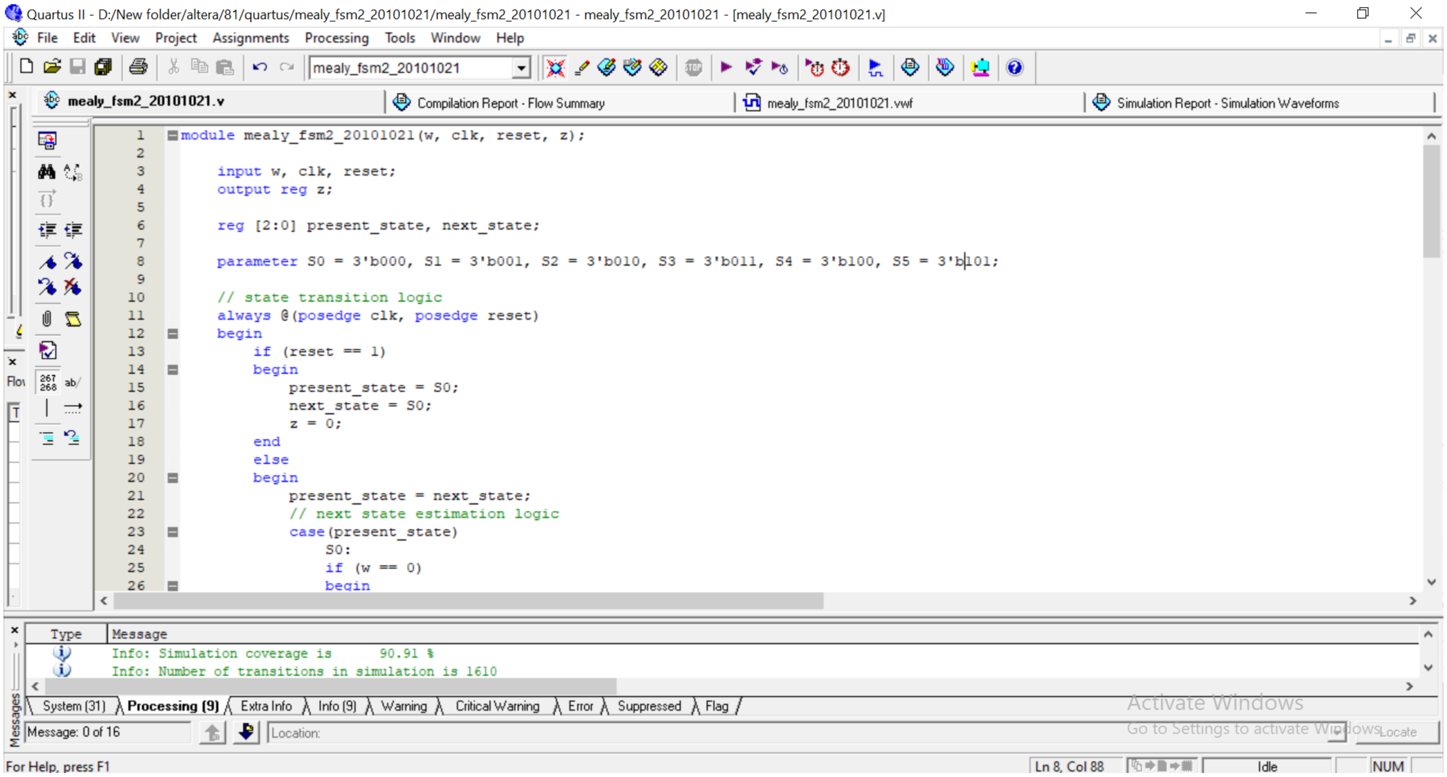
At the beginning of the code, initial state is set as S0 where reset =1 as the Moore State Diagram suggests.

For reset = 0, the conditions for the state table are applied for randomized values of w.

We can see from the simulation that for each 1001 or 1111 pattern detected in w values, at 4 consecutive positive edges of clock, after that, a positive-edged output, z=1, is noticed and hold till the following positive edge.

Problem 1(b) – Mealy FSM:

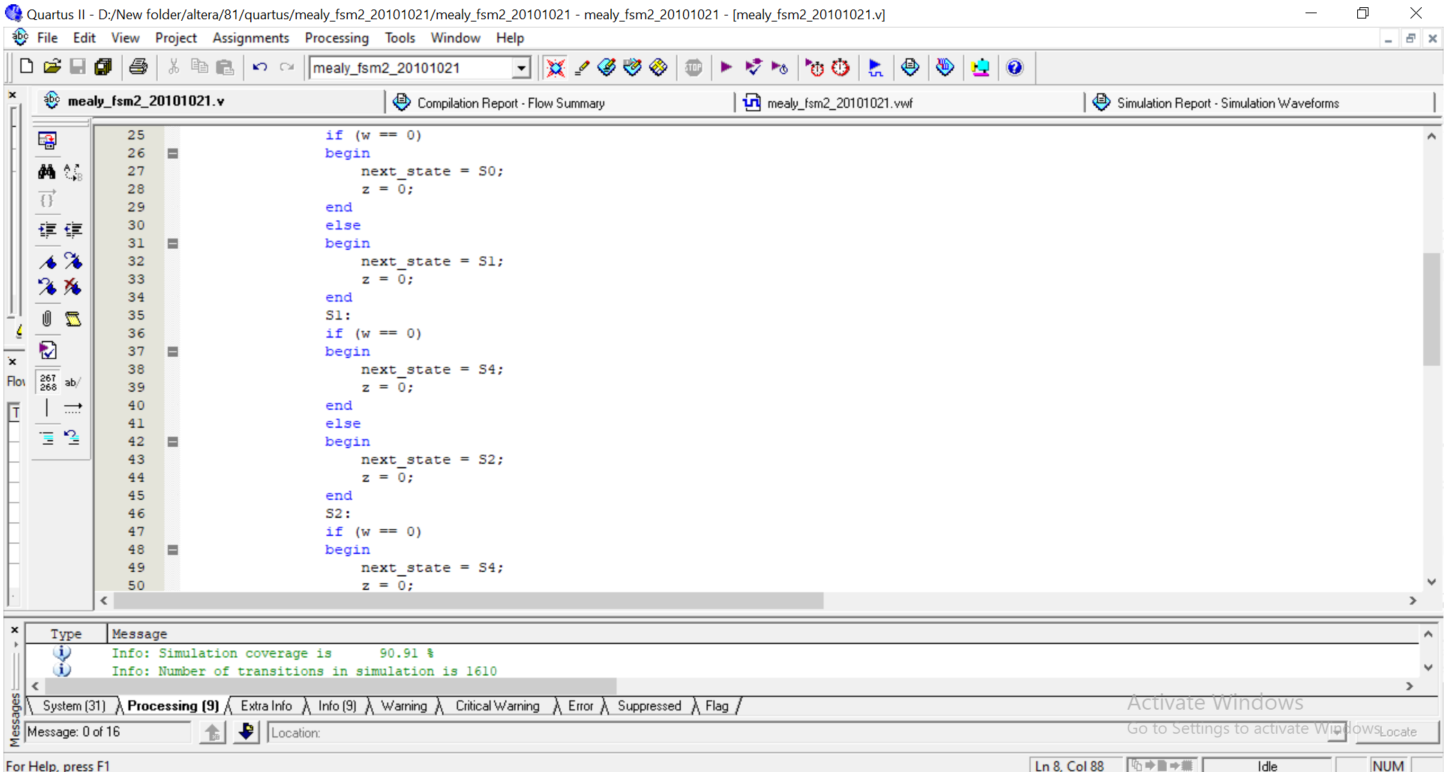
1. Screenshot of the Verilog Code



Quartus II - D:/New folder/altera/81/quartus/mealy_fsm2_20101021/mealy_fsm2_20101021 - mealy_fsm2_20101021 - [mealy_fsm2_20101021.v]

```
module mealy_fsm2_20101021(w, clk, reset, z);

    input w, clk, reset;
    output reg z;

    reg [2:0] present_state, next_state;

    parameter S0 = 3'b000, S1 = 3'b001, S2 = 3'b010, S3 = 3'b011, S4 = 3'b100, S5 = 3'b101;

    // state transition logic
    always @(posedge clk, posedge reset)
    begin
        if (reset == 1)
        begin
            present_state = S0;
            next_state = S0;
            z = 0;
        end
        else
        begin
            present_state = next_state;
            // next state estimation logic
            case(present_state)
                S0:
                if (w == 0)
                begin
```

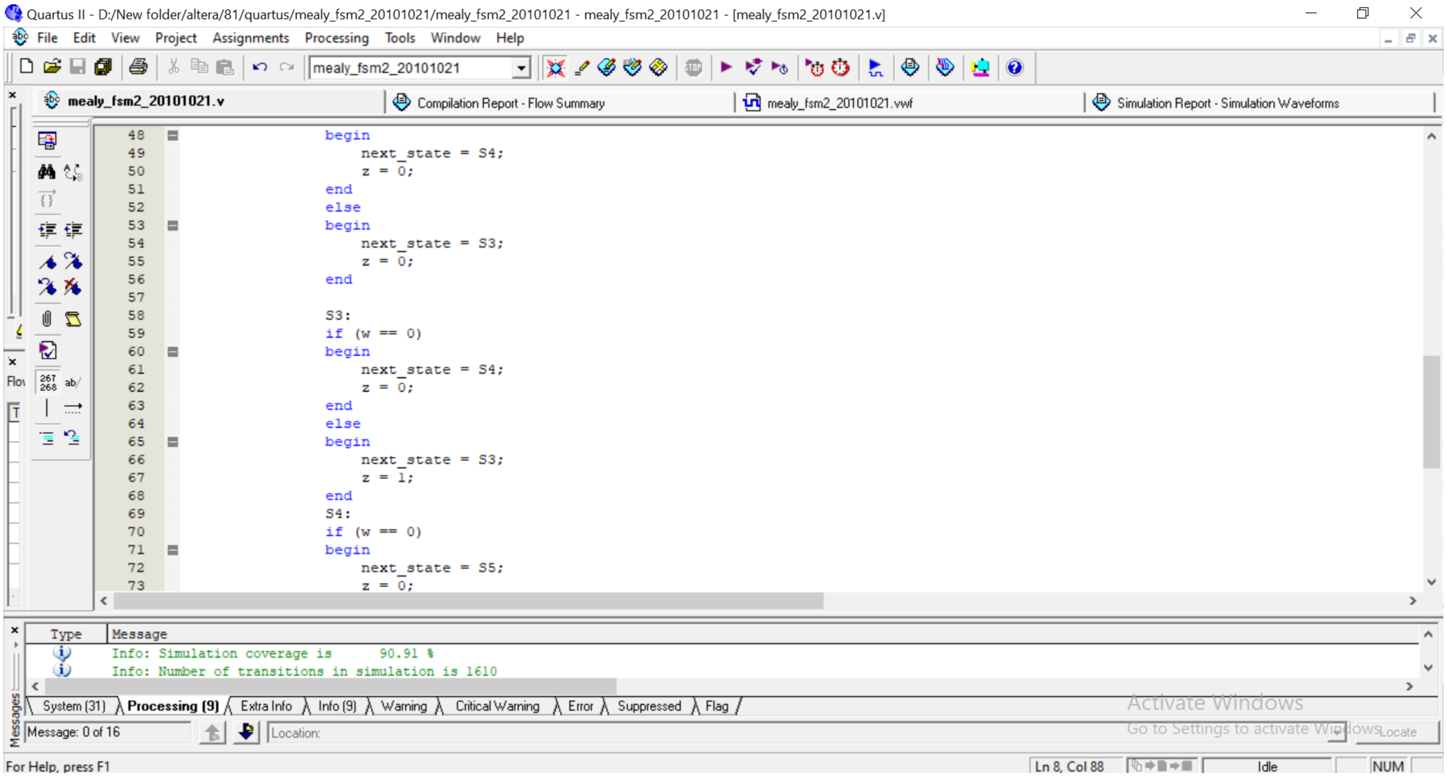
```
Type  Message
      Info: Simulation coverage is      90.91 %
      Info: Number of transitions in simulation is 1610
```



Quartus II - D:/New folder/altera/81/quartus/mealy_fsm2_20101021/mealy_fsm2_20101021 - mealy_fsm2_20101021 - [mealy_fsm2_20101021.v]

```
                if (w == 0)
                begin
                    next_state = S0;
                    z = 0;
                end
                else
                begin
                    next_state = S1;
                    z = 0;
                end
                S1:
                if (w == 0)
                begin
                    next_state = S4;
                    z = 0;
                end
                else
                begin
                    next_state = S2;
                    z = 0;
                end
                S2:
                if (w == 0)
                begin
                    next_state = S4;
                    z = 0;
```

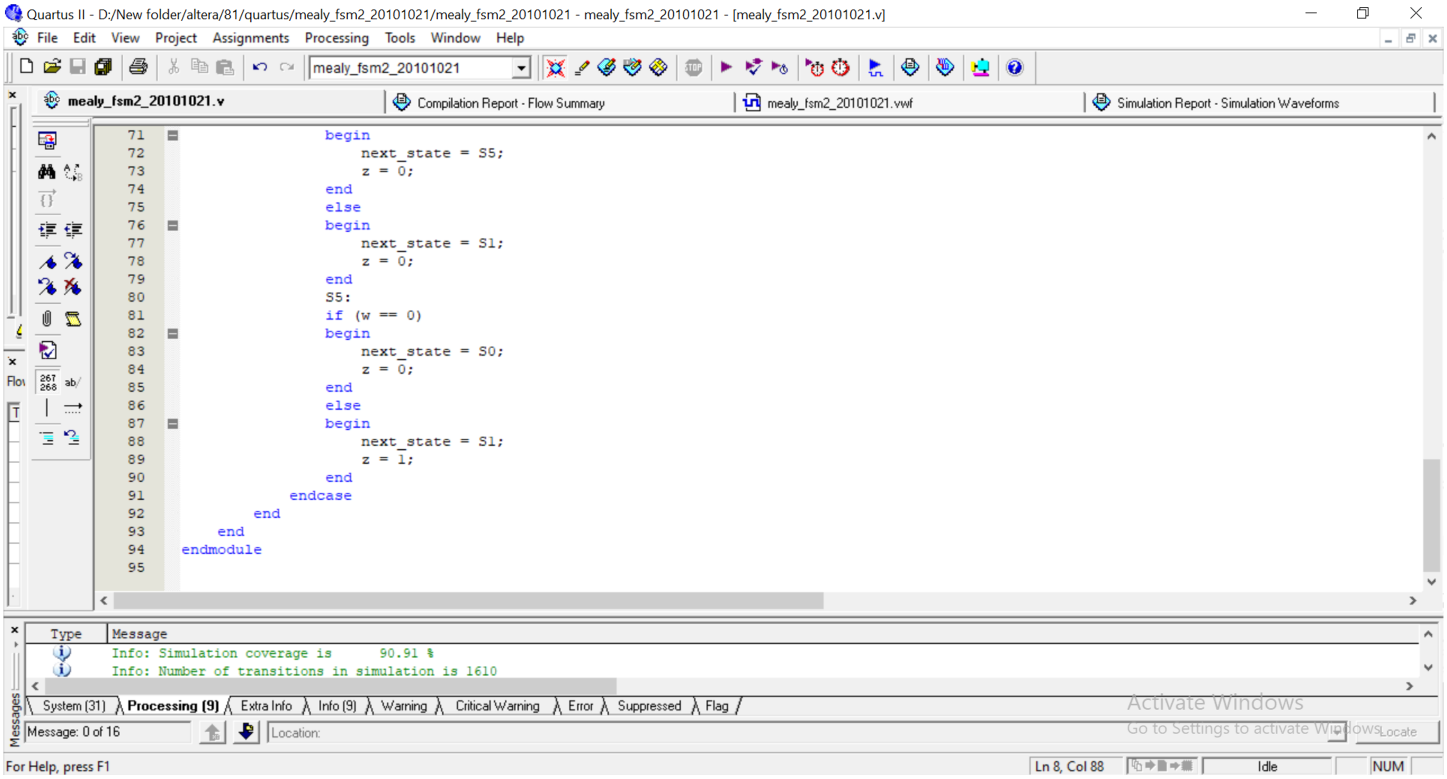
```
Type  Message
      Info: Simulation coverage is      90.91 %
      Info: Number of transitions in simulation is 1610
```


Quartus II - D:/New folder/altera/81/quartus/mealy_fsm2_20101021/mealy_fsm2_20101021 - mealy_fsm2_20101021 - [mealy_fsm2_20101021.v]
File Edit View Project Assignments Processing Tools Window Help
mealy_fsm2_20101021
mealy_fsm2_20101021.v
Compilation Report - Flow Summary
mealy_fsm2_20101021.vwf
Simulation Report - Simulation Waveforms

```
                begin
                    next_state = S4;
                    z = 0;
                end
                else
                begin
                    next_state = S3;
                    z = 0;
                end

                S3:
                if (w == 0)
                begin
                    next_state = S4;
                    z = 0;
                end
                else
                begin
                    next_state = S3;
                    z = 1;
                end
                S4:
                if (w == 0)
                begin
                    next_state = S5;
                    z = 0;
```

```
Type  Message
      Info: Simulation coverage is      90.91 %
      Info: Number of transitions in simulation is 1610
```

System (31)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
Locate
Activate Windows
Go to Settings to activate Windows.
For Help, press F1
Ln 8, Col 88
Idle
NUM

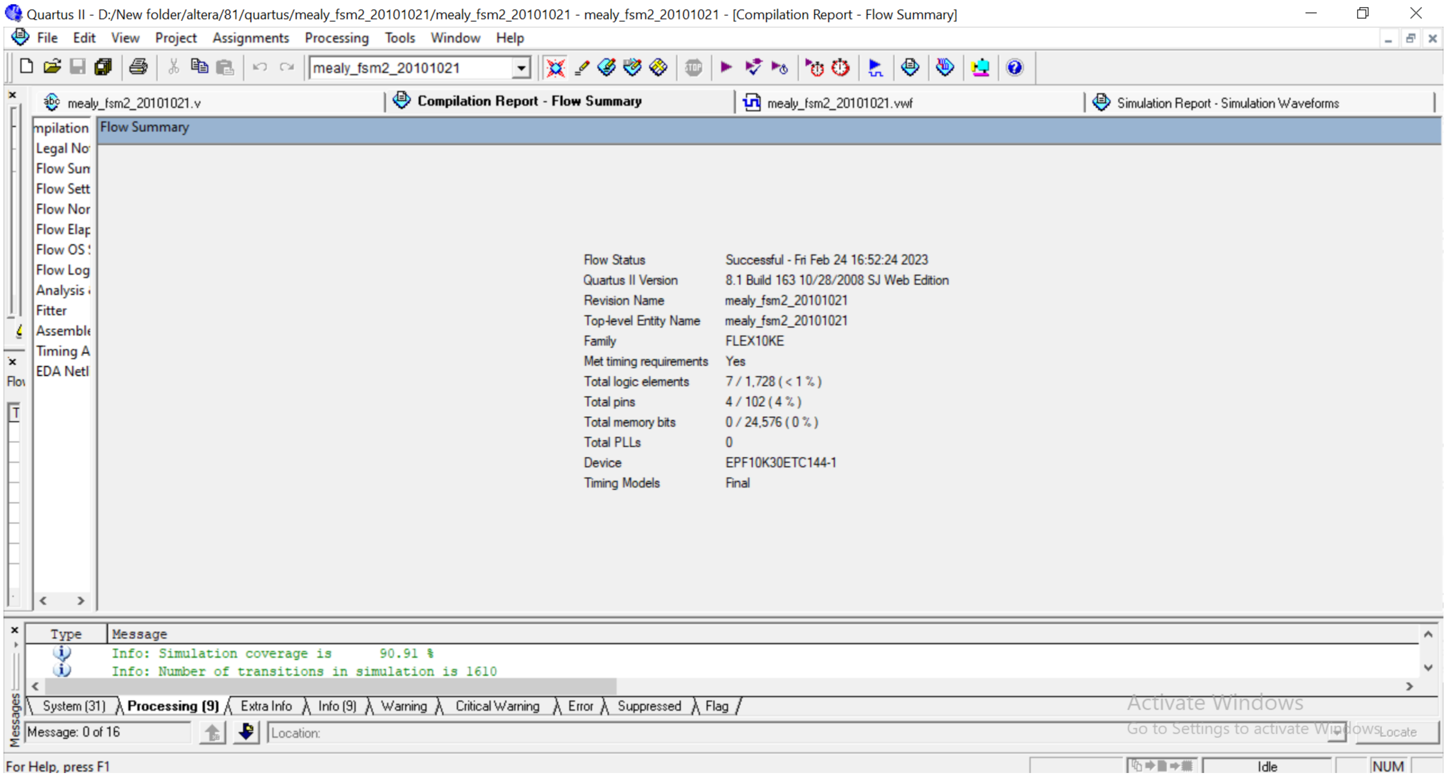

Quartus II - D:/New folder/altera/81/quartus/mealy_fsm2_20101021/mealy_fsm2_20101021 - mealy_fsm2_20101021 - [mealy_fsm2_20101021.v]
File Edit View Project Assignments Processing Tools Window Help
mealy_fsm2_20101021
mealy_fsm2_20101021.v
Compilation Report - Flow Summary
mealy_fsm2_20101021.vwf
Simulation Report - Simulation Waveforms

```
                begin
                    next_state = S5;
                    z = 0;
                end
                else
                begin
                    next_state = S1;
                    z = 0;
                end
                S5:
                if (w == 0)
                begin
                    next_state = S0;
                    z = 0;
                end
                else
                begin
                    next_state = S1;
                    z = 1;
                end
            endcase
        end
    end
endmodule
```

```
Type  Message
      Info: Simulation coverage is      90.91 %
      Info: Number of transitions in simulation is 1610
```

System (31)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
Locate
Activate Windows
Go to Settings to activate Windows.
For Help, press F1
Ln 8, Col 88
Idle
NUM

Compilation Report:



Quartus II - D:/New folder/altera/81/quartus/mealy_fsm2_20101021/mealy_fsm2_20101021 - mealy_fsm2_20101021 - [Compilation Report - Flow Summary]

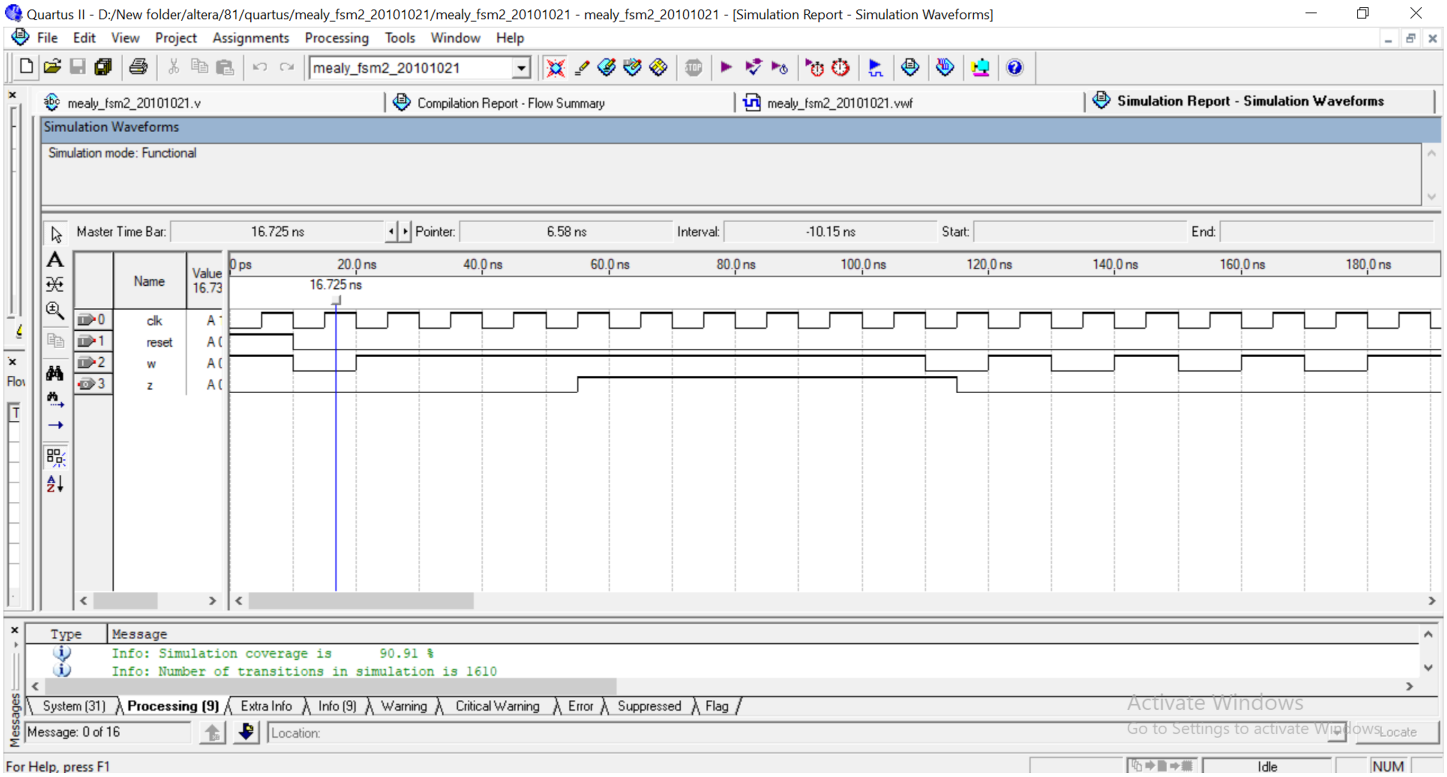
Flow Summary

Flow Status	Successful - Fri Feb 24 16:52:24 2023
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	mealy_fsm2_20101021
Top-level Entity Name	mealy_fsm2_20101021
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	7 / 1,728 (< 1 %)
Total pins	4 / 102 (4 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

```
Type  Message
      Info: Simulation coverage is      90.91 %
      Info: Number of transitions in simulation is 1610
```

System (31) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
Locate
Activate Windows
Go to Settings to activate Windows.
For Help, press F1
Idle
NUM

2. Screenshot of the timing diagram showing the patterns are detected successfully



Quartus II - D:/New folder/altera/81/quartus/mealy_fsm2_20101021/mealy_fsm2_20101021 - mealy_fsm2_20101021 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help
mealy_fsm2_20101021
mealy_fsm2_20101021.v
Compilation Report - Flow Summary
mealy_fsm2_20101021.vwf
Simulation Report - Simulation Waveforms

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 16.725 ns Pointer: 6.58 ns Interval: -10.15 ns Start: End:

0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
140.0 ns
160.0 ns
180.0 ns
16.725 ns
Name
Value 16.73
0 clk A
1 reset A 0
2 w A 0
3 z A 0

```
Type  Message
      Info: Simulation coverage is      90.91 %
      Info: Number of transitions in simulation is 1610
```

System (31) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
Locate
Activate Windows
Go to Settings to activate Windows.
For Help, press F1
Idle
NUM

3. Discussion and comments on the timing diagram.

We know, in Mealy type FSM, output of the sequential circuit depends on the states of the circuit and the present values of its input.

And since the above code shows this characteristic, it is a Moore type FSM.

Here, the finite state machine generates output, z =0 when the previous 4 values of w were are 1001 or 1111; otherwise output low, z=0, is returned.

At the beginning of the code, initial state is set as S0 where reset =1 as the Mealy State Diagram suggests.

For reset = 0, the conditions for the state table are applied for randomized values of w.

Mealy type needs smaller number of states in comparison to Moore type FSM. We can see from the simulation that the FSM successfully recognizes the patterns and returns the desired output for z.