Working with Altera Quartus:

Procedure:

<initial setup>
1. Open Quartus.
2. Click File->New Project Wizard->Next
3. Fill out the following:
What is the working directory for this project? – Browse->Create a folder in a suitable directory **other than C drive (Downloads, Desktop are also parts of C drive, DO NOT OPEN A PROJECT THERE!!)**->Select the folder
What is the name of the project->Type a name and remember it(Say “expt1”). Same name is going to be copied to the next box automatically.
Press next.
4. Press next (Page: 2/5, no need to fill)
5. Select Device Family: FLEX10KE and press next. (Page: 3/5)
6. Fill out the following in all three pair of boxes:
Tool name: Custom
Format: Verilog HDL/Verilog
Press Next->Finish

<code>
7. File->New->Verilog HDL File->OK
8. Write the code and save it with the same name as that given in expt1 with the extension of .v (Example: expt1.v)

<waveform: simulation>
9. File->New->Vector Waveform File
10. Right click on pin ‘Name’ (blank space)->Insert->Insert Node or BUS
11. Click Node Finder.
Filter: Pins: all.
Click list->Click “>>” -> OK -> OK
12. Right click on each input->Value->Clock and set up the clocks.
13. Save with the same filename as the .vwf file (Example: expt1.vwf)
14. Assignment->Settings->Simulator Settings
Simulation Mode: Functional
Click OK.
15. Processing-> Generate Functional Simulation Netlist
16. Processing-> Start Simulation

<RTL viewer>
17. Tools-> Netlist viewer->RTL viewer