CSE460L: Assignment 5

Assignment deadline: **April 14, 2023 (11.59 PM).**

General guidelines

Draw the circuit using the appropriate tool as taught in the lab and rectify all design errors (if any), submit the full screen screenshots of the design file and the simulation file **with proper discussion.**

Problem:

Derive the Boolean logic expression from the following K-Map and implement the logic function using CMOS technology. You may use blocks/sub-circuits made using CMOS technology but cannot use readily available logic gates.

CD \ AB	00	01	11	10
00	1	0	1	1
01	1	d	d	0
11	d	d	1	0
10	1	1	0	1

Submission link: https://forms.gle/Xpvb7Pb1rnnXNmEX7