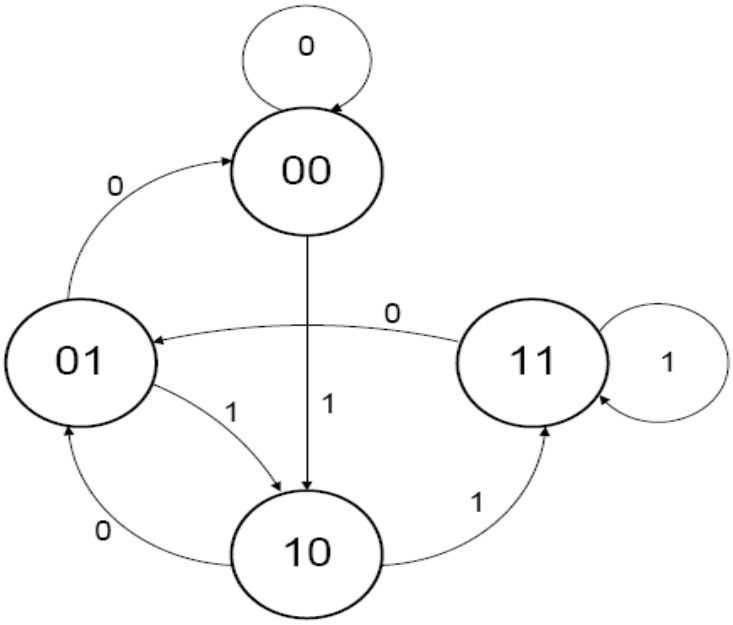
(10 points)
Draw the state diagram of a FSM that has an input D and output Z, such that the output is always equal to the input and delayed by 2 clock cycles.
Follow the sequential circuit design procedure using D flip flops design and implement the circuit.

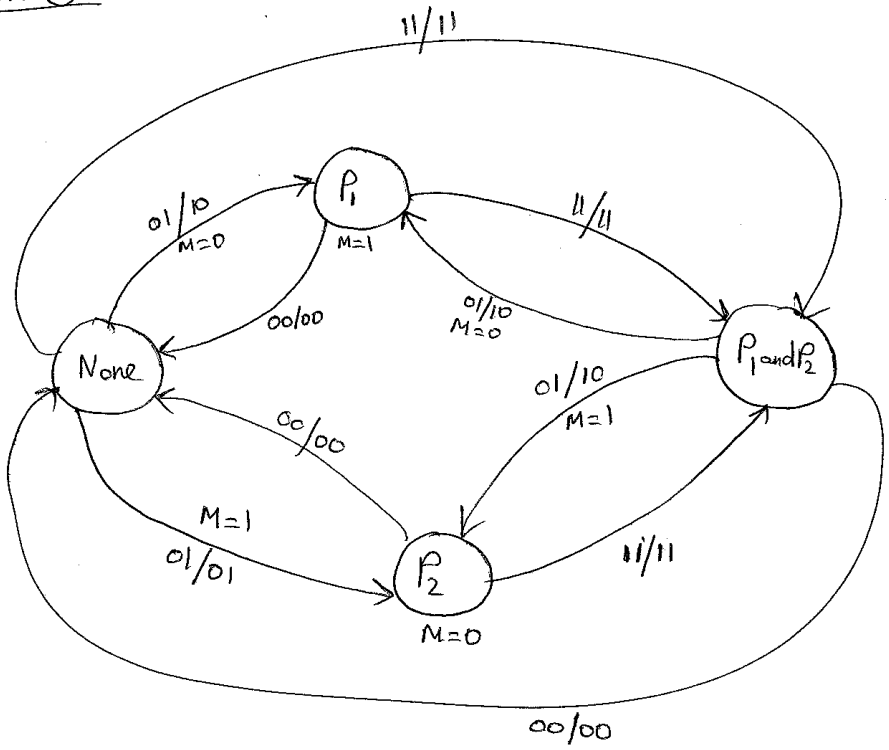


y_2	y_1	x=0		x=1	
		y_2^+	y_1^+	y_2^+	y_1^+
0	0	0	0	1	0
0	1	0	0	1	0
1	0	0	1	1	1
1	1	0	1	1	1

$$y_2^+ = x = D_2$$
$$y_1^+ = y_2 = D_1$$

Problem 2

Problem ①:



* Note: We ignored the part about exploiting both pumps equally intensively.