Galala University Computer Organization and Assembly programming
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Assignment 7

1. For the following code on a regular RISC 5 stage pipelined processor, calculate (with a complete description of each single micro-instruction) the value of R1 and R2 at the end of the program, where R1, R2 and R3 are general purpose registers, assume the initial value in R1=5 and R2=8 and R3=3

   Justify the value obtained

```
    ADD   R1,R3
    ADD   R2,R1
    If R2>= 10  goto  AAA
    ADD   R2,R3
AAA SUB   R2,R1
```

2. For the following so called GU processor that consists of the following steps (micro-instructions)
   - fetch instructions from memory (IF)
   - read registers and decode the instruction (ID)
   - execute the instruction or calculate an address (EX)
   - write the result into a register (WB)
   - access an operand in data memory (MEM)

   Calculate the value in R2, and R1 at the end of the program, where R1, R2 and R3 are general purpose registers, assume the initial value in R1=5 and R2=8 and R3=5 and data at memory location A=1, if data is needed to be loaded from MDR, assume the next micro-instruction is delayed until data reaches the MDR

```
    ADD   R1,A
    ADD   R2,R1
    If R2 >=10        goto AAA
    ADD   R2,R3
AAA SUB   R2,R1
```

3. TRUE or FALSE
   a. For a processor that receives serial data and gives out results at the same rate, it is possible and efficient to pipeline it only if there are no branch instructions
   b. Pipelining is a programming technique that exploits all empty registers in a processor

c. Stalls typically happen in a pipelining process due to increased bandwidth (increased speed) for input data.
d. Pipelining is preferred to increase the throughput for a running program

4. TRUE or FALSE
    a. A structural hazard may not necessary happen if two different micro instructions are trying access data from the General purpose registers.
    b. Although data hazards, and control hazards both affect the pipelining performance, they cause bubbles (stalls/idle's) in different manners.
    c. With the presence of stalls in the pipelining diagram, the program execution time will increase when compared to the absence of stalls scenario.
    d. Pipelining reduces the execution time for every micro instruction

5. In the following example, detect if any type of hazard will occur, if we are dealing with the RISC architecture, initially R1=5, R2=3, R3=12

```
        ADD     R1,R2
        Mov     R2,R3
        If  R2>=10  goto  AAA
        ADD     R1,A
        END

AAA     SUB     R1,R2
        END
```