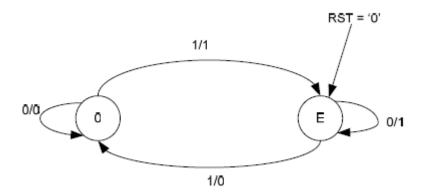
Digital Logic Design CSE 131 Dr Gamal Fahmy Galala University Problem 5_11

Homework 11

For the state diagram given below, draw the schematic circuit with D-flipflops



Assume you have two States: O and E, one input: X, one output: Z

<u>Problem 5-12:</u> Reduce the number of states in the following table and tabulate the reduced state table.

	NEXT STATE		OUTPUT	
PRESENT STATE	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	С	0	0
С	f	е	0	0
d	g	a	1	0
е	d	С	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0