Galala University, Faculty of Computer Science and Engineering
CSE 230 Computer Organization
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Homework 1

Problem 1

Draw the state diagram of a FSM that has an input D and output Z, such that the output is always equal to the input and delayed by 2 clock cycles.
Follow the sequential circuit design procedure using D flip flops design and implement the circuit.

Problem 2

Design a sequential FSM, which will control two pumps working in a coal mine. A sensor measuring the level of water in hazardous place provides the input to your FSM. The water level is encoded as follows:

00 - very low, no danger
01 - increased, warning of possible danger
11 - dangerously high
10 - not used

Your FSM has two active-1 outputs, which turn on or off two pumps: pump1 and pump2. Both pumps should work as follows:

If the water level is low (00), none of the pumps is working.
If the water level is increased (01), only one pump is working.
If the water level is high (11), both pumps are working.

Additionally you want to exploit both pumps equally intensively, therefore they should interchange in cases when when only one pump should work. For example:

Clock cycle	**water level**	**pump 1**	**pump 2**
1	00	0	0
2	00	0	0
3	01	1	0
4	01	1	0
5	00	0	0
6	01	0	1
7	01	0	1
8	11	1	1
9	11	1	1
10	01	1	0
11	01	1	0
12	00	0	0

For simplification, assume that water level does not change rapidly, therefore you don't have to consider these situations. Implement your FSM as either Moore or Mealy machine.
The output should be encoded as follows:

No pumps working - Blank display
Pump 1 working - Number 1
Pump 2 working - Number 2
Both pumps working - Capital character A