Sequential Circuits

Module 5

UGTA - Corey Lancelotta

Key Takeaways

Combinational vs. Sequential Circuits

Memory vs. No Memory

SR Latch

Problem: Oscillation

Level-Sensitive SR Latch

Problem: Avoiding SR = 11

D Latch

Problem: Clock Dependence

D Flip-Flop

Problem: Resource Heavy

Registers

Collection of D Flip-Flops

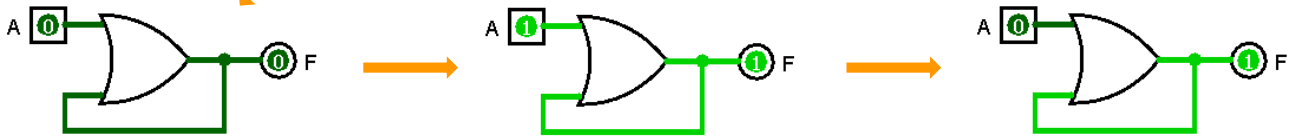
SEQUENTIAL

1. Output depends on inputs and previous states
2. Can store values (memory)
3. Goal: We need to figure out a way to store a value without permanently storing the value

COMBINATIONAL

1. Output depends only on inputs
2. Can't store values (no memory)

We can't change the value of F after initially setting the value!



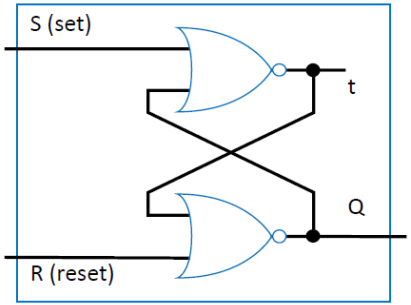
SR LATCH

DETAILS

1. Introduces a feedback mechanism
2. Cross Coupling: The output of each NOR gate serves as an input to the other NOR gate
3. SR = 00 is "undefined" without knowledge of the previous state

SOLUTION & PROBLEM

1. SOLUTION: Allows us to store a value AND change it
2. PROBLEM: Oscillation occurs when the input changes from SR = 11 to SR = 00. (We must prevent SR = 11)



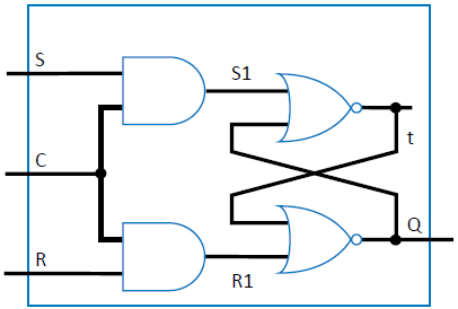
S	R	t	Q
0	0	*	*
0	1	1	0
1	0	0	1
1	1	0	0

* Unknown without knowledge of previous state

F. Vahid and J. Wiley. Digital design. Wiley, 2006.

DETAILS

1. Introduces a mechanism to regulate when the SR values enter the latch
2. Enable Input, C: The latch receives changes in SR values only when C = 1
3. We still need to design a way to ensure that SR = 11 does not get sent to the latch
4. S1 and R1 can change only when C = 1



SOLUTION & PROBLEM

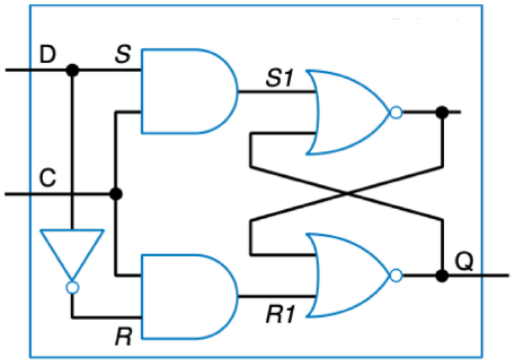
1. SOLUTION: Allows us to regulate when SR values are passed into the latch
2. PROBLEM: Regulating SR values before entry into the latch can be a burden (We are essentially just relocating the problem)

F. Vahid and J. Wiley. Digital design. Wiley, 2006.

D LATCH

DETAILS

1. Introduces a mechanism to ensure SR = 11 can't occur
2. The value of R will always be the opposite of S
3. Still uses the enable input, C



SOLUTION & PROBLEM

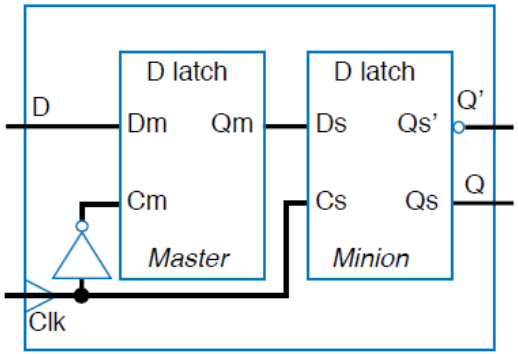
1. SOLUTION: Relieves the burden on regulating SR values prior to entry into the latch
2. PROBLEM: When chaining D Latches together, the number of latches that are triggered is dependent on the clock signal

F. Vahid and J. Wiley. Digital design. Wiley, 2006.

D FLIP-FLOP

DETAILS

1. Introduces a mechanism to ensure that storing values is independent of the clock signal
2. Uses 2 D Latches: Master and Minion
3. Storing values is edge-triggered
4. Master is enabled when Clk = 0
5. Minion is enabled when Clk = 1



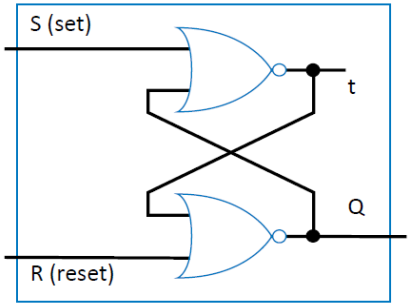
SOLUTION & PROBLEM

1. SOLUTION: Removes the dependence on the clock signal
2. PROBLEM: Uses a lot of components (resource heavy)

F. Vahid and J. Wiley. Digital design. Wiley, 2006.

LATCH OVERVIEW

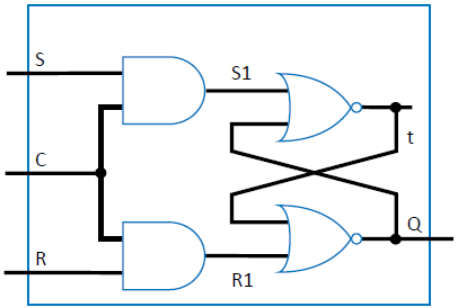
SR Latch



FEATURE: Store and change stored values

PROBLEM: Oscillation

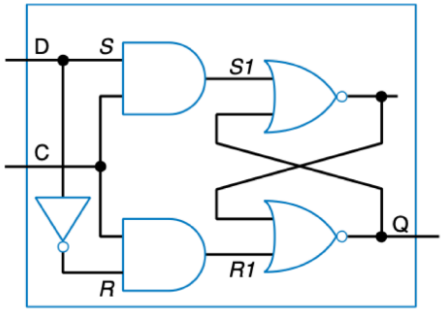
Level-Sensitive SR Latch



FEATURE: Regulate when SR values enter the latch

PROBLEM: Burdensome to manage SR values

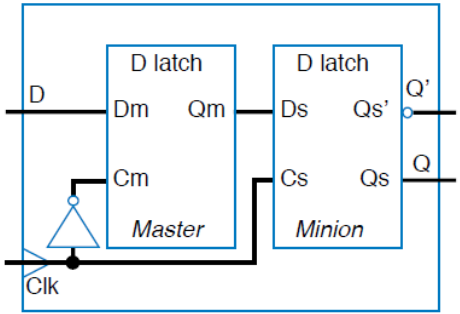
D Latch



FEATURE: Relieves burden of managing SR values

PROBLEM: Clock frequency dependence

D Flip-Flop



FEATURE: Clock frequency independence

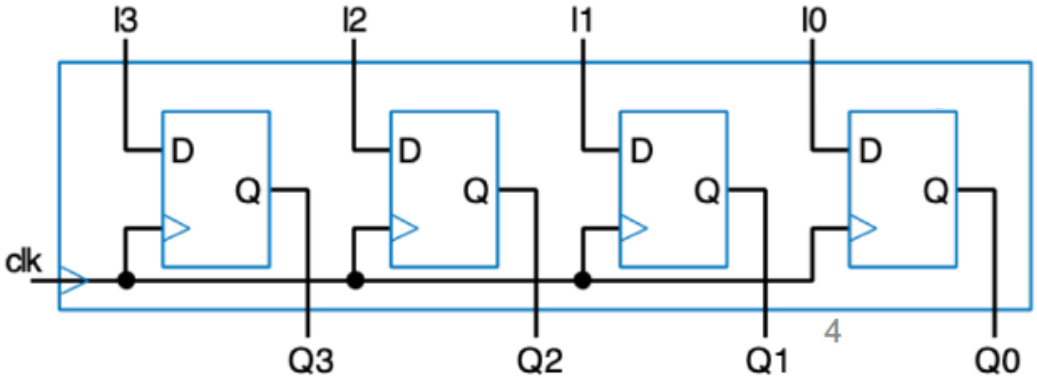
PROBLEM: Resource heavy

F. Vahid and J. Wiley. Digital design. Wiley, 2006.

DETAILS

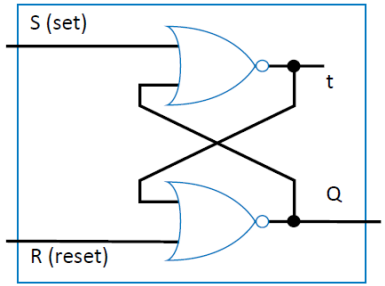
1. Combines multiple D Flip-Flops

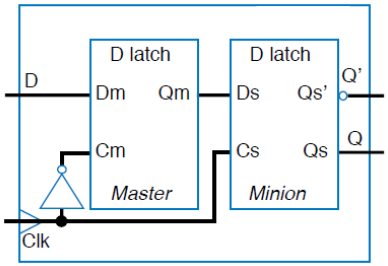
2. All latches share a single clock signal



F. Vahid and J. Wiley. Digital design. Wiley, 2006.

Practice Problems Questions





1. In the **SR Latch** to the right, what are the values of **t** and **Q** when **SR = 10**?
2. In the **SR Latch** to the right, what are the values of **t** and **Q** when **SR = 01**?
3. In the **D Flip-Flop** to the right, what is the value of **Qm** when **D = 1** and **Clk = 1**?
4. In the **D Flip-Flop** to the right, what is the value of **Qm** when **D = 0** and **Clk = 0**?
5. Why is it an issue for **D Latches** to be **dependent on the frequency** of the clock signal?
6. (**True or False**) In a chain of D Flip-Flops, a **high clock frequency** could cause **zero** D Flip-Flops from storing a value?
7. (**True or False**) In a chain of D Flip-Flops, a **short clock period** could cause **zero** D Flip-Flops from storing a value?

F. Vahid and J. Wiley. Digital design. Wiley, 2006.

Practice Problems Answers

1. **t = 0** and **Q = 1**
2. **t = 1** and **Q = 0**
3. **Impossible to tell** without knowledge of the previous state. The value stored in **Qm** will update with the value of **D** only when **Clk = 0.**
4. **Qm = 0**
5. The **frequency of a CPU is variable**. Therefore, if the circuit behavior is dependent on the frequency, **we can't be certain** that the circuits we create will always exhibit the desired behavior.
6. **Yes!** A high frequency means the clock period is shorter. This short clock period could be too short to fully trigger the first D Flip-Flop.
7. **Yes!** A short clock period could be too short to fully trigger the first D Flip-Flop (same behavior as previous question)!