SER 232

Computer Systems Fundamentals I

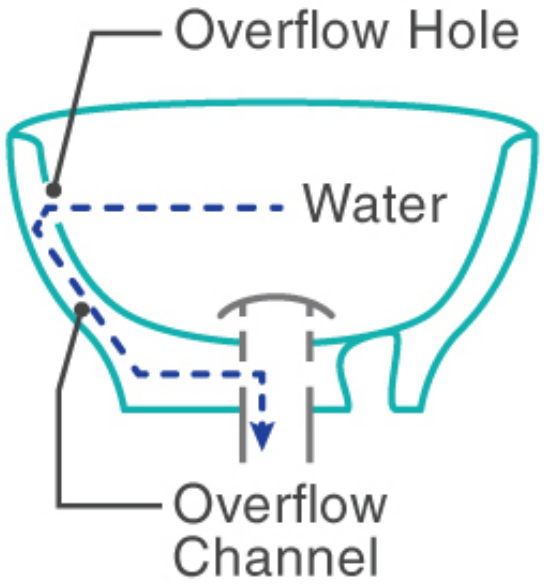
Dr. Heinrichs

Topics

- Gate Delay

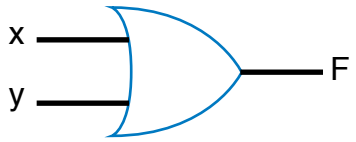
Gate Delay

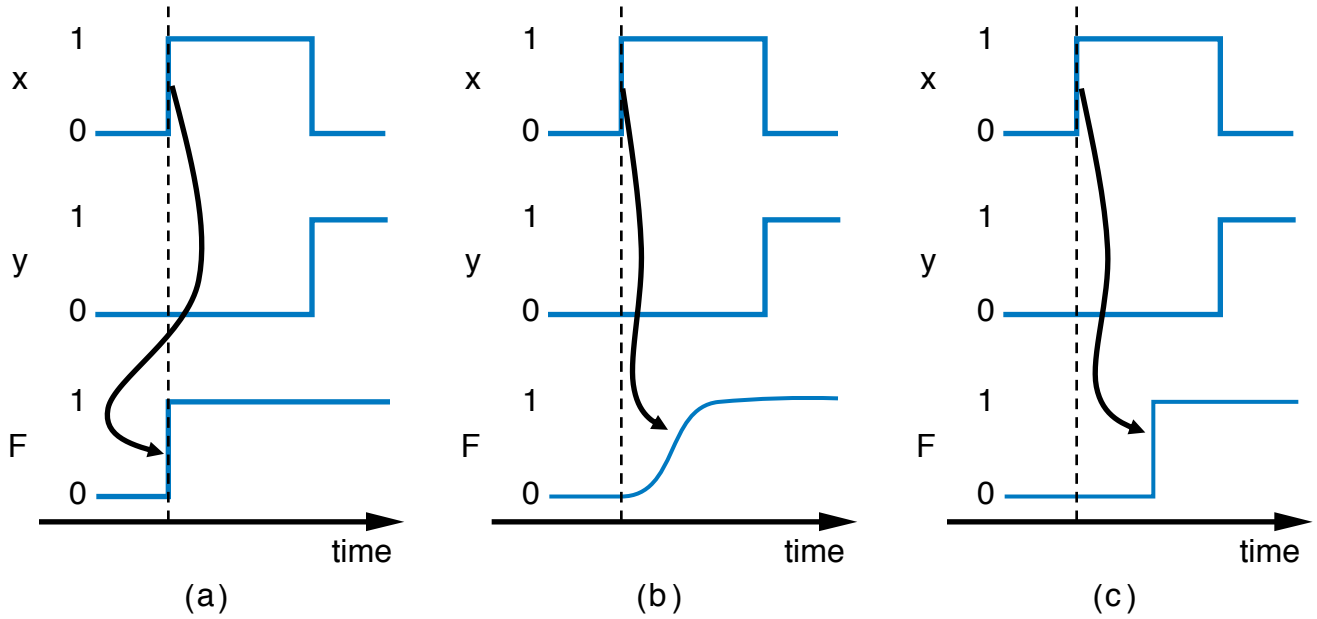
- It takes time for an input signal change to be reflected in the output signal of a gate
  - The more gates a signal passes through, the longer it takes for the correct output to be reached
- Analogy: Sink (with closed drain)
  - Water has to rise to a certain level before it overflows
    - Opening faucet is our “input change”
    - Overflowing water is our “output”
    - Delay between opening faucet and overflowing is our “gate delay”



Gate Delay

- Real gates have some delay
  - Outputs don't change immediately after inputs change





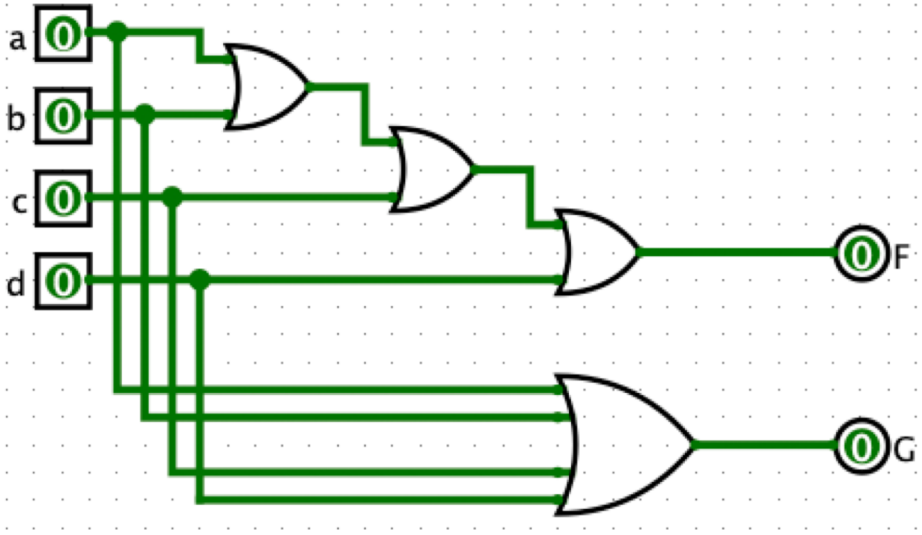
ideal

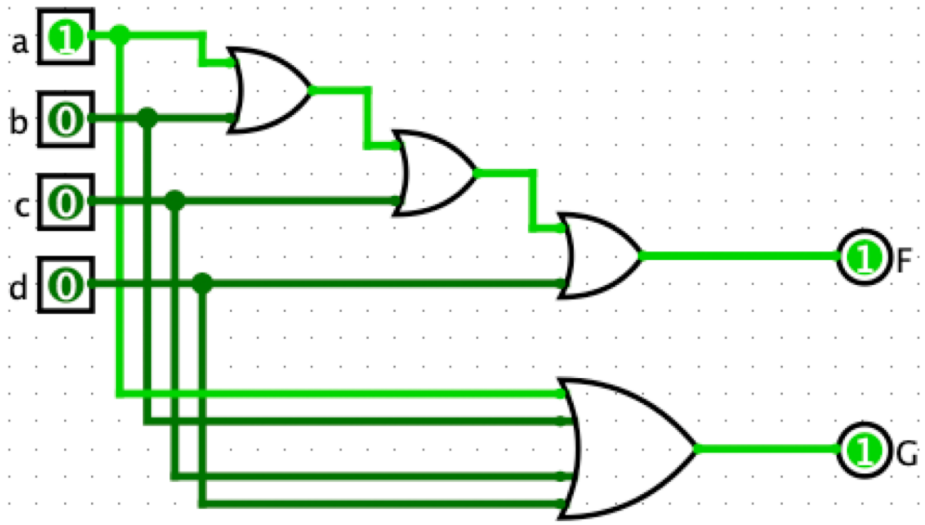
more realistic

with delay but otherwise ideal

Gate Delay

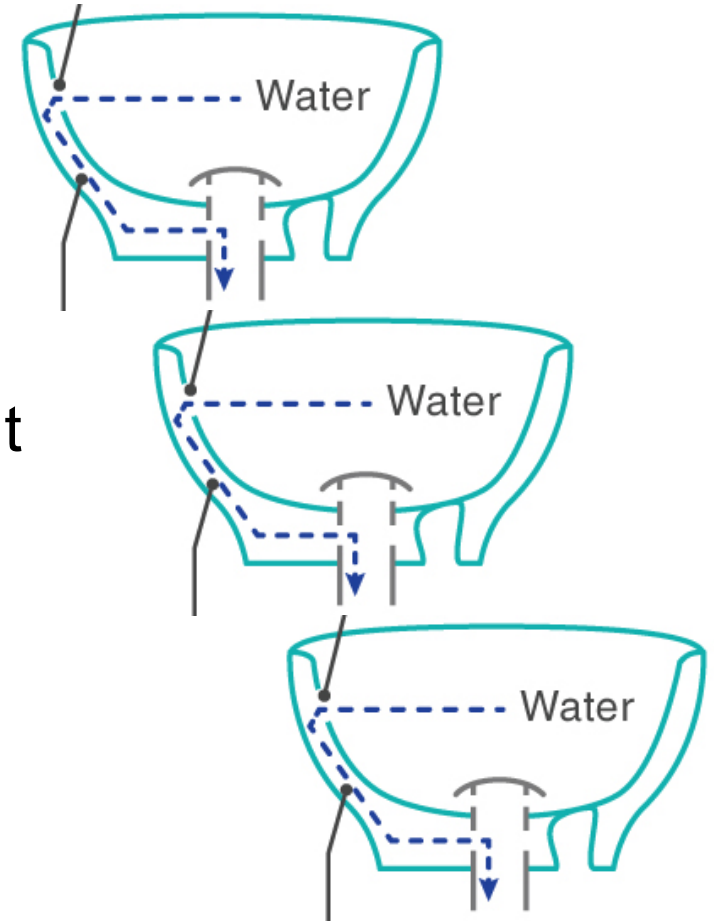
- Output F and G have identical behavior from a logic perspective
  - F = G = a+b+c+d
- However, the output changes at different speeds
  - If **a** changes: F has 3 gate delays, G only 1 gate delay





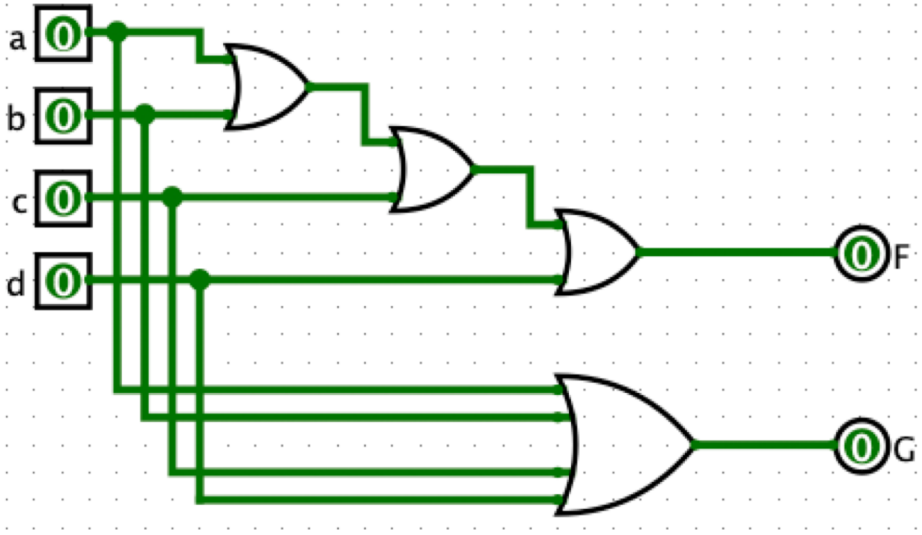
Gate Delay

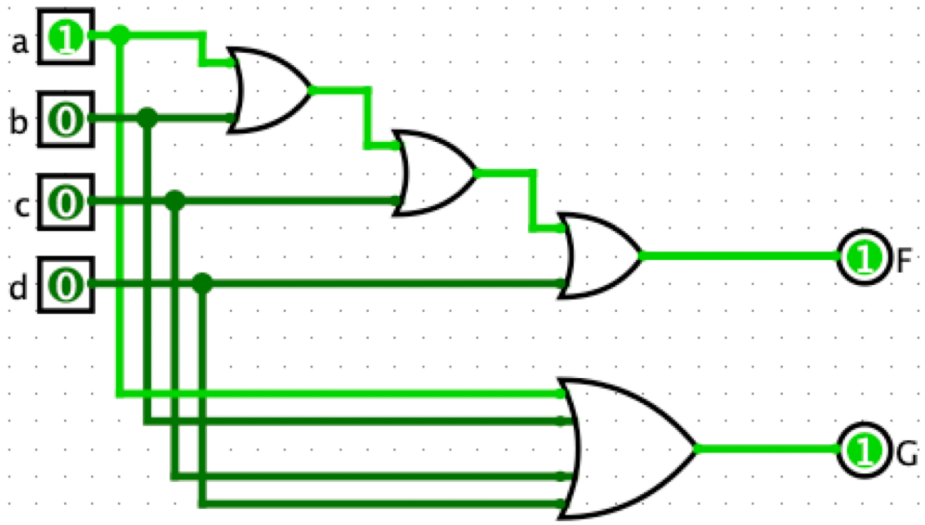
- Analogy: Circuits with multiple gates can be seen as multiple sinks chained together
  - Faucet fills the first (upper) sink
  - Overflow of first sink fills second sink
  - Overflow of second sink fills third sink
  - Overflow of third sink is our output
- Now the water takes 3 “sink delays” to reach our output



Gate Delay

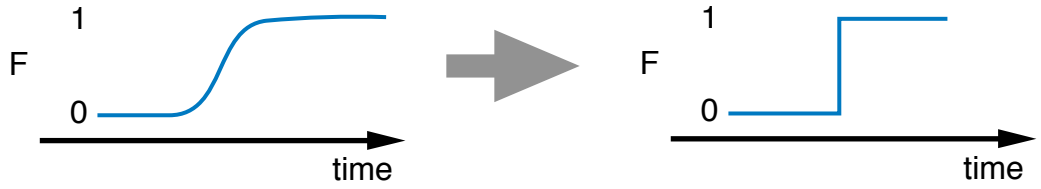
- What could we change in the circuit to make the delay of F and G equal for the case that input **a** changes?
  - Adding two NOT gates right before the G output would add 2 gate delays but not change the circuit logic





Gate Delay

- A large reason why your CPU has a maximum clock frequency
  - If the CPU doesn't wait long enough then input signals don't have time to travel through all of the gates and reach outputs
  - This is one source of instability that prevents further overclocking
- Part of overclocking: Increasing CPU voltage, which speeds up reaction time of gates (reduces the gate delay slightly)
- Select side effects of higher voltage:
  - more heat
  - higher risk of permanently damaging transistors
  - faster wear of transistors



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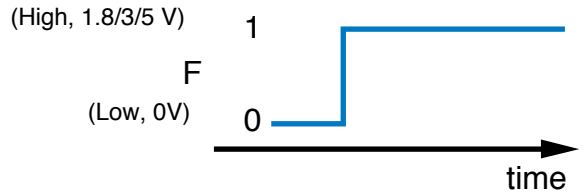
Topics

- Timing Diagram

Timing Diagram

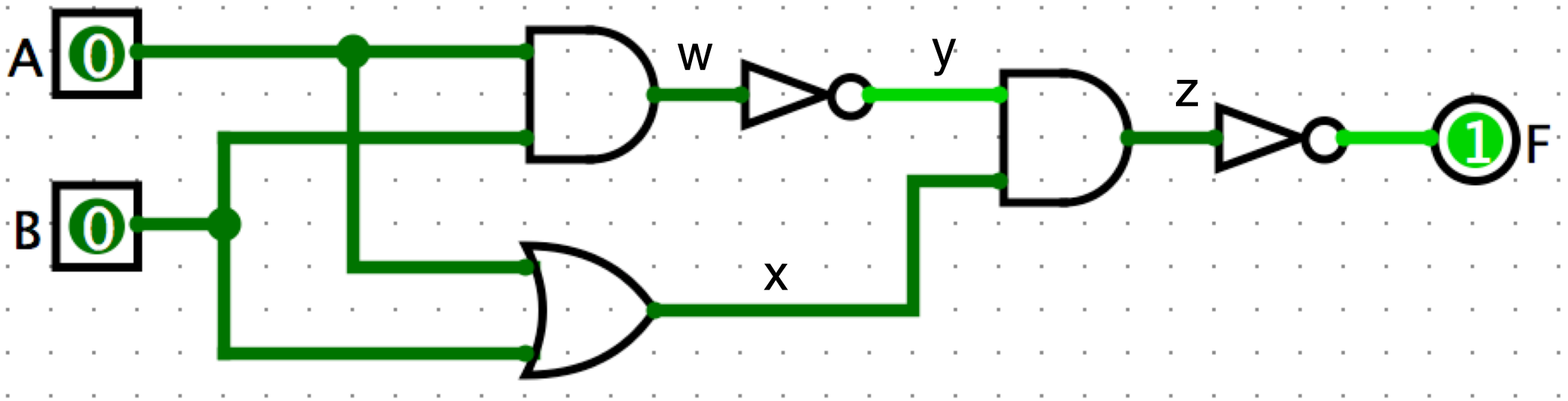
- Timing diagram can show circuit inputs, outputs and intermediate values
- Shows circuit state(s) over time
- Can make gate delays visible



- Assumptions:
  - All gates have the same delay
  - Wires do not have any delay

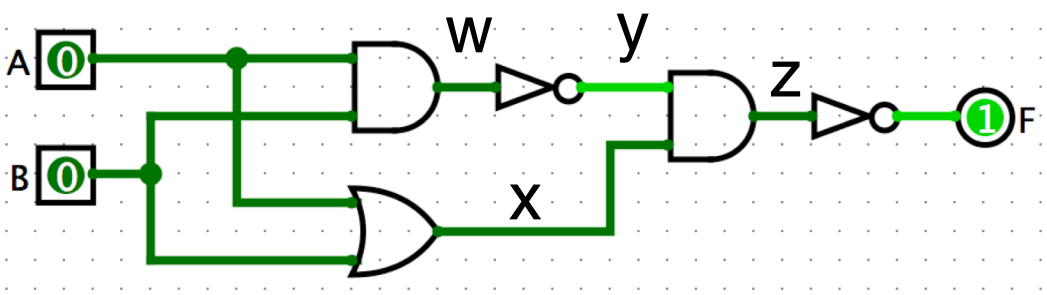
Timing Diagram

- Create a timing diagram with gate delays for the change **`A=0,B=0`** to **`A=1,B=0`** with the following circuit:
  - Include `A,B,w,x,y,z,F` in your diagram



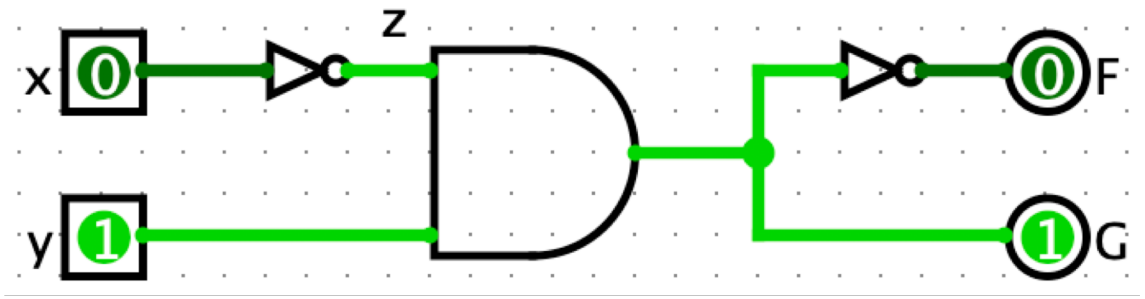
Timing Diagram

- Change **`A=0,B=0`** to **`A=1,B=0`**



Timing Diagram

- Create a timing diagram with gate delays for the change **`x=0,y=1`** to **`x=1,y=1`** with the following circuit
  - Include `x,y,z,F,G` in your diagram



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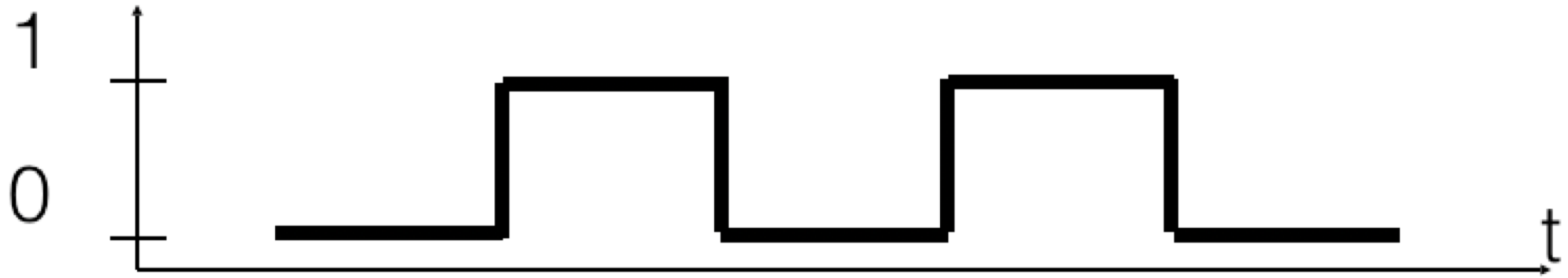
Topics

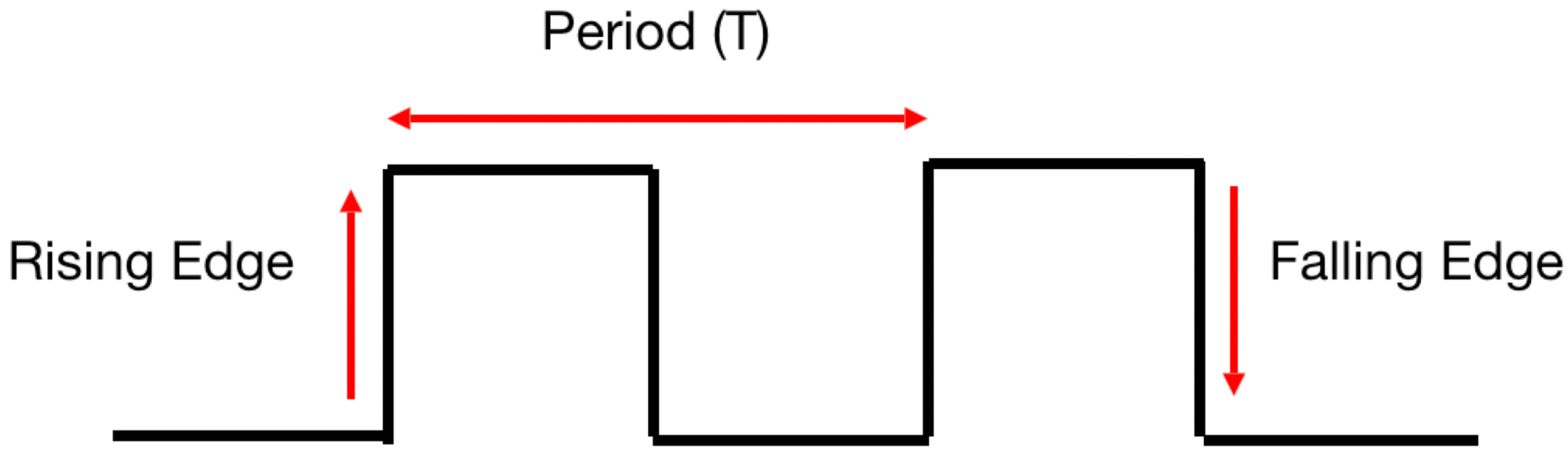
- Clock

Clock Signal

- A signal that oscillates between high and low
    - Used to synchronize circuits



Clock Signal Definitions



Clock Frequency & Period

- Clock frequency tells us how many clock periods will happen per second
  - Modern CPUs typically have clock speeds of 1 to 4 GHz (billion clock periods per second)
- Conversion between period (T) and frequency (f):
  - Frequency: f = 1/T
  - Period: T = 1/f
- Important: convert values to base units (Hz and s) before calculating

- Example 1: f = 3.4 GHz = 3,400,000,000 Hz = $3.4 * 10^9$ s
  - T = 1/ 3,400,000,000 Hz = 0.000000000294118 s = 0.294118 ns (10^{-9}s)
- Example 2: T = 87 ns
  - F = 1 / ($87 * 10^{-9}$ s) = 11,494,252.87 Hz = ~11.49 MHz

Why Have a Clock?

- This is our solution to **gate delay**
  - Period of the clock signal needs to be longer than the longest delay between an input and an output