If a 32 bit microprocessor system is designed to access a memory system of total of 256 K bytes what is the Data Bus and the Address Bus lengths of the system. If this micro processor can bring 4 bytes at a time.

Solution
DataBus length = 32=4*8=4*bytes=32 bits width of data bus
AddressBus length = 16, as memory it 2^18 bytes, 256KB, as we access 4 bytes at one time, then we need 16 bits address bus

Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long and 40% are only 8 bits long.

i) Which micro-processor will give better performance.
ii) Calculate the improvement achieved when fetching instructions and operands with micro processor you mentioned in part i.

i- the 32 micro processor gives better performance 1 point

ii- Consider a mix of 100 instructions and operands. On average, they consist of 20 32-bit items, 40 16-bit items, and 40 bytes. The number of bus cycles required for the 16-bit microprocessor is (2 × 20) + 40 + 40 = 120. For the 32-bit microprocessor, the number required is 100. This amounts to an improvement of 20/120 or about 17%. 5 point

3.2 (6 points) Consider two microprocessors having 8 and 16 bit wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.

i) Suppose all instructions and operands and instructions are two byte long. By what factor do the maximum data transfer rate differs
ii) Repeat part i assuming half of the operands and instructions are one byte long and the other half is two byte long.

a. During a single bus cycle, the 8-bit microprocessor transfers one byte while the 16-bit microprocessor transfers two bytes. The 16-bit microprocessor has twice the data transfer rate. 3 points

b. Suppose we do 100 transfers of operands and instructions, of which 50 are one byte long and 50 are two bytes long. The 8-bit microprocessor takes 50 + (2 x 50) = 150 bus cycles for the transfer. The 16-bit microprocessor requires 50 + 50 = 100 bus cycles. Thus, the data transfer rates differ by a factor of 1.5. 3 points

Consider a hypothetical microprocessor having 32 bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

i) What is the maximum directly addressable memory capacity (in bytes)
ii) Discuss the impact on the system speed if the microprocessor bus has
    (a) A 32 bit local address bus and a 16 bit local data bus
    (b) A 16 bit local address bus and a 16 bit local data bus.
iii) How many bits are needed for the program counter and the instruction register?

i. 2^{24} = 16 Mbytes 2 points

ii. **(a)** If the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory. However, because the data bus is only 16 bits, it will require 2 cycles to fetch a 32-bit instruction or operand. 3 points

(b) The 16 bits of the address placed on the address bus can't access the whole memory. Thus a more complex memory interface control is needed to latch the first part of the address and then the second part (because the microprocessor will end in two steps). For a 32-bit address, one may assume the first half will decode to access a "row" in memory, while the second half is sent later to access a "column" in memory. In addition to the two-step address operation, the microprocessor will need 2 cycles to fetch the 32 bit instruction/operand.

3 points

iii. The program counter must be at least 24 bits. Typically, a 32-bit microprocessor will have a 32-bit external address bus and a 32-bit program counter, unless on-chip segment registers are used that may work with a smaller program counter.

If the instruction register is to contain the whole instruction, it will have to be32-bits long; if it will contain only the op code (called the op code register) then it will have to be 8 bits long.
4 points