# SER232 - Assignment 5

[10 Points]

## Description

This assignment covers the different variants of memory: SR Latch, Level-Sensitive SR Latch, D Latch, D Flip Flop, Register.

In this assignment you will create each of those memory variants as a circuit by reusing the previous one. Ultimately, you will create your own 12-bit register.

## Tasks

The goal is to create an 12-bit register from scratch, using only the three basic logic gates (inverting inputs of AND, OR gates is allowed, since this simply adds a NOT gates in front of the respective input; also a NOR gates (OR and NOT gate chained together) are okay to use). All necessary labels are given in the *Important* section below.

1. Create a subcircuit called "SR Latch" and add the circuit for the SR latch.
2. Create a subcircuit called "Level-Sensitive SR Latch". Add "SR Latch" as subcircuit(s) and the required circuit around it to create a level-sensitive SR latch.
3. Create a subcircuit called "D Latch". Add "Level-Sensitive SR Latch" as subcircuit(s) and the required circuit around it to create a D latch.
4. Create a subcircuit called "D Flip Flop". Add "D Latch" as subcircuit(s) and the required circuit around it to create a D flip flop.
5. Create a subcircuit called "6-Bit Register". Add "D Flip Flop" as subcircuit(s) and the required circuit around it to create an 6-bit register. Use one 6-bit input and one 6-bit output. You will have to use splitters to connect everything to the input/output.
6. Create a subcircuit called "12-Bit Register". Add two "6-bit Register" as subcircuit(s) and the required circuit around it to create an 12-bit register. Use one 12-bit input and one 12-bit output. You will have to use splitters to connect everything to the input/output.
7. Create a verification circuit with the name "Erinaceous" (you can rename the "main" circuit). Add your "12-Bit Register" and one instance of the Logisim built-in 12-bit register (can be found in folder "Memory"; make sure to change the *data width* accordingly). Create one 12-bit input (label: i) and connect it to the two registers in parallel. If both registers are connected in parallel, they share the same inputs, but have each their own outputs.

8. Connect the output of each register to a splitter, which splits the 12-bit bus into three 4-bit busses (bit 0-3, bit 4-7 and bit 8-11). Then, add three hex digit displays for each splitter and connect one to each of the splitter fanout. Make sure to order the hex displays so the rightmost display shows the 4 LSB and the leftmost display the 4 MSB. This is important, since you want to confirm that both registers behave the same (for identical inputs).

9. Test your verification circuit created in the previous step to confirm that both registers behave exactly the same (hex displays show the same value and change at the same time).

**Important:**

- You are not allowed to use any of the built-in components in Logisim, except one 12-bit register in the main/verification circuit. **Note:** Wires, splitters, inputs, outputs, clocks are considered *wiring components* and can be used!
- Use the slides as reference for the circuits you have to create. You do not need to research anything outside of the course material.
- The output Q' or t (inverted value of the stored bit) is not necessary for this assignment. Feel free to omit it. If you are adding Q' as an output (optional), make sure to use the correct output when using it as a subcircuit somewhere else.
- For the clock input: You can either use a "manual clock" (1-bit input) and toggle it by hand or use the element "Clock" (can be found in folder "Wiring"). To enable the clock element, go to "Simulate" and click "Ticks Enabled". Make sure to adjust the "Tick Frequency" to an appropriate speed that allows you to compare your register to the built-in one (e.g. 0.5 Hz or 1 Hz).
- Place the clock only in the verification circuit and pass it into the components that need it.
- You must use the following labels:
  - S, R, Q for SR latch and additionally C for level-sensitive SR latch
  - D, C, Q for D latch
  - D, Clk, Q for D flip flop
  - i, Q, Clk for the register

## Deliverables

The deliverables must be submitted on Canvas before the due date as a single submission:

1. Submit your circit as *.circ*, named: *lastname_a5.circ*