SER 232 - Assignment 2 Example

Description

This assignment will introduce the use of logic gates in a circuit and practice converting between different circuit representations. The goal of this assignment is to create derive Boolean equations from a given truth table and then use those to create a circuit, which behaves as described in the table.

Tasks

For this assignment, do the following:

1. Derive the Boolean equations from the truth table below. You need to execute the conversion process once for each output. This will yield one Boolean equation for each output of the circuit.

2. Convert the Boolean equations to a circuit in Logisim. Name the circuit "Green Spaghetti".

3. Use the "Simulation Tool" (hand cursor in the top left; this allows you to change the value of any input) and verify that the circuit behaves as the truth tables indicates: Change the input values and check if the output values are as stated in the respective row of the truth table. Test all possible input combinations to verify the entire circuit behavior.

Any wire can be branched and connected to multiple components at the same time. Simply click on an existing wire and drag the new wire to the second "target" component.

Tip: You can re-use duplicate terms / gates between the equations.

Deliverables

Submit the following deliverables on Canvas in *Module 2* before the due date (see Canvas):

1. Submit your document file containing the Boolean equations and a screenshot of your circuit as a .pdf with the following naming convention: *lastname_a2.pdf*

2. Submit your Logisim file with the following naming convention: *lastname_a2.circ*

Important: Make sure to submit both files in one submission. Only the files of the last submission will be graded. If one is missing, you will receive 0 points for the missing part.

w	x	y	z	F2	F1	F0
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	0	0	1
1	0	1	0	0	0	0
1	0	1	1	0	0	1
1	1	0	0	1	0	1
1	1	0	1	0	1	0
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Figure 1: Truth Table - inputs are lower case, outputs are upper case