Gate Delay & Clocks

Module 4

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Key Takeaways

Gate Delay

Characterizing Circuits

Timing Diagrams

Identifying Intermediate Values

Clocks

Calculating Periods and Frequencies

GATE DELAY

Longest Path

- A theoretical "upper bound" on the delay of a circuit.
- The greatest number of gates from any input to any output.

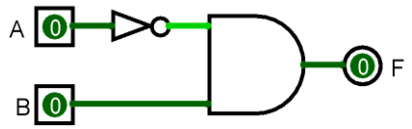
Shortest Path

- A theoretical "lower bound" on the delay of a circuit.
- The least number of gates from any input to any output.

Useful Notes

- Longest Paths and Shortest Paths are unrelated to specific input changes and unrelated to Timing Diagrams.

- You can rule out some inputs by noticing that another input will include more or less gates. (For example, the longest path will never include Input B, since a path including Input A will always be longer)



GENERAL CONCEPTS

1. Gates require time to "process" their inputs

2. Assumptions made in the context of this course:
   - All gates have identical delays
   - Wires do not have delays

3. Longest Path and Shortest Path are "properties" of a circuit as a whole

TIMING DIAGRAMS

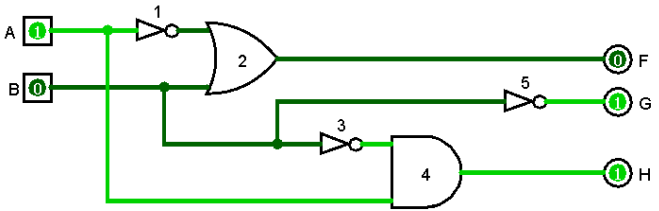
Setting up the Timing Diagram

1. Identify all Inputs, Outputs, and Intermediate Variables
2. Identify the initial values of all of these variables

Identifying Synchronous Gate Delays

1. When a wire changes value, follow the wire to ALL gates
2. Any and all gates (no matter how long the wire is) you reach will introduce simultaneous gate delays

For Example: In the following circuit diagram, the delays from gates 2, 3, and 5 occur simultaneously after the input changes from AB = 10 to AB = 11



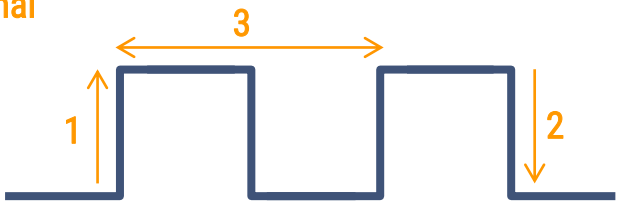
DON'T FORGET

1. Timing Diagrams describe the dynamic behavior of a circuit given a change of state. There is no single timing diagram for a circuit
2. We are assuming that all gates have identical delays and that wires do not have delays
3. Timing Diagrams are a separate concept from Longest/Shortest Paths
4. Logisim's wire coloring can be very helpful in identifying initial and intermediate values

CLOCKS

Describing the Clock Signal

1. Rising Edge
2. Falling Edge
3. Period
4. Takes a value of 0 or 1



Converting between Period and Frequency

1. Convert to base units (Hz and seconds)
2. Use the Period = 1 / Frequency relationship
3. Convert to the requested units

Pico (p)	10^{-12}
Nano (n)	10^{-9}
Micro (μ)	10^{-6}
Milli (m)	10^{-3}

Kilo (K)	10^{3}
Mega (M)	10^{6}
Giga (G)	10^{9}
Tera (T)	10^{12}

DON'T FORGET

1. Converting to base units (Hz and seconds) first is often a fool proof method
2. Clocks can be used to synchronize circuits
3. Clocks are the solution to Gate Delay
4. Period = 1 / Frequency

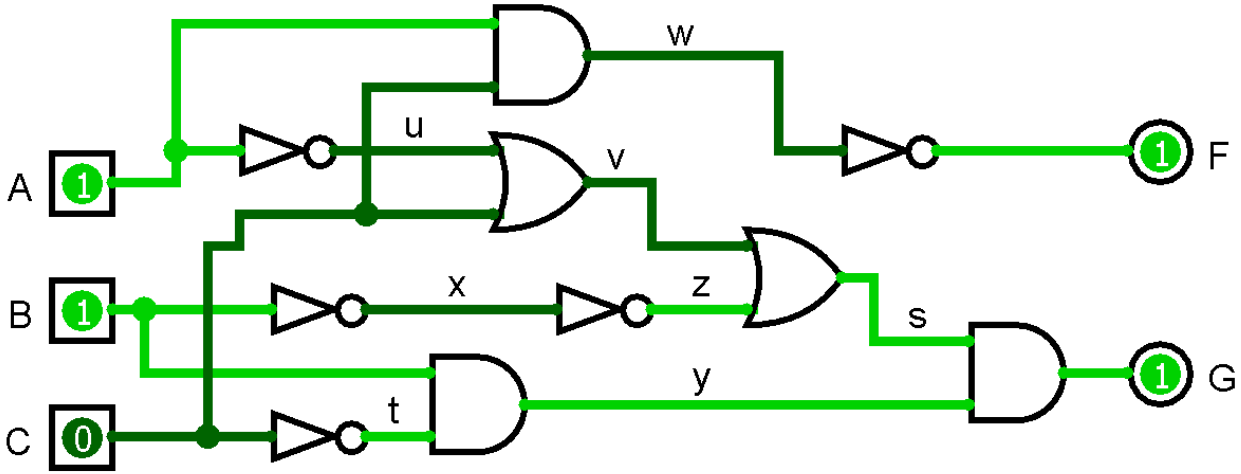
Practice Problems Conversions

1. Convert the **Frequency of 200 Hz** to a **Period in nanoseconds**.
2. Convert the **Frequency of 490 kHz** to a **Period in picoseconds**.
3. Convert the **Frequency of 4.5 GHz** to a **Period in seconds**.
4. Convert the **Frequency of 0.1 MHz** to a **Period in microseconds**.
5. Convert the **Period of 500 nanoseconds** to a **Frequency in MHz**.
6. Convert the **Period of 4,500 microseconds** to a **Frequency in Hz**.
7. Convert the **Period of 24 seconds** to a **Frequency in GHz**.
8. Convert the **Period of 60,000 picoseconds** to a **Frequency in MHz**.

Practice Problems Timing Diagram

9. What is the **longest path** and **shortest path** in the following circuit?

10. Create a **Timing Diagram** for the following circuit's input change of **ABC = 110** to **ABC = 100**.

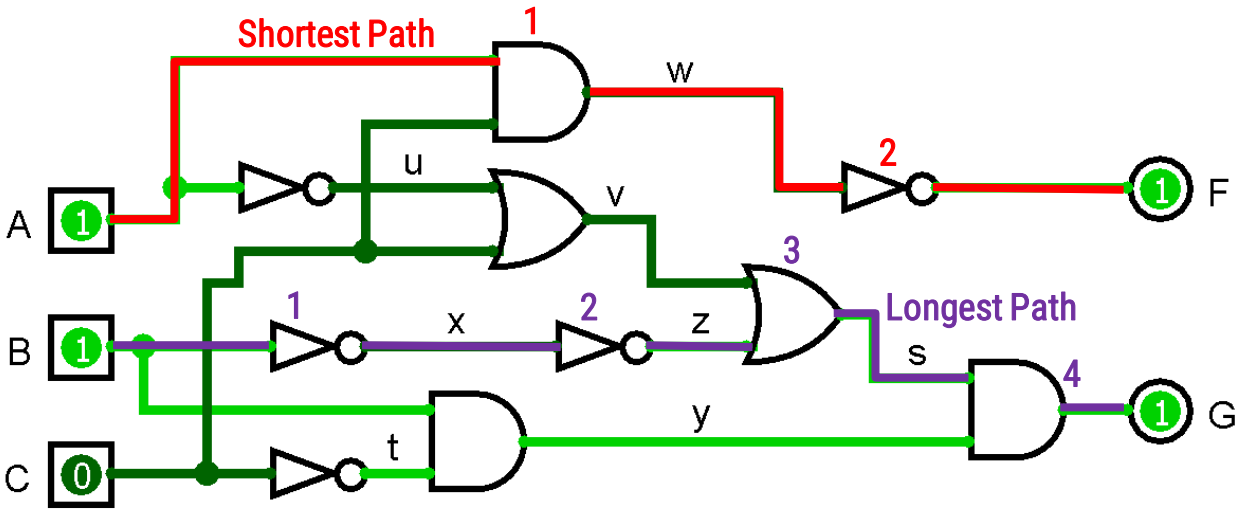


Practice Problems Answers

1. 5×10^{6} **ns**
2. 2.04×10^{6} **ps**
3. 2.22×10^{-10} **s**
4. 10 **µs**
5. 2 **MHz**
6. 222.22 **Hz**
7. 4.17×10^{-11} **GHz**
8. 16.67 **MHz**

Practice Problems Answers

9. Longest Path = **4 Gate Delays**
   Shortest Path = **2 Gate Delays**



Practice Problems Answers

10.