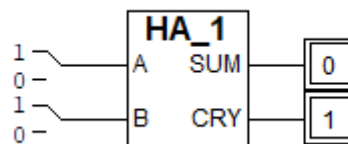
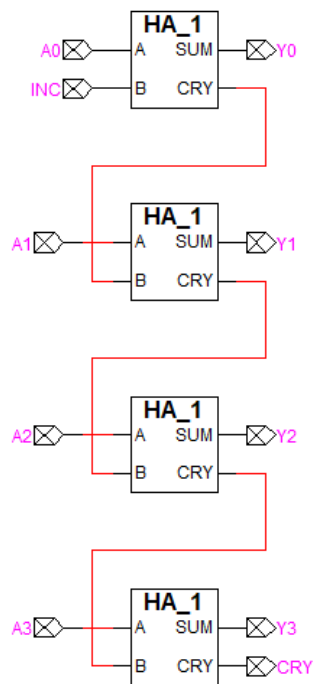


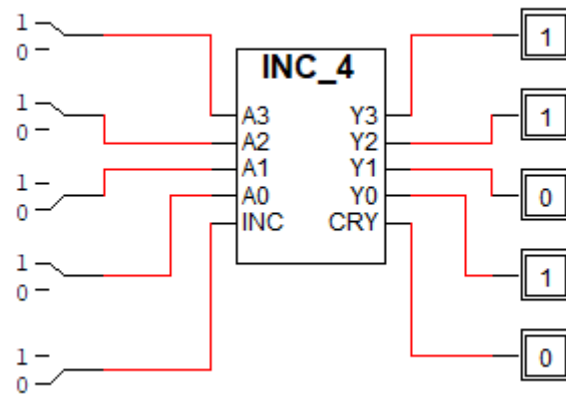
1-Bit Half-Adder



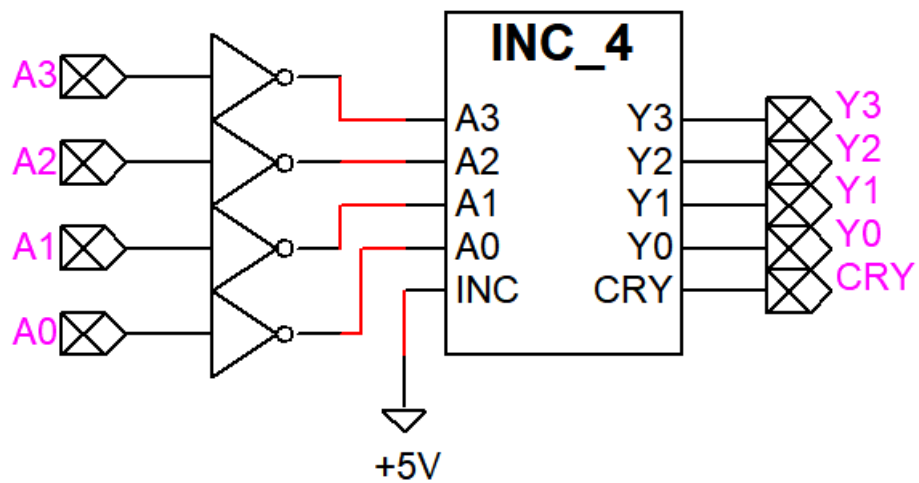
1-Bit Half-Adder subcircuit



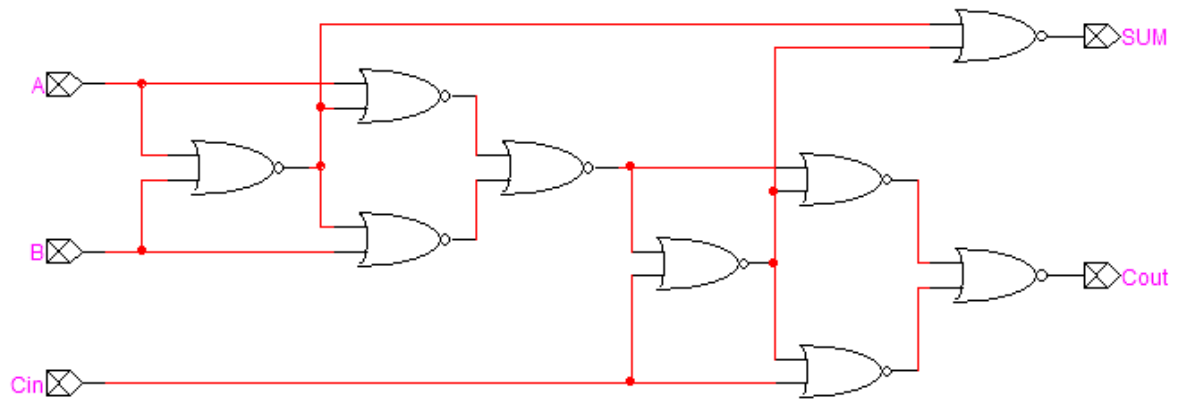
4-Bit Increment Circuit



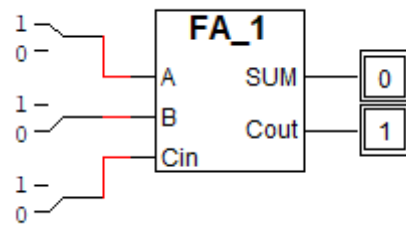
4-Bit Increment subcircuit



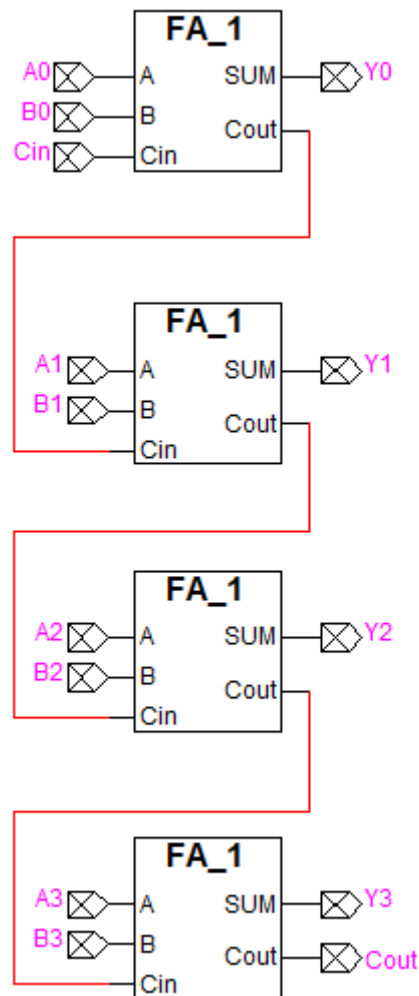
4-Usage of INC\_4 to Perform 2's-complement operation



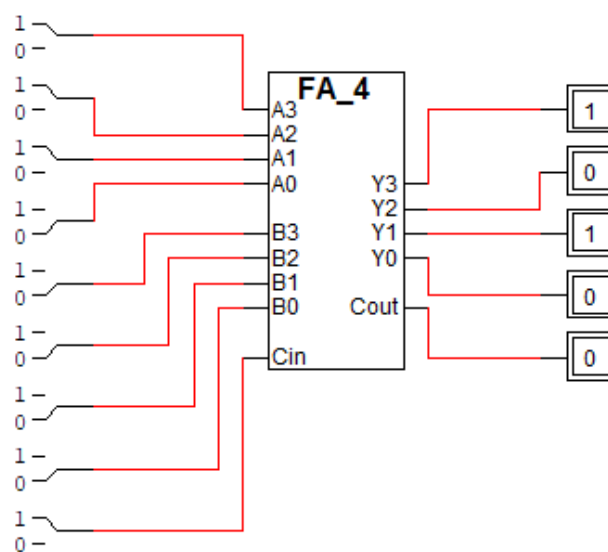
Full Adder using NOR/NOR logic



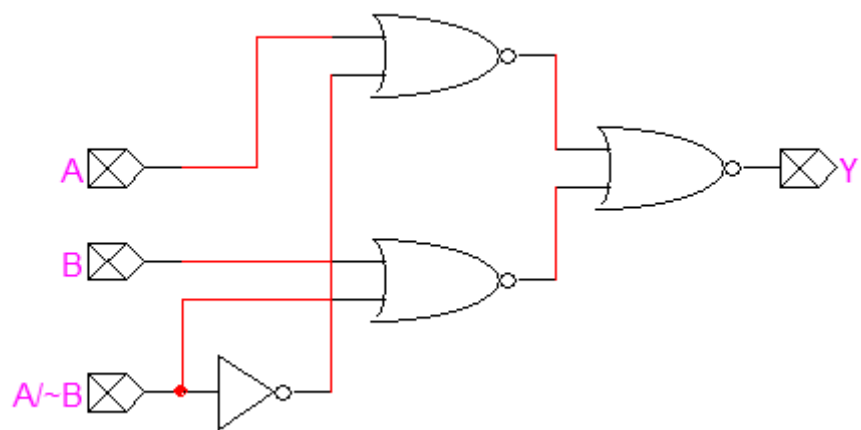
Full Adder using NOR/NOR logic subcircuit



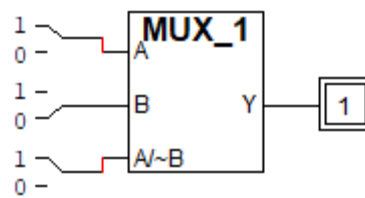
4-Bit Full Adder



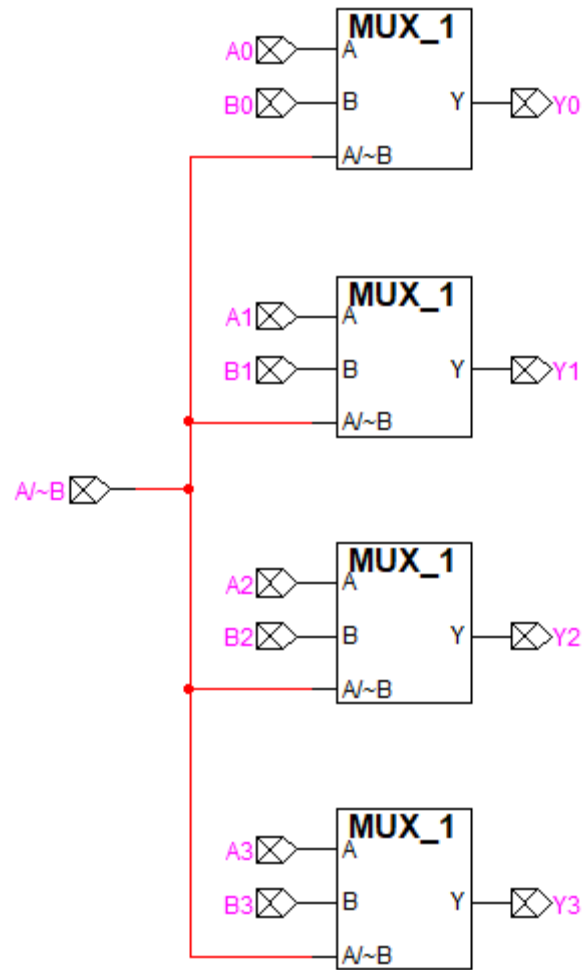
4-Bit Full Adder subcircuit



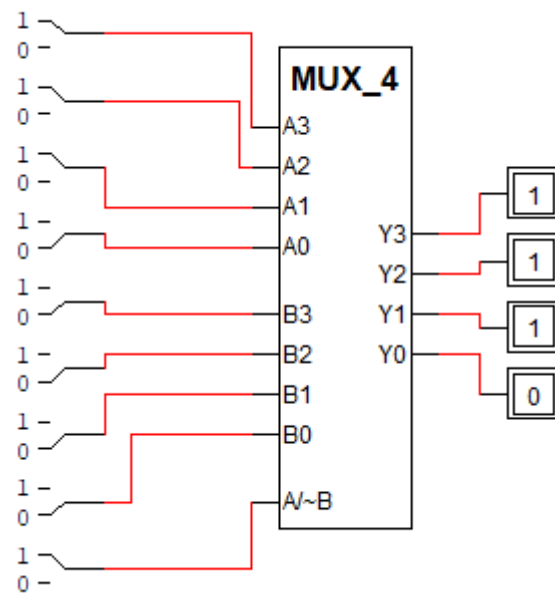
1-Bit MUX using NOR/NOR logic



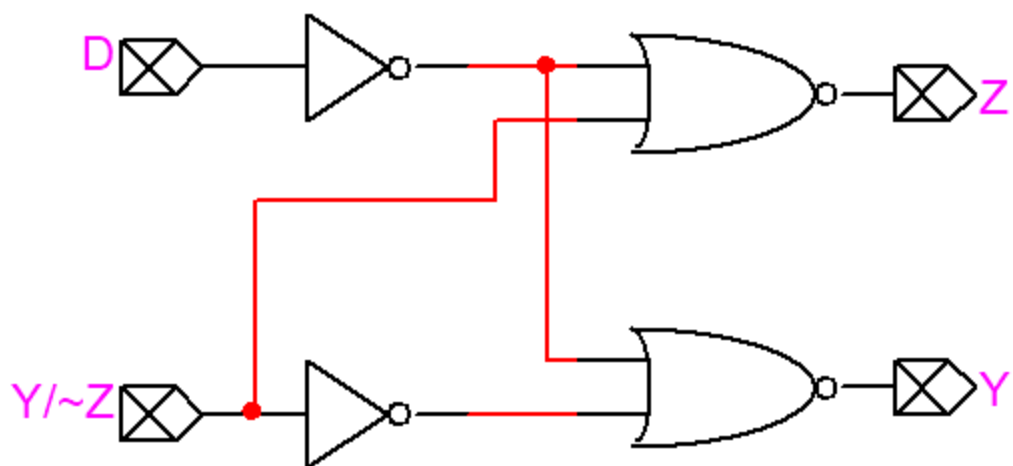
1-Bit MUX using NOR/NOR logic subcircuit



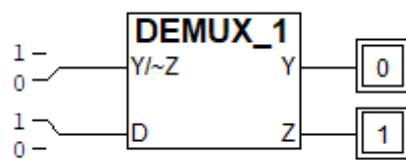
4-Bit MUX



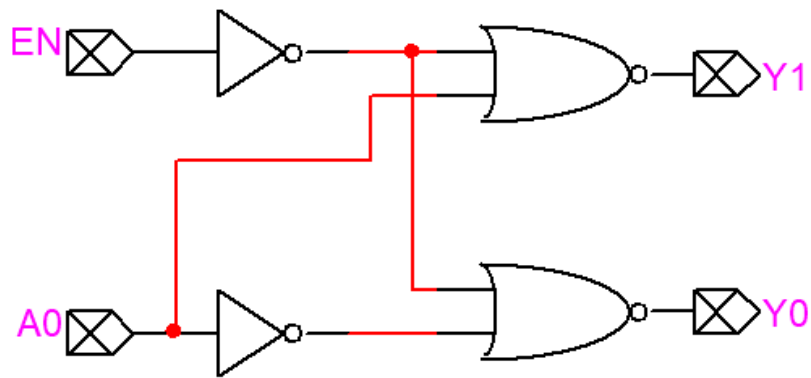
4-Bit MUX subcircuit



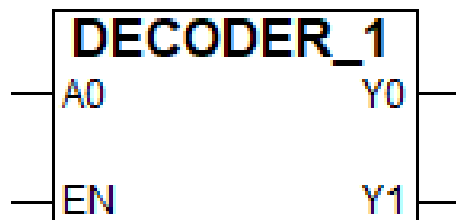
1-Bit DeMUX



1-Bit DeMUX subcircuit

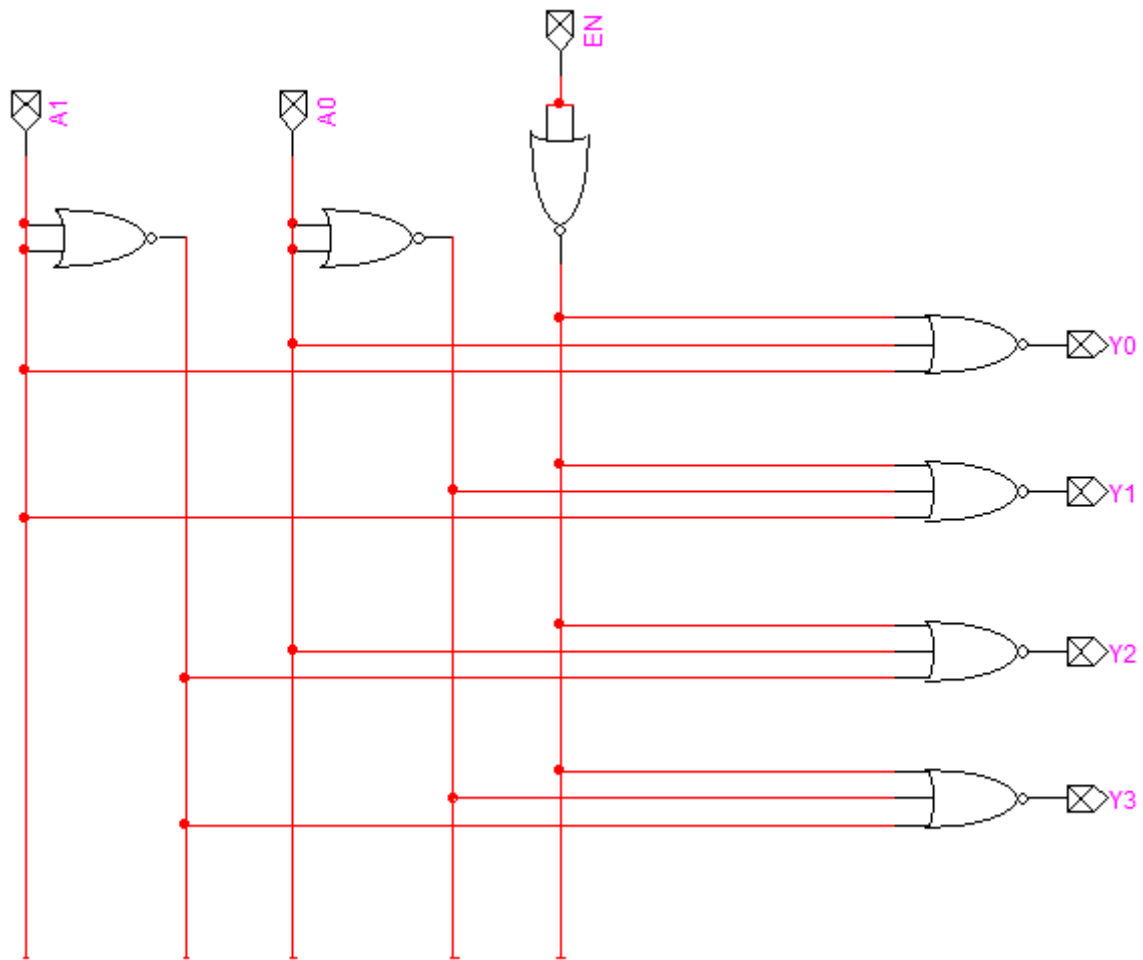


1-Bit Decoder

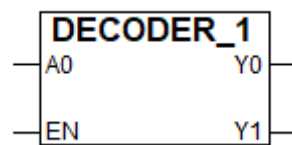


1-Bit Decoder subcircuit

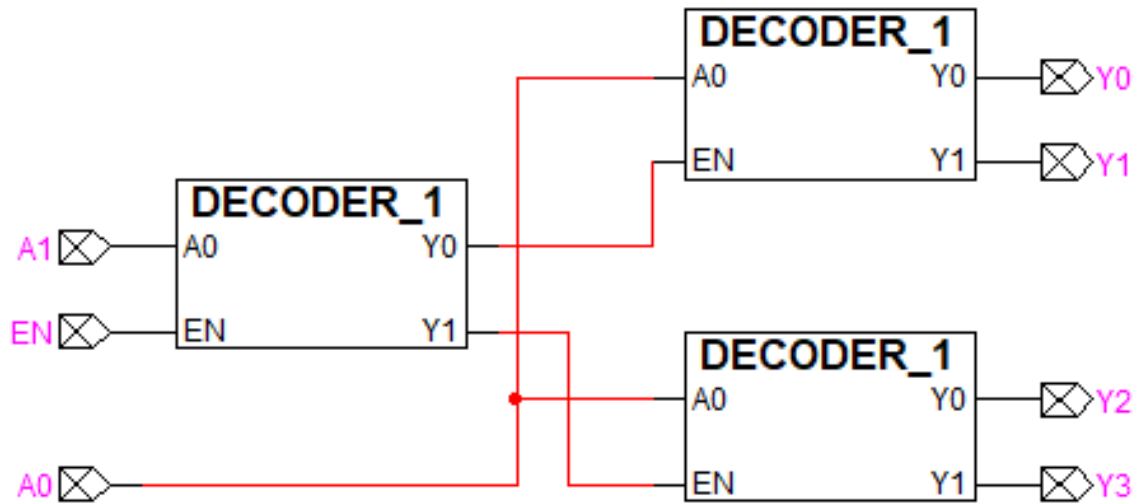




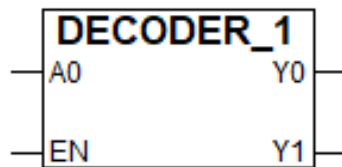
2-Bit Decoder



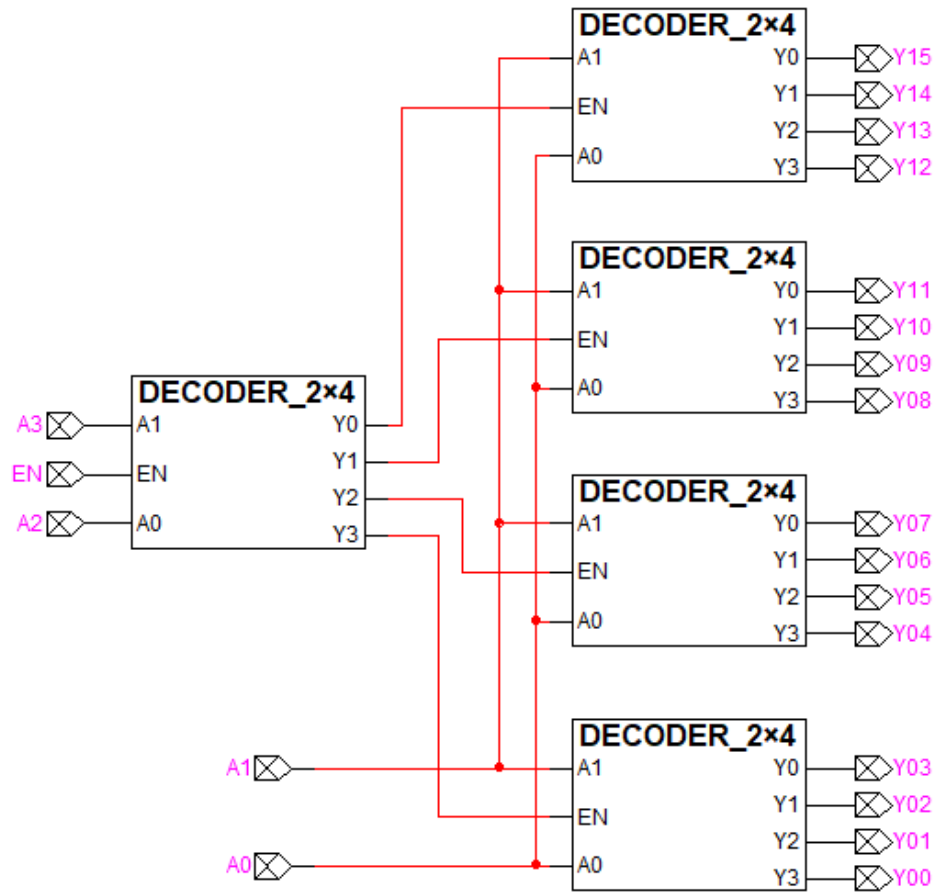
2-Bit Decoder subcircuit



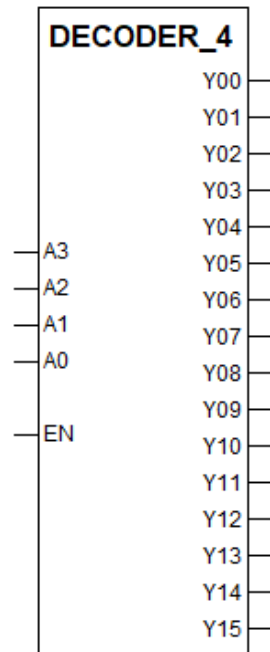
2-to-4 Decoder



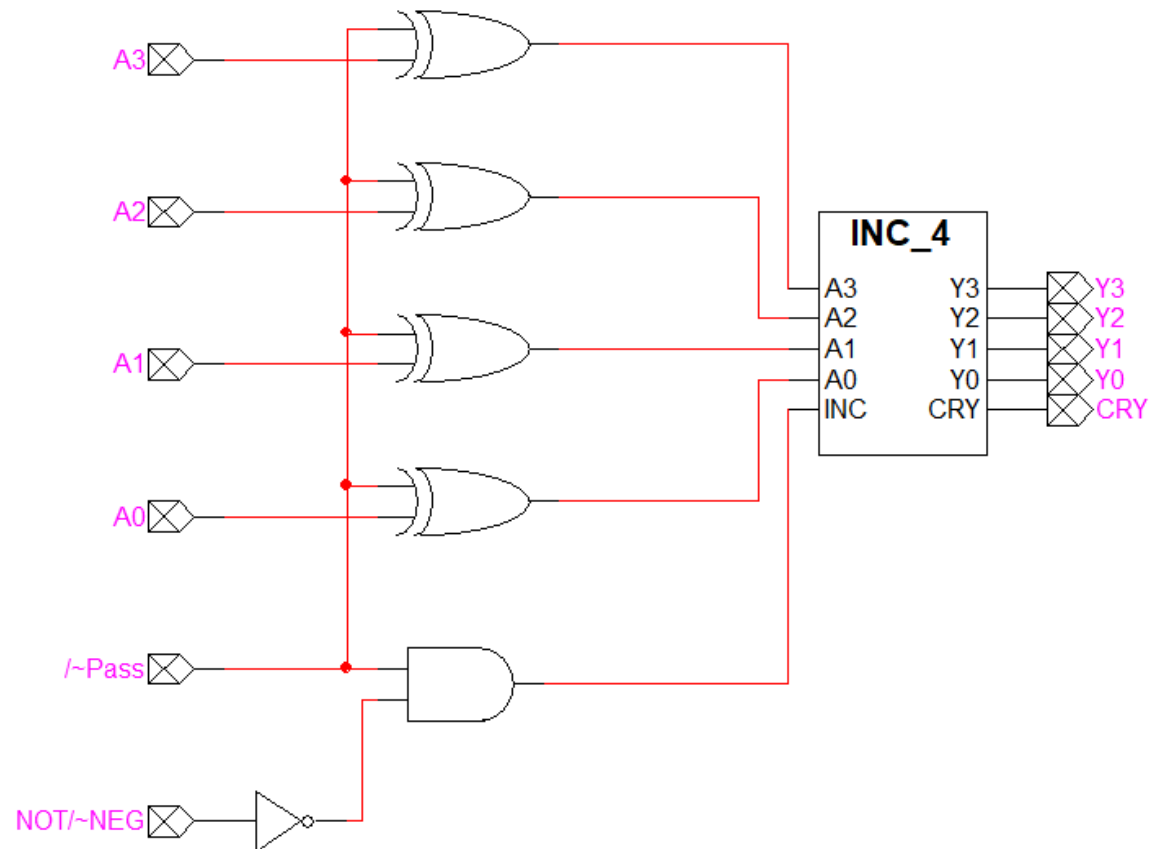
2-to-4 Decoder subcircuit



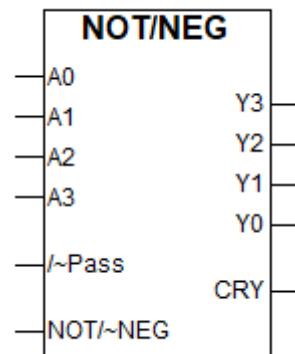
4-to-16 Decoder



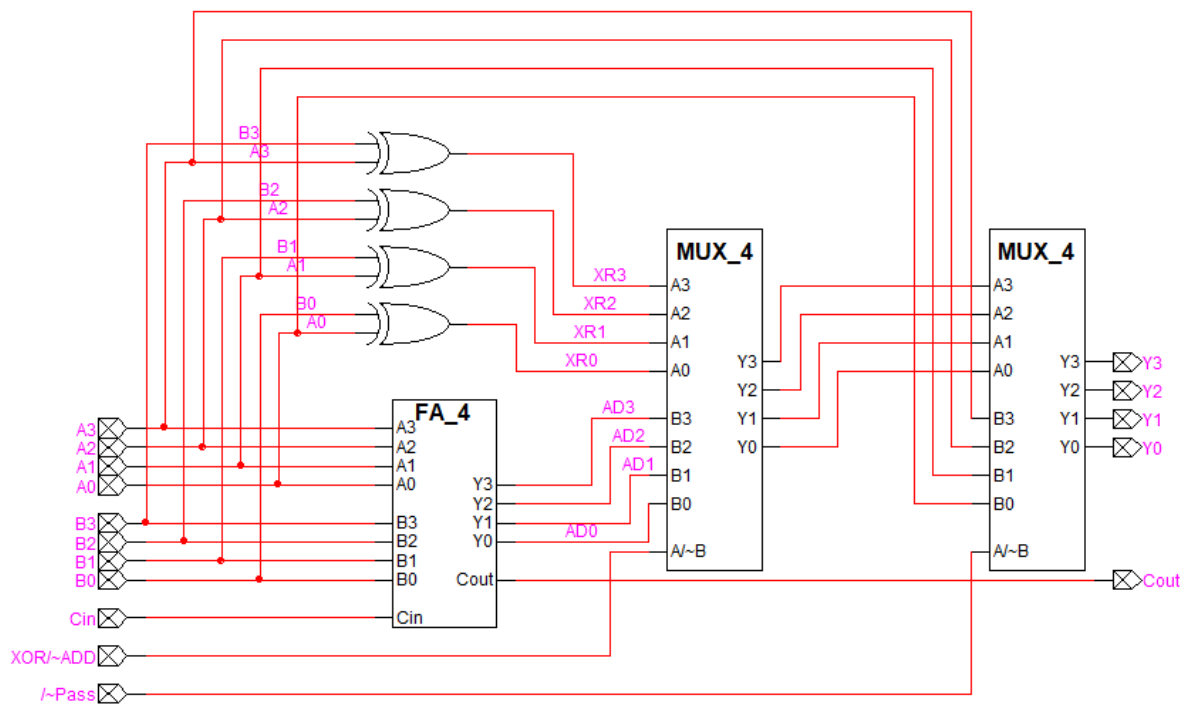
4-to-16 Decoder subcircuit



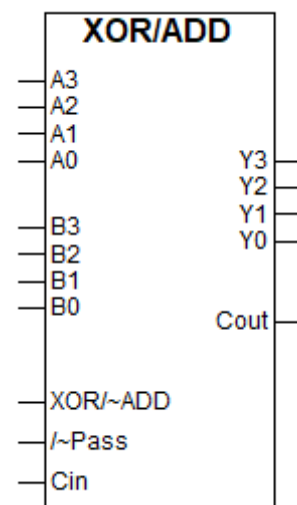
NOT/NEG circuit



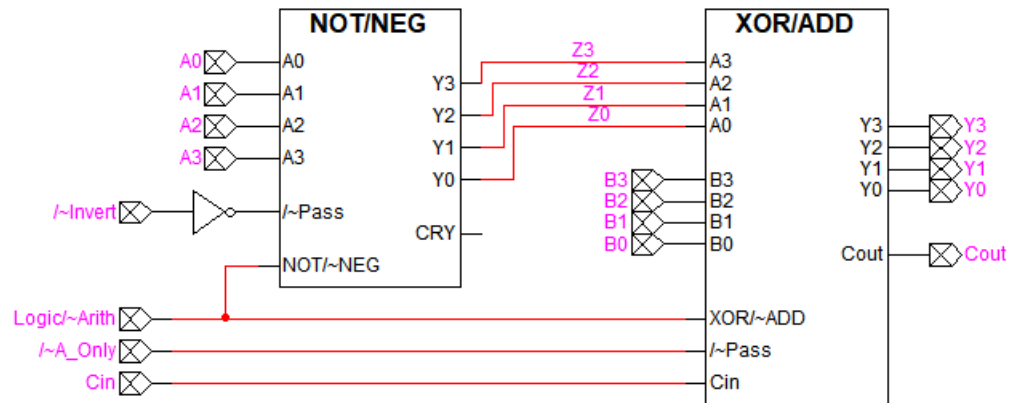
NOT/NEG subcircuit



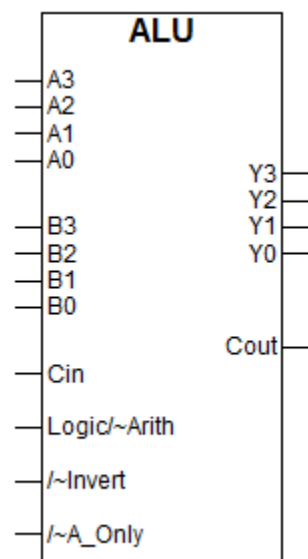
XOR/ADD circuit with pass-through



XOR/ADD circuit with pass-through subcircuit



ALU



ALU subcircuit