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Assignment 7 sol

1. For the following code on a regular RISC 5 stage pipelined processor, calculate (with a complete description of each single micro-instruction) the value of R1 and R2 at the end of the program, where R1, R2 and R3 are general purpose registers, assume the initial value in R1=5 and R2=8 and R3=3
   Justify the value obtained.

```
      ADD   R1, R3                  → R1=8
      ADD   R2, R1                  → R2=16
      IF    R2>=10      goto  AAA   → go to AAA
      ADD   R2, R3
AAA   SUB   R2, R1                  → R2=8
```

1	2	3	4	5	6	7	8	9	10
IF	ID	EX R3=3 R1=5	MEM	WB R1=8					
	IF	ID	EX R2=8 R1=5	MEM	WB R2=13				
		IF	ID	EX R2=8	MEM	WB			
			IF	ID	EX R2=8 R1=8	MEM	WB R2=0		

2. For the following so-called GU processor that consists of the following steps (micro-instructions)
   - fetch instructions from memory (IF)
   - read registers and decode the instruction (ID)
   - execute the instruction or calculate an address (EX)
   - write the result into a register (WB)
   - access an operand in data memory (MEM)

   Calculate the value in R2, and R1 at the end of the program, where R1, R2 and R3 are general purpose registers, assume the initial value in R1=5 and R2=8 and R3=5 and data at memory location A=1, if data is needed to be loaded from MDR, assume the next micro-instruction is delayed until data reaches the MDR

```
      ADD   R1, A
      ADD   R2, R1
      IF    R2>=10      goto  AAA
      ADD   R2, R3
AAA   SUB   R2, R1
```

1	2	3	4	5	6	7	8	9	10
IF	ID	EX (R1=5, A=1)	WB (R1=6)	MEM					
	IF	ID	EX (R1=5, R2=8)	WB (R2=13)	MEM				
		IF	ID	EX (R2=8)	WB	MEM			
			IF	ID	EX	WB	MEM		

					(R2=13, R3=5)	(R2=18)			
				IF	ID	EX (R2=13, R1=6)	WB (R2=7)	MEM	

3. TRUE or FALSE
    a. For a processor that receives serial data and gives out results at the same rate, it is possible and efficient to pipeline it.
    False
    b. Pipelining is a programming technique that exploits all empty registers in a processor. **False (implementation)**
    c. Stalls typically happen in a pipelining process due to increased bandwidth (increased speed) for input data.
    False
    d. Pipelining is preferred to increase the throughput for a running program.
    True

4. In the following example, detect if any type of hazard will occur, if we are dealing with the RISC architecture, initially R1=5, R2=3, R3=12, A=1

```
            ADD   R1, R2
            MOV   R2, R3
            IF    R2>=10      goto  AAA
            ADD   R1, A
            END
AAA         SUB   R1, R2
            END
```

1	2	3	4	5	6	7	8	9	10
IF	ID	EX R1=5 R2=3	MEM	WB R1=8					
	IF	ID	EX R2=3 R3=12	MEM	WB R2=12				
		IF	ID	EX R2=3	MEM	WB			
			IF	ID	EX R1=8 R2=3	MEM	WB R1=5		