Eyad Mohamed AbdelMohsen Ghanem

***Project***

A diagram of a circuit

Description automatically generated

1\_5\_HA\_1

A diagram of a computer program

Description automatically generated with medium confidence

1\_8\_INC\_4

A diagram of a rocket

Description automatically generated

2\_13\_FA\_1

A diagram of a circuit

Description automatically generated

2\_17\_FA\_4

A diagram of a circuit

Description automatically generated

2\_18\_MUX\_1

A diagram of a circuit

Description automatically generated

2\_21\_MUX\_4

A diagram of a circuit

Description automatically generated

3\_2\_NOT\_NEG

A diagram of a circuit

Description automatically generated

3\_5\_XOR\_ADD circuit with pass-through

A diagram of a circuit

Description automatically generated

3\_7\_ALU

A diagram of a computer

Description automatically generated

3\_7\_ALU\_TESTING

A diagram of a circuit

Description automatically generated

4\_2\_REG\_1

A diagram of a circuit

Description automatically generated

4\_2\_REG\_4

A diagram of a circuit

Description automatically generated

4\_5\_Three-state buffer circuit

A diagram of a circuit

Description automatically generated

4\_6\_Three-state 4-bit buffer circuit

A diagram of a computer

Description automatically generated

4\_7\_Schematic of brainless central processing unit

A diagram of a code

Description automatically generated

4\_10\_Addressing logic

A diagram of a buffet

Description automatically generated

4\_11\_4-bit ROM memory cell

A diagram of a circuit

Description automatically generated

4\_12\_4-bit output device

A diagram of a computer

Description automatically generated

4\_13\_4-bit RAM

A diagram of a machine

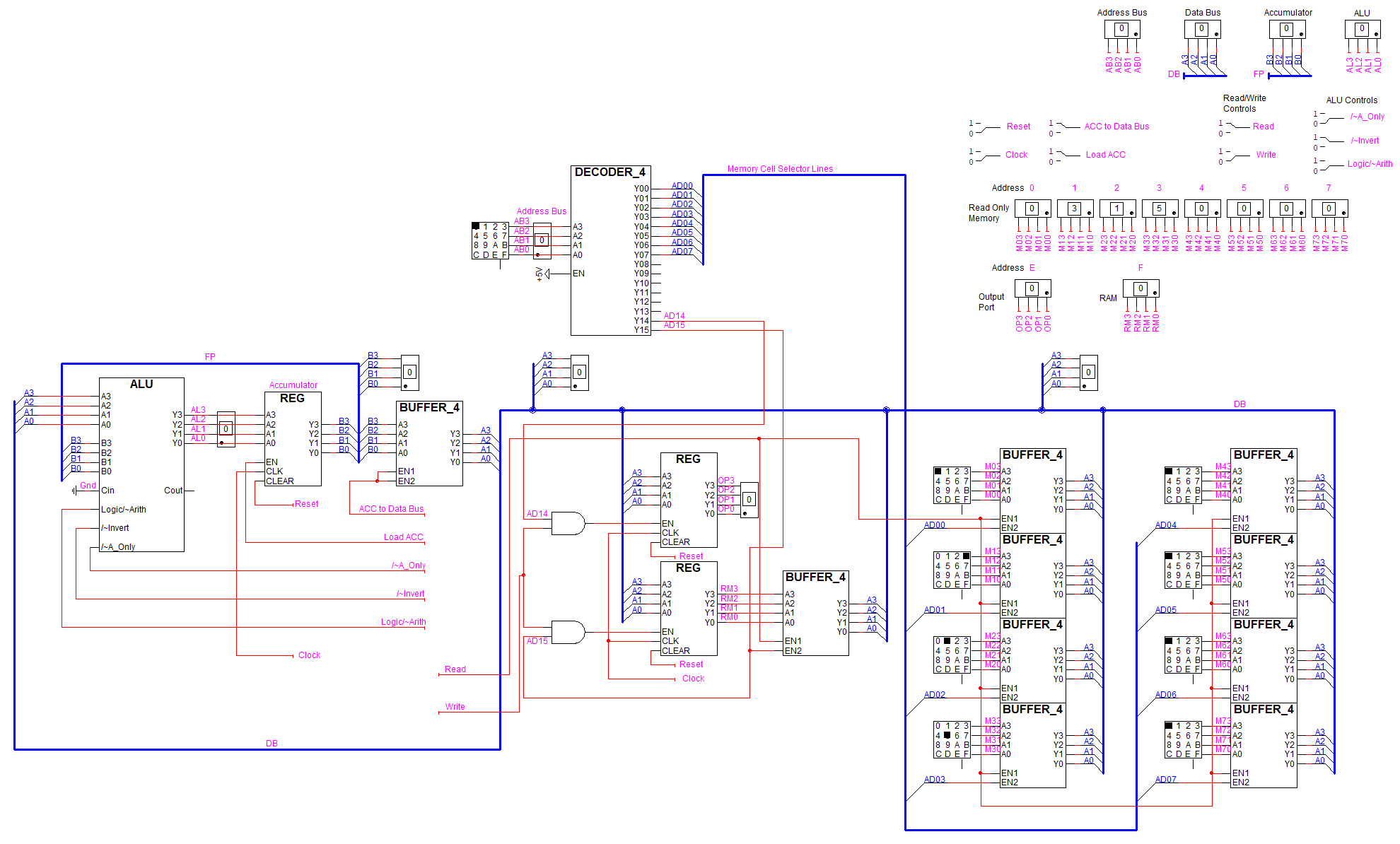
Description automatically generated

4\_15\_The brainless microprocessor

A blueprint of a house

Description automatically generated

4\_17\_Brainless microprocessor with display\_control panel



5\_2\_Schematic of brainless microprocessor showing added memory

A diagram of a program counter bus

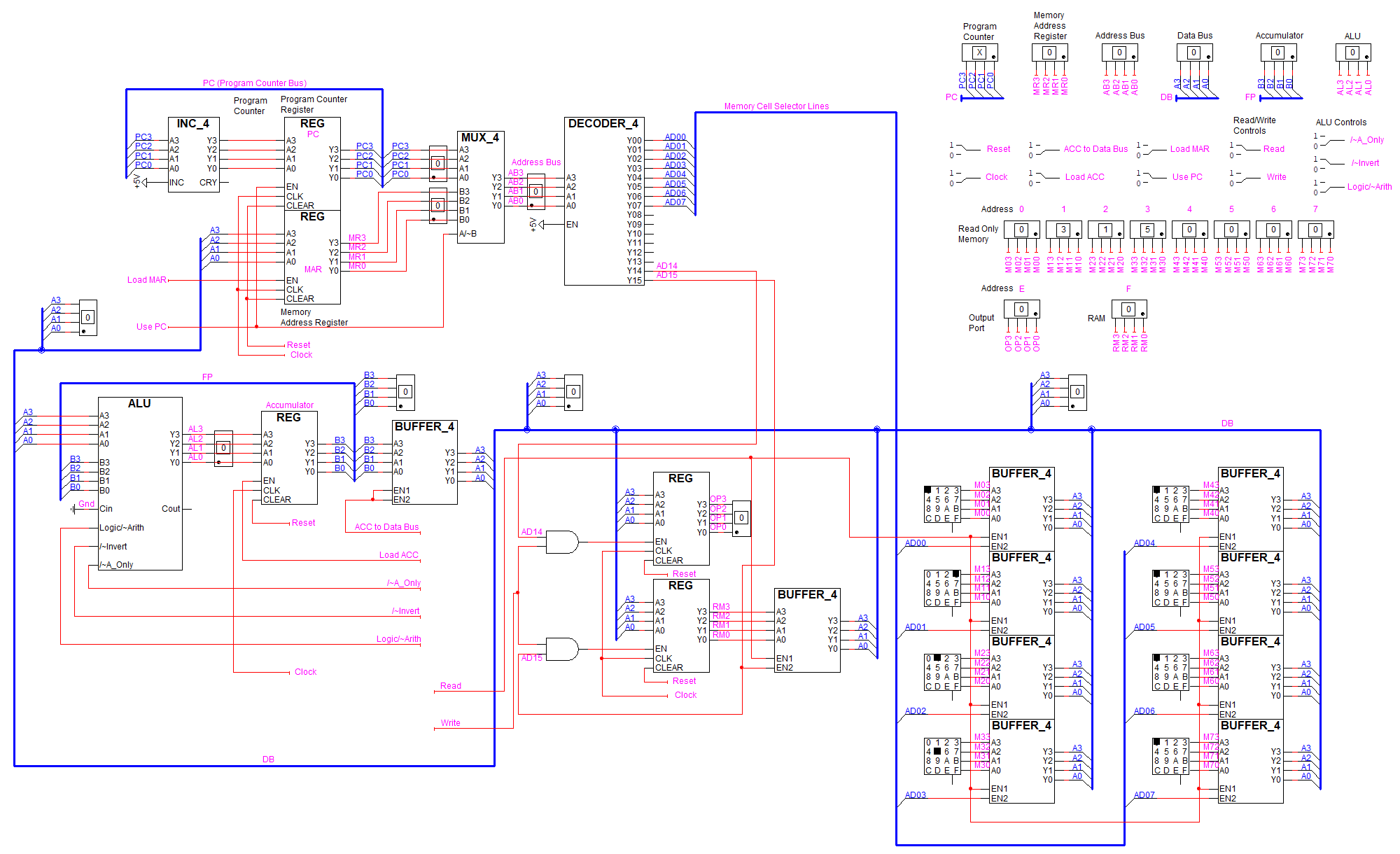
Description automatically generated

5\_4\_Memory address generation circuit

A diagram of a program counter

Description automatically generated

5\_4\_Memory address generation circuit\_TESTING



5\_5\_Schematic of brainless microprocessor emphasizing memory-address-generation circuitry

A diagram of a program

Description automatically generated

5\_10\_Microprocessor controller circuit

PROM.hex

0115 0550 0000 0000

0115 0750 0000 0000

0000 0000 0000 0000

0115 0001 0000 0000

A diagram of a program

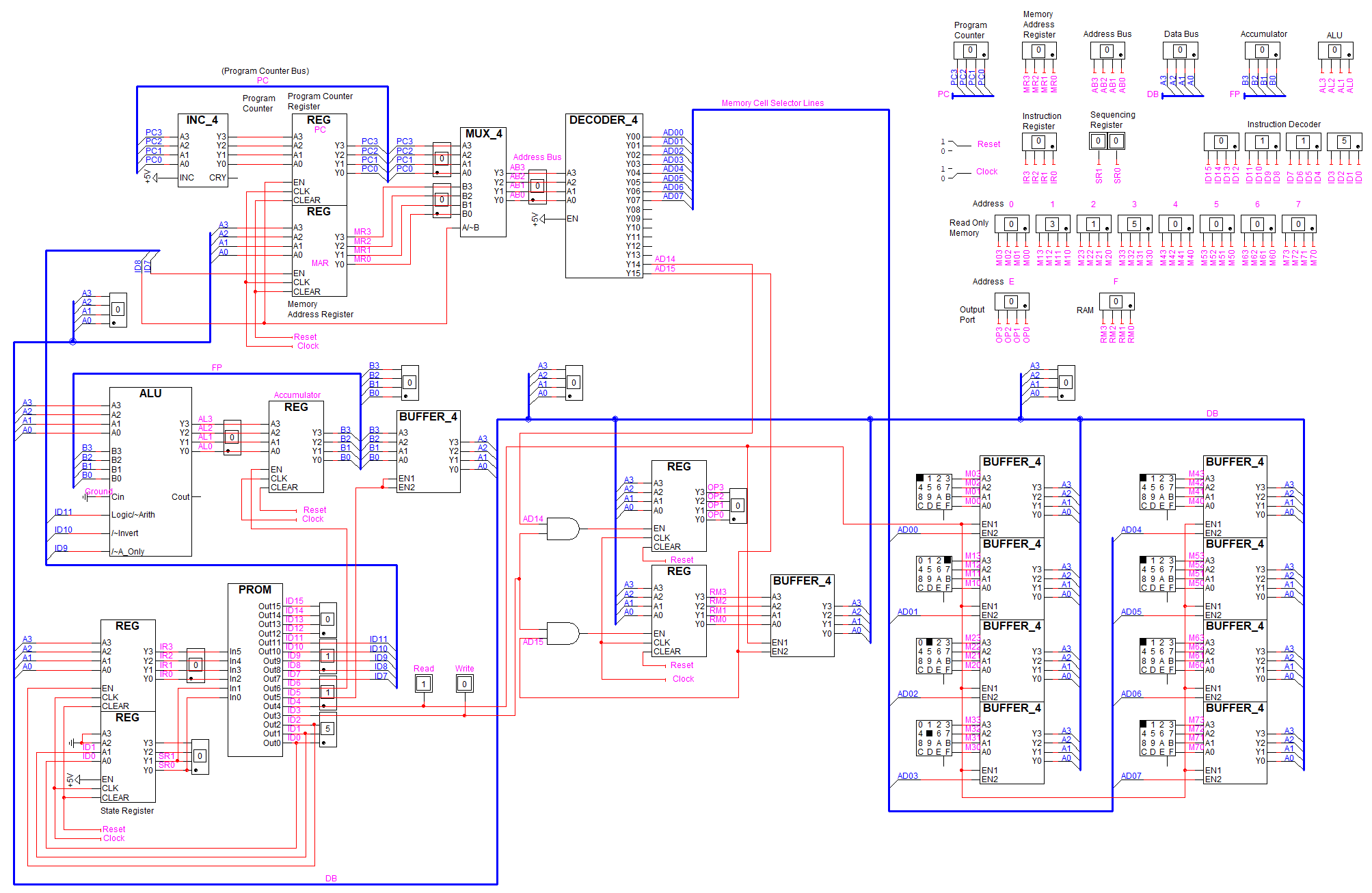
Description automatically generated

5\_10\_Microprocessor controller circuit\_TESTING

A diagram of a program

Description automatically generated

5\_12\_Test circuit for instruction decoder



5\_13\_The complete microprocessor circuit