Eyad Tarek Nagy

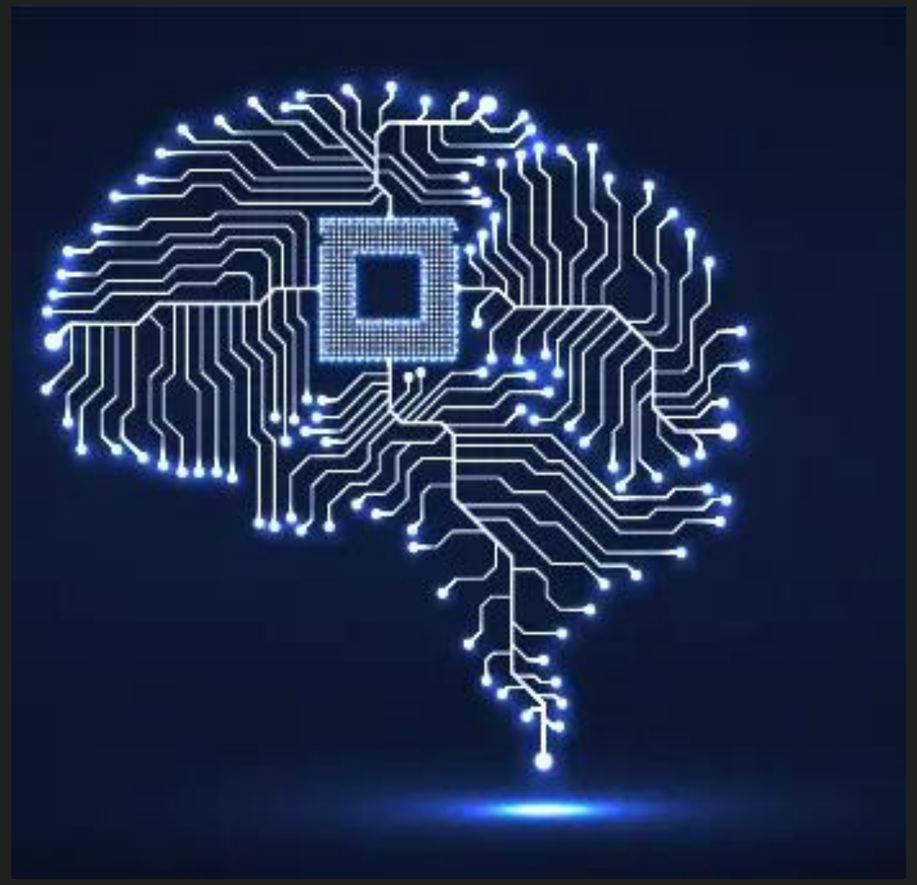
Digital IC design and Verification.

ABOUT ME

I am passionate about Digital IC Design and Verification, with a strong foundation in RTL design, logic synthesis, and verification methodologies. I enjoy solving complex hardware design challenges and ensuring reliable, high-performance circuits through simulation and testing. My goal is to contribute to developing innovative and efficient digital systems.

Why Me ?

Because i have make hardware implementation by three main HDL language (VHDL, Verilog,System Verilog) and because I combine a solid foundation in Digital IC Design and Verification with strong problem-solving skills and attention to detail.



Education

Ain Shams University

Bachelor, Computer and System engineering
2022 - 2027

SKILL

- Strong background in Logic Design & Computer Architecture.
- RTL Design & Verification expertise (VHDL/Verilog/SystemVerilog).
- Experience with Simulation and Synthesis tools(ModelSim,Vivado).
- Solid problem solving skills.
- Strong time management and meeting deadlines.

Work Experience

01. National Telecommunication Institute - NTI
Digital Design Using FPGA,

02. Udemy
System Programming in Linux,

Offered Services

Service 1

RTL Design (Verilog / VHDL): Developing efficient and optimized digital circuits.

Service 2

Functional Verification (SystemVerilog): Building robust testbenches to ensure design correctness.

Service 3

Digital System Simulation: Using industry tools (ModelSim, Questa, Vivado) for accurate performance analysis.

Service 4

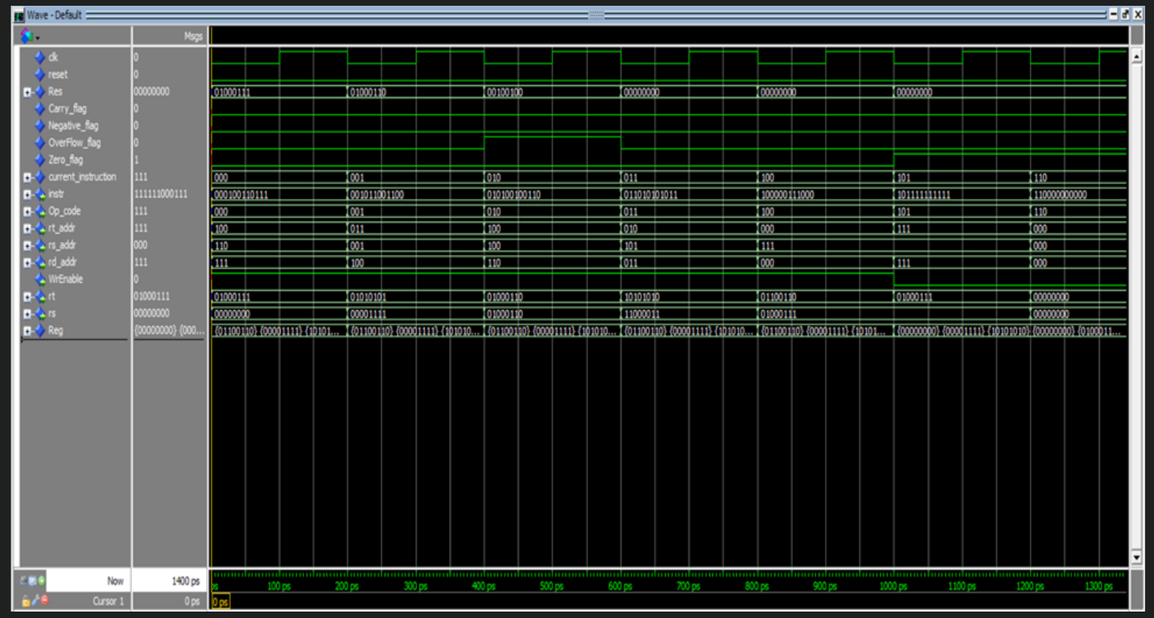
Synthesis & Timing Analysis: Ensuring designs meet timing and power requirements.

Service 5

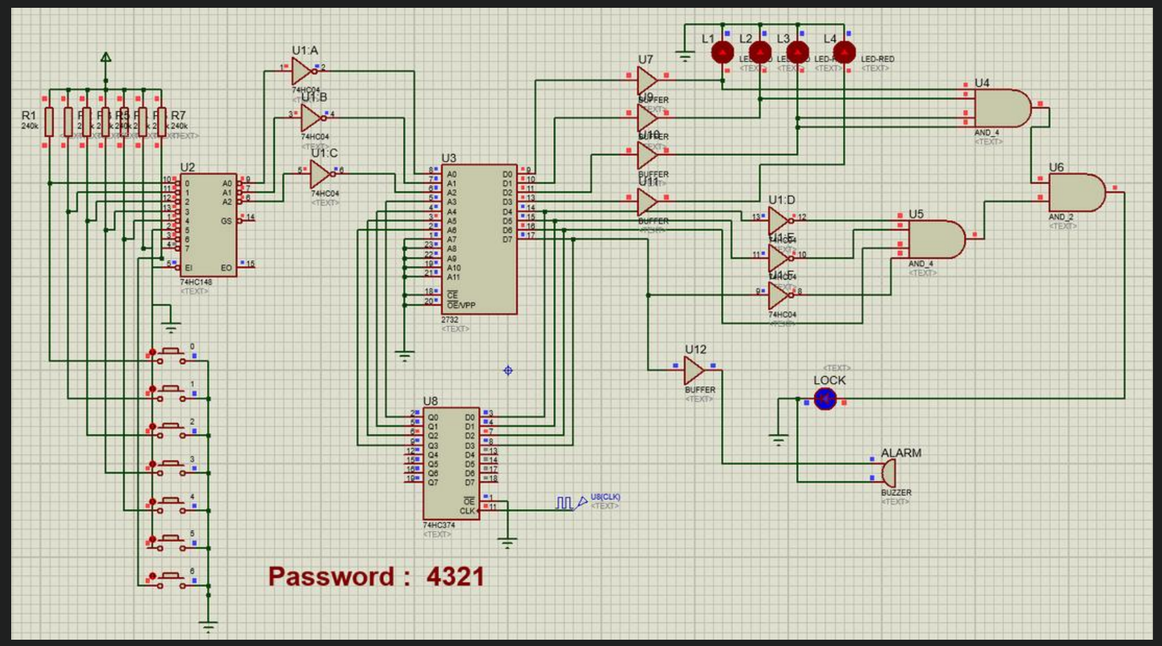
Documentation & Reports: Clear design specifications, test plans, and verification reports.

Projects

8-bit Microprocessor using VHDL

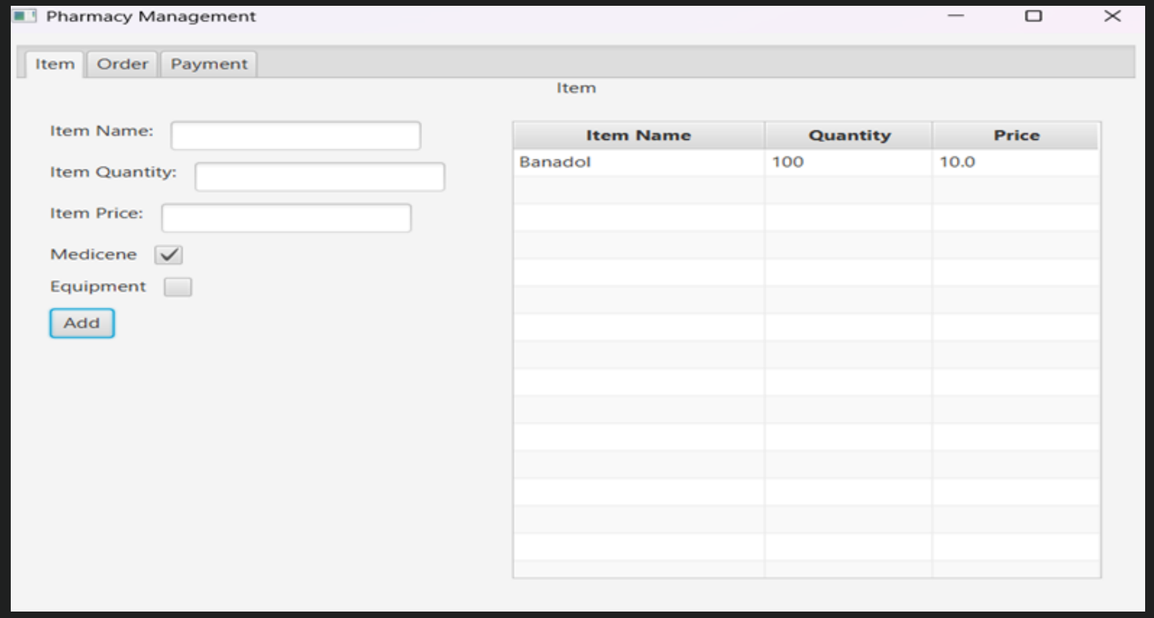


Digital Lock Circuits



CONT.Projects

Pharmacy Management System



I2C Master Communcation Protocol

```
module i2c_master_core (
    input  wire clk,
    input  wire rst_n,

    // I2C physical lines
    output reg  scl_o,
    output reg  scl_oe,
    input  wire scl_i,
    output reg  sda_o,
    output reg  sda_oe,
    input  wire sda_i,

    // CPU Master Interface
    input  wire         m_start_i,
    input  wire         m_stop_i,
    input  wire         m_read_nwrite_i,
    input  wire [6:0]   m_slave_addr_i,
    input  wire [7:0]   m_data_i,
    output reg  [7:0]   m_data_o,
    output reg          m_data_valid_o,
    output reg          m_busy_o,
    output reg          m_error_o
);
```

My Contact

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Thank You