Alexandria University
Faculty of Engineering

Computer Organization
Fall 2025
Sheet 7
Assigned: 2/12/2025
Due: 8/12/2025

Sheet 7

1. Explain briefly the function of the following signals of 8086
   a. TEST
   b. READY
   c. DT/R
   d. BHE
   e. INTR
   f. HLDA

2. For an 8086, draw a method of generating the read and write signals for memory and I/O under the isolated IO paradigm. Draw the circuit and specify the signals.

3. Design decoder address that locates three block of memory
   a. 00 0000 → 7F FFFF
   b. A0 8000 → A0 8FFF
   c. F0 0000 → FF FFFF

4. What is the difference between Full address decoding and partial address decoding putting emphasis on the mirroring effect?