Date : ____/____/____

Sheet 6

(1)

(a) TEST This is used to synchronize an external activity to the processor's internal operation after execution of the WAIT instruction.

(b) READY This is the acknowledgment from the slow device or memory that

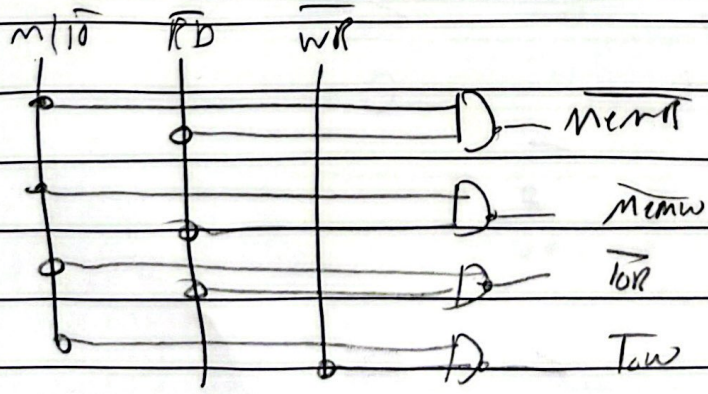
(c) DT/R output signal from the processor to control the direction of data flow through the data transceivers

(d) BHE it is used to enable data onto the most significant half of data bus D8 - D15

(e) INTR input signal used to inform the processor that a device requests an interrupt

(f) HLDA output signal from the processor informing the DMAC to use the bus for data transfer

(2)



Date : ____/____/____

(3)

	A_{23}	A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}–A_0
start	0	0	0	0	0	0	0	0	0	0	0	0	0
end	0	1	1	1	1	1	1	1	1	1	1	1	1
start	1	0	1	0	0	0	0	0	1	0	0	0	0
end	1	0	1	0	0	0	0	0	1	0	0	0	1
start	1	1	1	1	0	0	0	0	0	0	0	0	0
end	1	1	1	1	1	1	1	1	1	1	1	1	1

(4) In full address decoding, all high-order address bits are used to decode different ranges uniquely. This scheme leads to precise allocating of address ranges inside the whole memory.

In partial decoding, a subset of the high-order address bits is used to decode different ranges.