Sheet 8

1. Explain briefly the function of the following signals of 8086
   a. TEST
      This is used to synchronize an external activity to the processor's internal operation after execution of the WAIT instruction

   b. READY
      This is the acknowledgment from the slow device or memory that they have completed the data transfer.

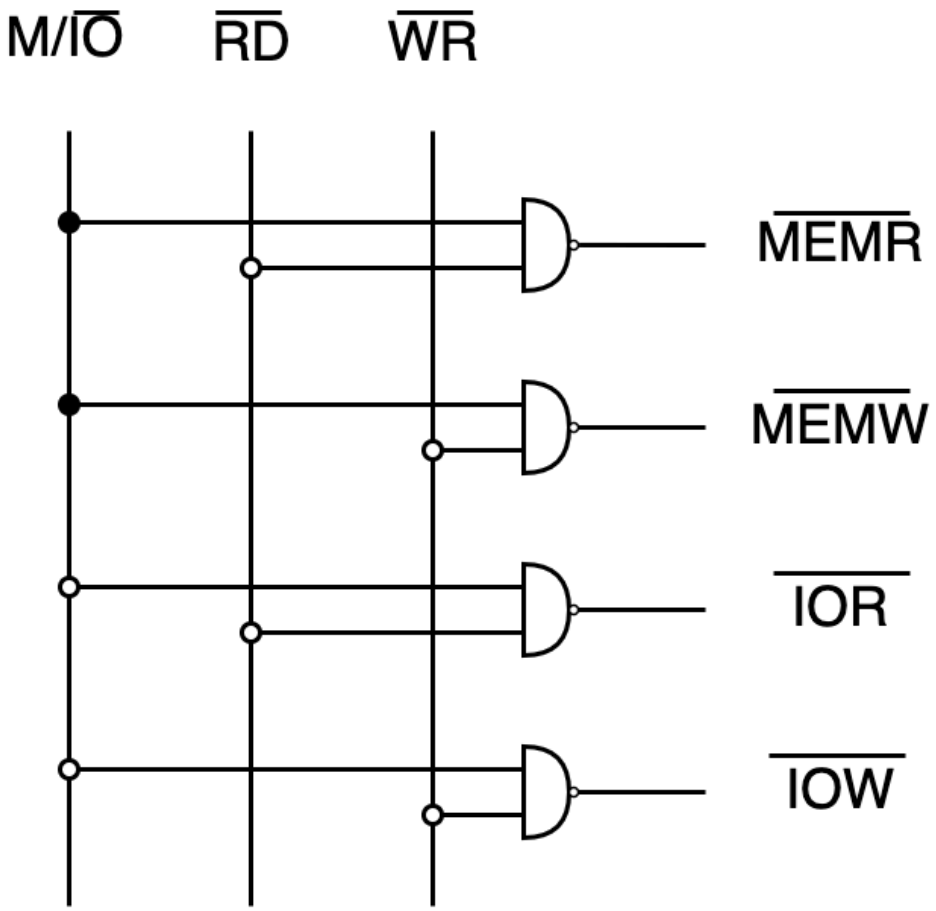
   c. DT/R
      Output signal from the processor to control the direction of data flow through the data transceivers

   d. BHE
      It is used to enable data onto the most significant half of data bus D_8-D_{15}

   e. INTR
      Input signal used to inform the processor that a device requests an interrupt

   f. HLDA
      Output signal from the processor informing the DMAC to use the bus for data transfer

2. For an 8086, draw a method of generating the read and write signals for memory and I/O under the isolated IO paradigm. Draw the circuit and specify the signals.



3. Design decoder address that locates three block of memory
    a. 00 0000 → 7F FFFF
    b. A0 8000 → A0 8FFF
    c. F0 0000 → FF FFFF

Direction	A_{23}	A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}-A_0
start	0	0	0	0	0	0	0	0	0	0	0	0	0
end	0	1	1	1	1	1	1	1	1	1	1	1	1
start	1	0	1	0	0	0	0	0	1	0	0	0	0
end	1	0	1	0	0	0	0	0	1	0	0	0	1
start	1	1	1	1	0	0	0	0	0	0	0	0	0
end	1	1	1	1	1	1	1	1	1	1	1	1	1

4. What is the difference between Full address decoding and partial address decoding putting emphasis on the mirroring effect?

In full address decoding, all high-order address bits are used to decode different ranges uniquely. This scheme leads to precise allocating of address ranges inside the whole memory space.

In partial address decoding, a subset of the high-order address bits is used to decode different ranges. Since we are leaving a part of the high-order address that is not used either in the decoding or actual allocation, we create a mirroring effect where the allocated address range is repeated multiple times inside the memory space