Simple Monolength Instruction Set (SMIS)

User Manual

Architecture overview

REGISTERS

4-bit addressing, supporting up to 16 general-purpose registers
16-bit data, supporting an unsigned value of up to 65,535
R0 is a constant zero value, can be referenced with RZR
R15 is conventionally used for stack pointer, can be referenced with RSP
R14 is conventionally used for base pointer, can be referenced with RBP
R13 is conventionally used for link register, can be referenced with RLR

MEMORY

16-bit addressing, supporting up to 65,535 halfwords of memory
16-bit data, supporting an unsigned value of up to 65,535

SYNTAX

Registers: R<number 0-15>
Immediates: #<16-bit unsigned value>
Comments: //<comment text>
Labels: <label name>:

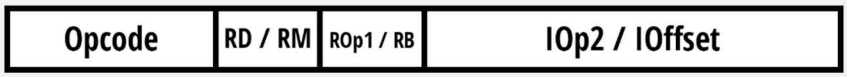
NOTES

All opcodes are 8 bits
Program is always assumed to begin at memory address 0

```
[I] SET                 <dest reg>          <immediate>
[R] COPY                <dest reg>          <source reg>

[R] ADD                 <dest reg>          <op1 reg>           <op2 reg>
[I] ADD-IMM             <dest reg>          <op1 reg>           <op2 imm>
[R] SUBTRACT            <dest reg>          <op1 reg>           <op2 reg>
[I] SUBTRACT-IMM        <dest reg>          <op1 reg>           <op2 imm>
[R] MULTIPLY            <dest reg>          <op1 reg>           <op2 reg>
[I] MULTIPLY-IMM        <dest reg>          <op1 reg>           <op2 imm>
[R] DIVIDE              <dest reg>          <op1 reg>           <op2 reg>
[I] DIVIDE-IMM          <dest reg>          <op1 reg>           <op2 imm>
[R] COMPARE             <op1 reg>           <op2 reg>
[I] COMPARE-IMM         <op1 reg>           <op2 imm>

[R] SHIFT-LEFT          <dest reg>          <op1 reg>           <shift reg>
[I] SHIFT-LEFT-IMM      <dest reg>          <op1 reg>           <shift imm>
[R] SHIFT-RIGHT         <dest reg>          <op1 reg>           <shift reg>
[I] SHIFT-RIGHT-IMM     <dest reg>          <op1 reg>           <shift imm>

[R] AND                 <dest reg>          <op1 reg>           <op2 reg>
[I] AND-IMM             <dest reg>          <op1 reg>           <op2 imm>
[R] OR                  <dest reg>          <op1 reg>           <op2 reg>
[I] OR-IMM              <dest reg>          <op1 reg>           <op2 imm>
[R] XOR                 <dest reg>          <op1 reg>           <op2 reg>
[I] XOR-IMM             <dest reg>          <op1 reg>           <op2 imm>
[R] NAND                <dest reg>          <op1 reg>           <op2 reg>
[I] NAND-IMM            <dest reg>          <op1 reg>           <op2 imm>
[R] NOR                 <dest reg>          <op1 reg>           <op2 reg>
[I] NOR-IMM             <dest reg>          <op1 reg>           <op2 imm>
[R] NOT                 <dest reg>          <op1 reg>

[I] LOAD                <dest reg>          <base reg>          <offset imm>
[I] STORE               <src reg>           <base reg>          <offset imm>

[J] JUMP                <dest label>
[J] JUMP-IF-ZERO        <dest label>
[J] JUMP-IF-NOTZERO     <dest label>
[J] JUMP-LINK           <dest label>

[J] HALT
```

R(egister)-type: 4-bit destination register, 4-bit operand 1 register, 4-bit operand 2 register

I(mmediate)-type: 4-bit arithmetic destination/memory source or destination register, 4-bit operand 1 or base address register, 16-bit operand 2 or offset immediate



J(ump)-type: 16-bit destination immediate assembled from label