

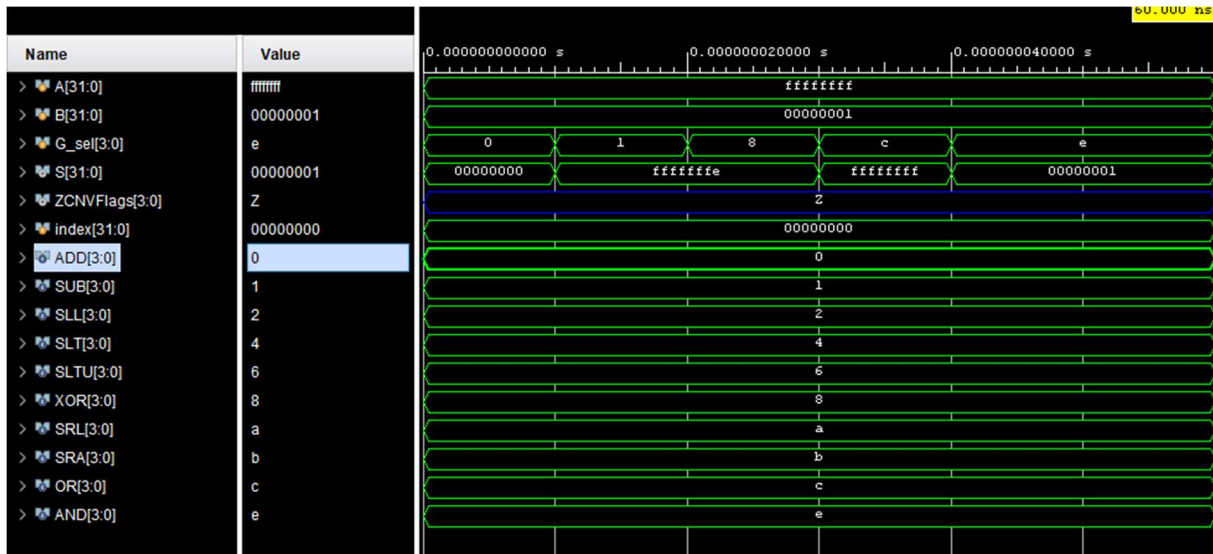
HW8

For the functional unit ALU and Shifter modules were designed. Ripple carry adder was modified to host the subtraction operation in addition. With this modification a single bit of funct7[6] can be used for carryin and operation selection.

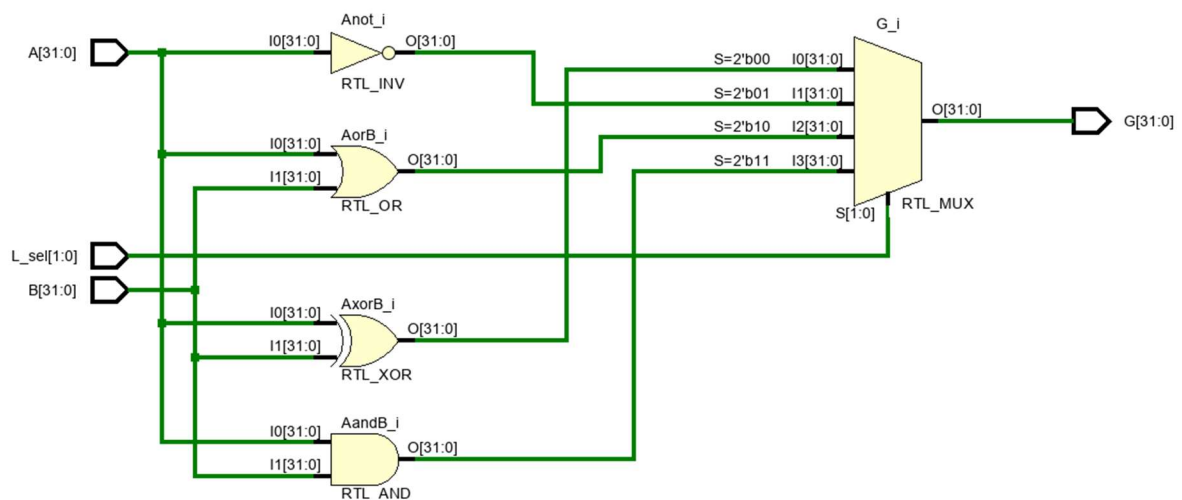
Flags are updated according to the result of ALU. Zero is detected by ORing the arithmetic result and NOTing. Overflow is detected by checking input sign bits, operation and the resulting sign bits.

Shifter is designed fully parametric with a barrel shift topology. The input and outputs are reversed to change the direction of the shift. 31st bit is used for arithmetic sign extension.

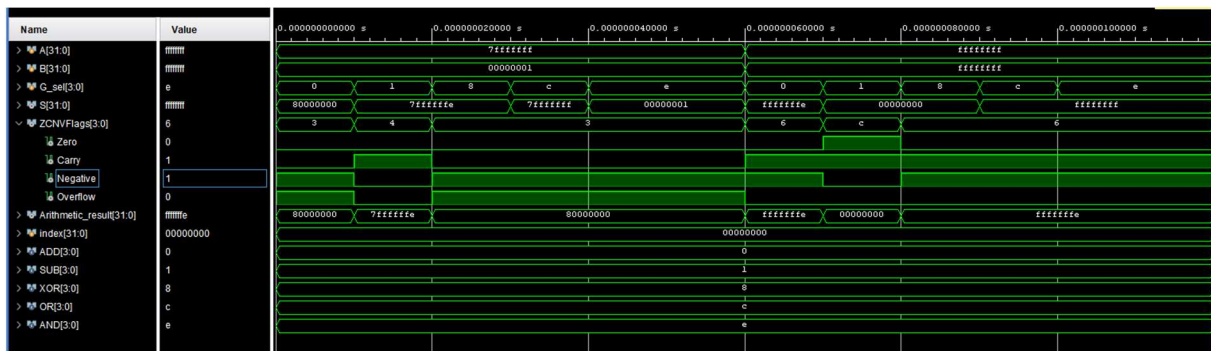
ALU simulation:



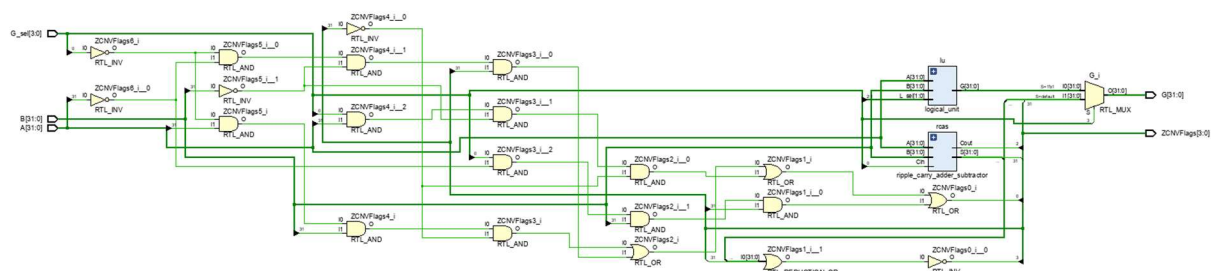
Logical unit RTL schematic:



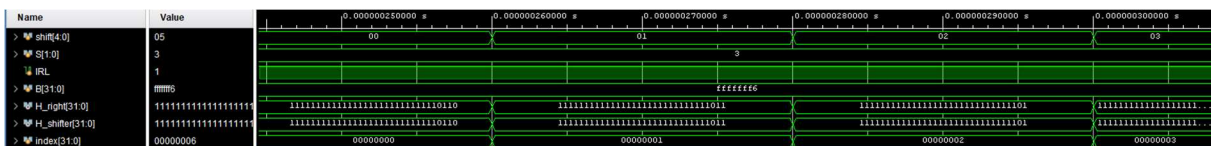
ALU simulation with Flags:



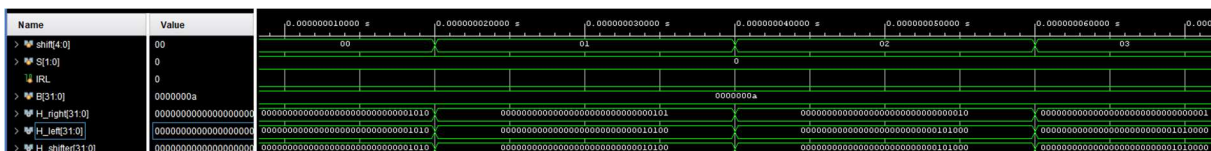
ALU RTL schematic:



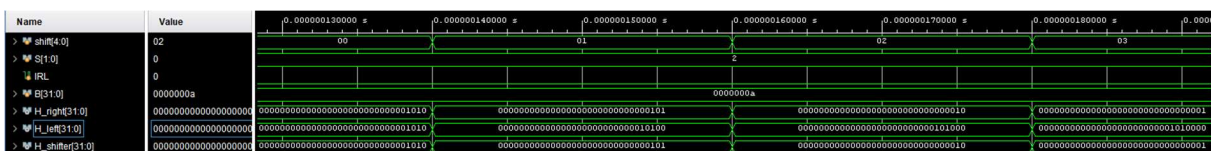
SRA: Arithmetic shift can sign extend the number as can be seen below.



SLL:

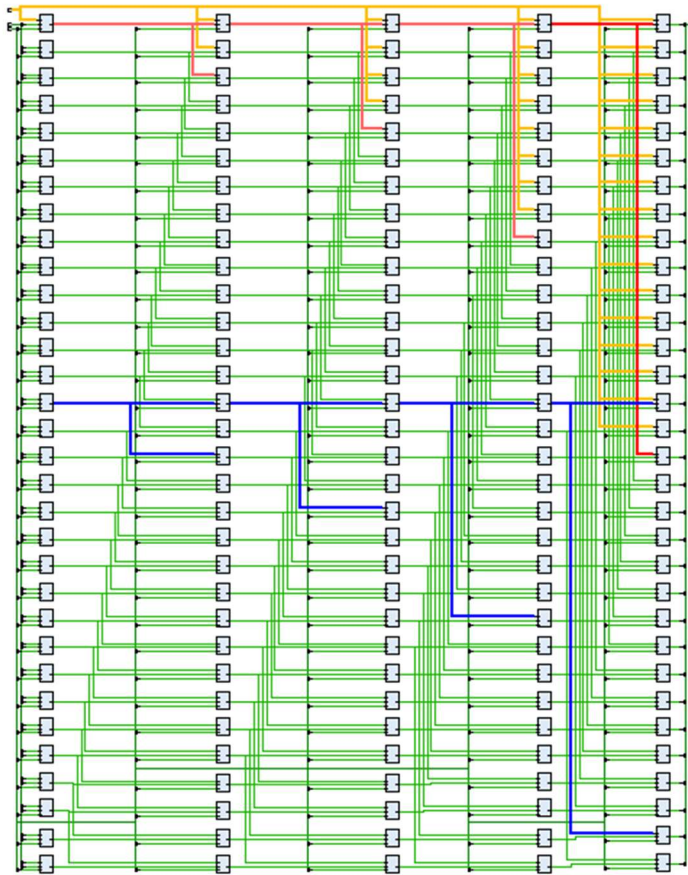


SLR:

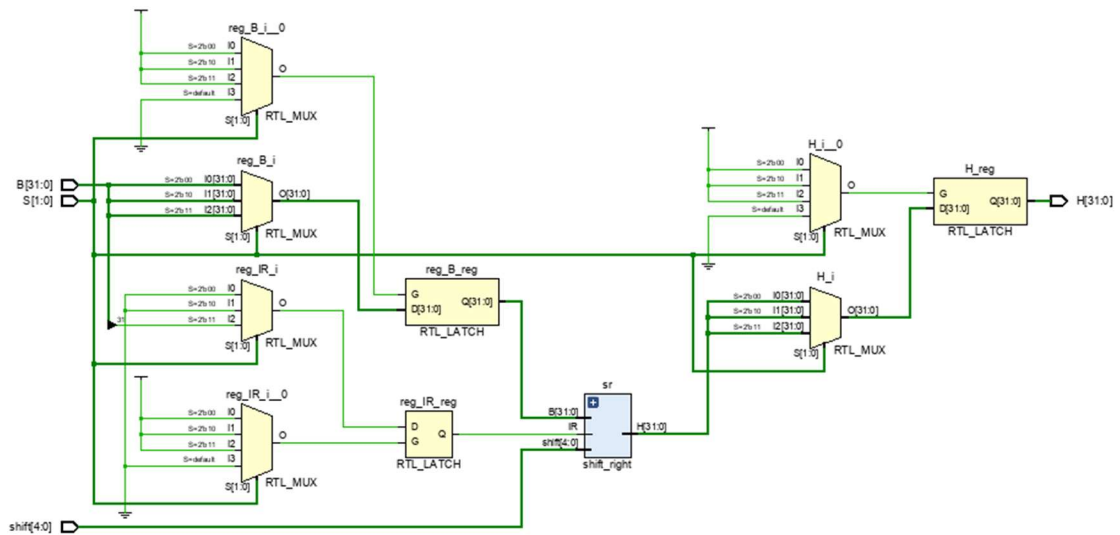


Barrel Left Shifter RTL schematic:

Orange highlighted line is connected to the IR/IL bit which gets shifted into the number. Red and blue highlighted lines indicate the pattern of 2^n .

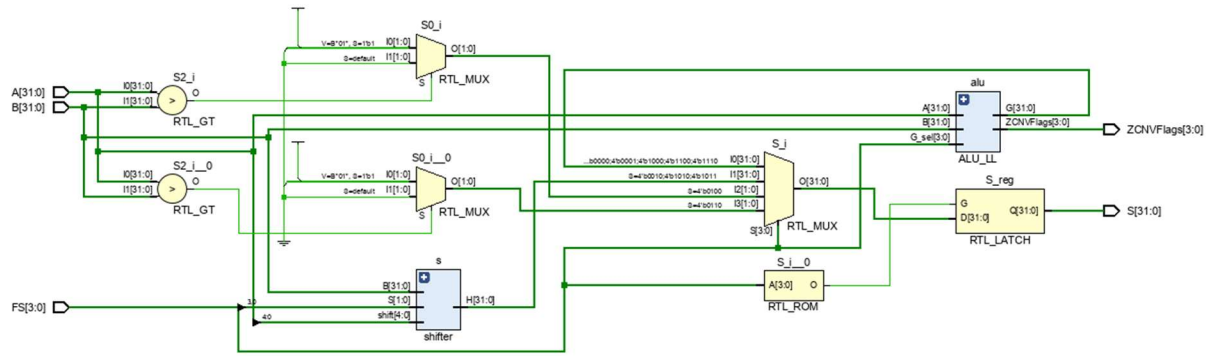


Shifter RTL schematic:



Functional Unit RTL schematic:

Mehmet Eymen Ünay



Functional Unit Simulation:

