Universidad Rafael Landívar
Facultad de Ingeniería
Ingeniería en Industrial y de Sistemas
Arquitectura del Computador I
Ing. Jefferson Esquivel

Laboratorio No. 2

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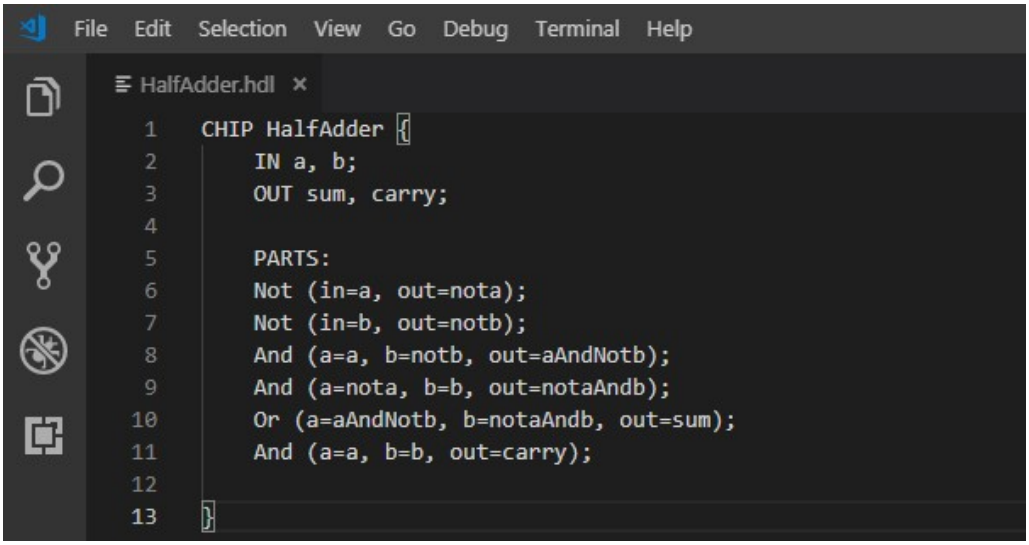
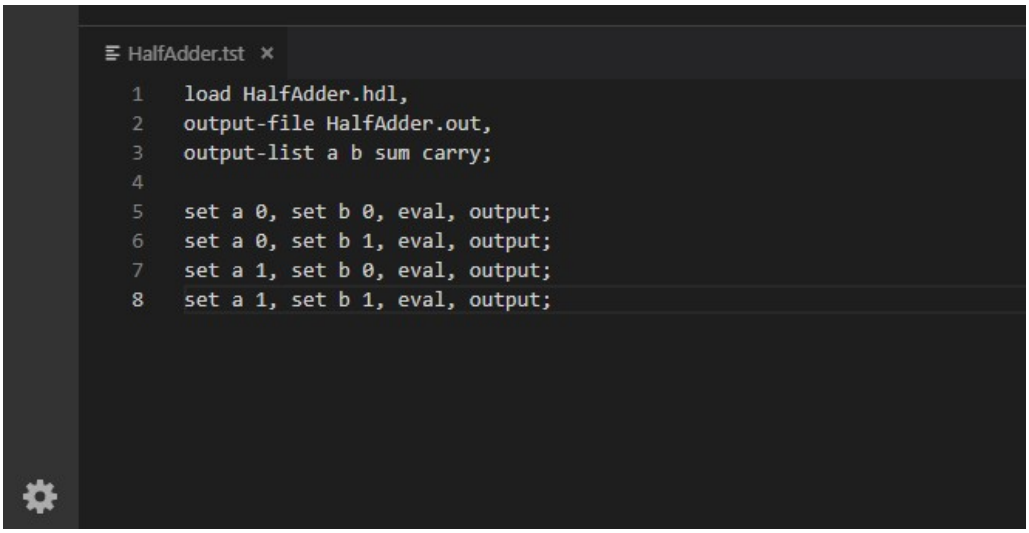
Guatemala, 31 de enero del 2019

Screenshots

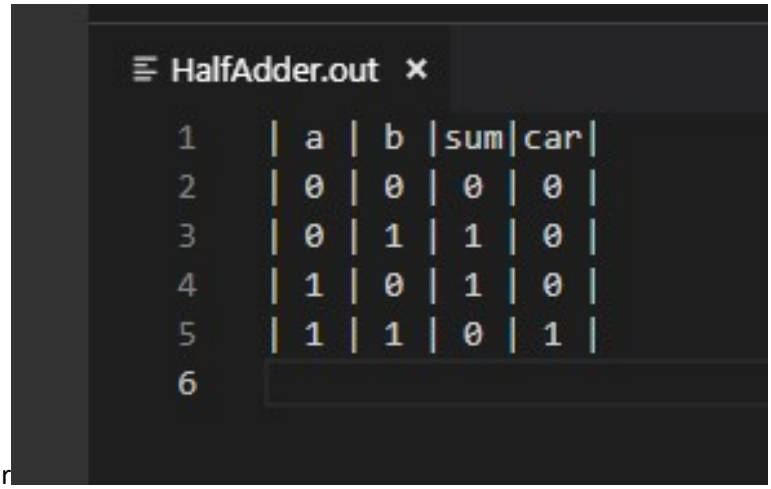
Archivo HDL del medio sumador



Archivo para pruebas del medio sumador

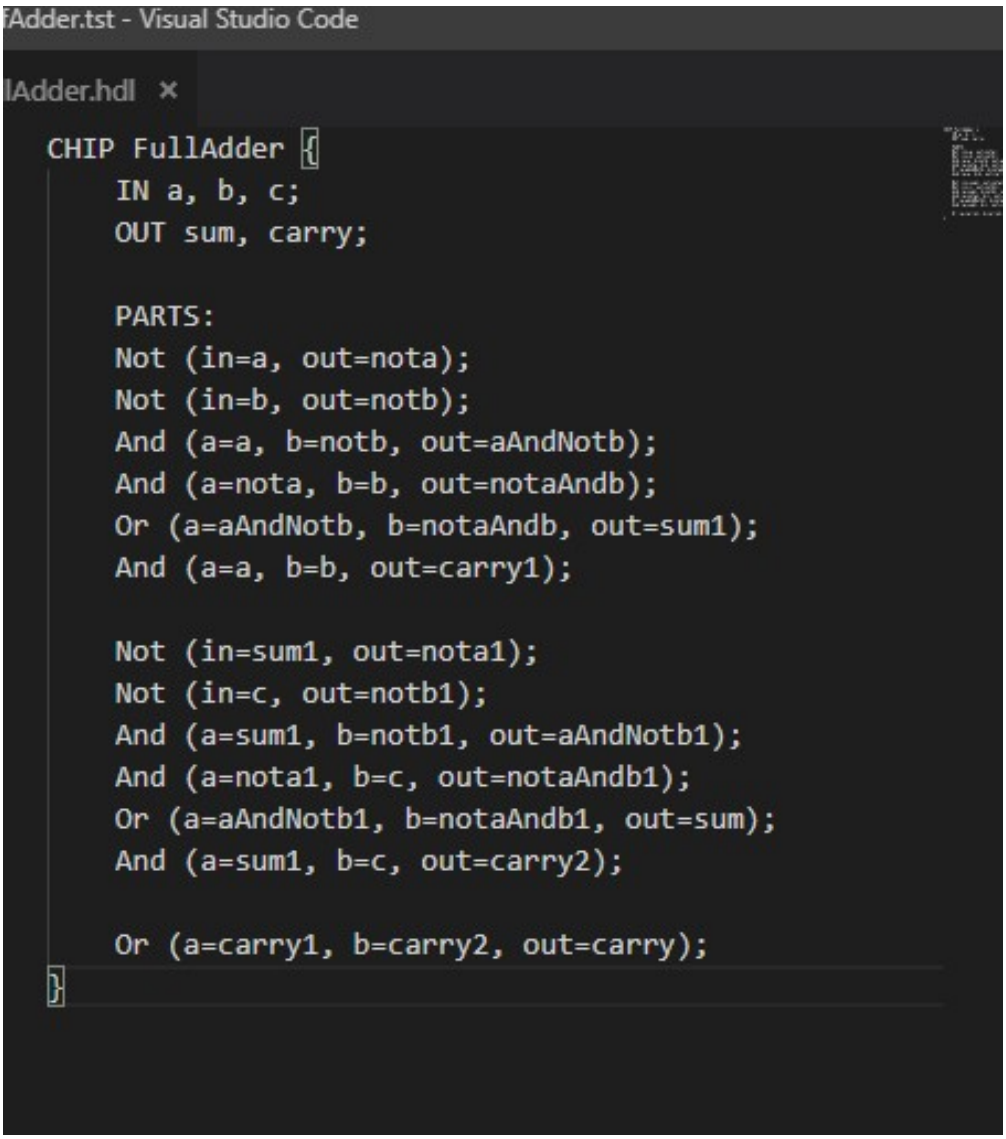


Salida del medio sumador y la tabla de verdad para comparar



Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Archivo HDL del sumador completo



Archivo de pruebas para el sumador completo

FullAdder.tst

```
load FullAdder.hdl,
output-file FullAdder.out,
output-list a b c sum carry;

set a 0, set b 0, set c 0, eval, output;
set a 0, set b 0, set c 1, eval, output;
set a 0, set b 1, set c 0, eval, output;
set a 0, set b 1, set c 1, eval, output;
set a 1, set b 0, set c 0, eval, output;
set a 1, set b 0, set c 1, eval, output;
set a 1, set b 1, set c 0, eval, output;
set a 1, set b 1, set c 1, eval, output;
```

Salida del sumador completo y tabla de verdad para comparar

FullAdder.out

```
| a | b | c |sum|car|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |
```

A	B	CarryIn	CarryOut	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1